Analog Electronic Circuits
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Lecture 24
Use of Current Mirrors in Differential Amplifiers

Lecture number is 24th today and we are going to discuss the use of current mirrors in differential amplifiers. This discussion had already started. We wanted this R E E to be replaced by a current mirror because we could not use R E E indefinitely in a lumped form because of two difficulties, one is difficulty of fabrication in integrated circuit and the other is difficulty of increasing what? Supply voltage.

The third difficulty a companying difficulty is that if you increase the supply voltage, if you increase the resistance then there would be consequent increase of dissipation also and integrated circuits are not geared to dissipate a large amount of heat. So the circuit that we had proposed was the following. A simple current mirror capital R, let me draw this circuit again. This was Q 2, this is the reference transistor and then we have the second transistor where we want the current and this resistance was R E.

In the actual circuit of the differential amplifier this is to go to minus V E E and this is to go to plus V C C and this is the current that I want. We call this I sub C 1. This will actually be in the differential amplifier I sub E E, okay, I sub E E. Now this transistor is Q 1 and our interest was to find out what is the effective resistance, effective R E E offered by this transistor current mirror or we wanted to calculate this. And in the process we have taken some numerical values to illustrate the values and this we shall require now.

V C C was taken as 15, V E E was taken as 0, the current through the reference current was taken as 1 point 43 milliampere which means that this resistance is equal to 10 K, 15 minus point 7 divided by 10 K is 1 point 43 milliampere. I sub C 1 you wanted to be 50 microampere, as an example this is the level of current that is permitted in an integrated circuit differential amplifier.

Then R sub E was calculated as 1 point 68 K. With 15 microampere and 1 point 43 milliampere R E E was calculated as 1 point 6 K and we had assumed that V A 1 2 was equal to 100 volt and beta was assumed to be I do not remember, maybe 100.

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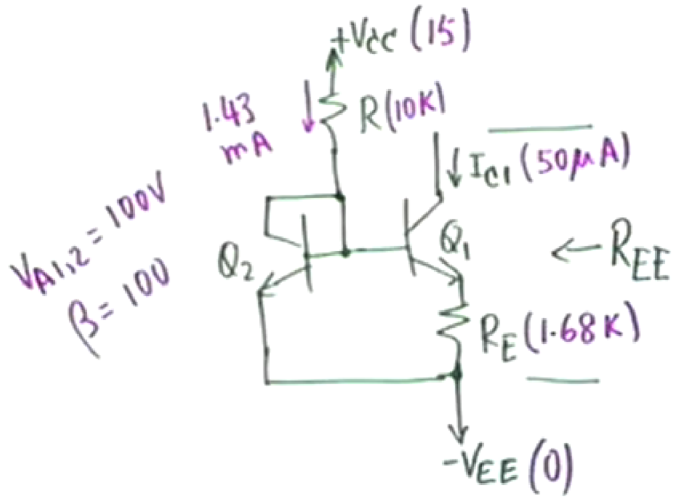

We will see as we go ahead.

Student: Sir, 200.

200? Alright, let us keep it at 100. I think we took it as 100. Beta was 100, yes. Okay, now we drew the equivalent circuit very carefully and we saw that in the equivalent circuit the resistance that is offered by the left of the circuit was the parallel combination of r pie 2 and what else? Capital R, r pie 2 capital R then r 02 because from collector to emitter and also that g m 2 V pie 2 was equivalent to a resistance of 1 by g m 2.

This we had agreed to call small r sub 1 and we also argued that because I C 1 is much less than I C 2, r pie 1 which is inversely proportional to I C 1 must be very large compared to r pie 2, agreed? And therefore r 1 is very small compared to r pie 1 and we could ignore it in the equivalent circuit, is the logic clear? Because the r pie is inversely proportional to collector current and the two collector currents are widely different. R pie 1 would be much larger compared to r pie 2 and r 1 is smaller than r pie 2 because it is paralleled by a number of other resistance.

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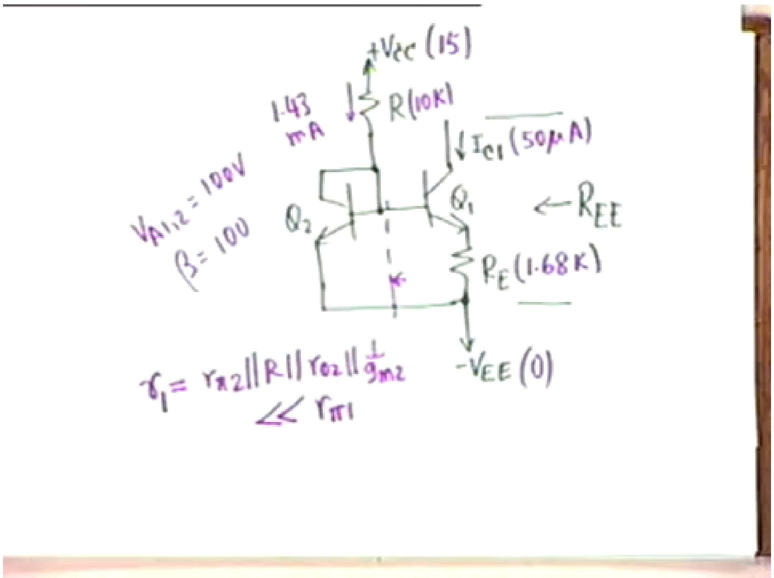

And therefore the simplified equivalent circuit would be like this. We have E 1, C 1. Between E 1 and C 1 we have g m 1 V pie 1 and the inevitable r 0 1. Now we cannot ignore r 0 1 because that is what we are going to calculate. The effective output resistance offered, okay. Then from C 1, well it is between C 1 and what? Which terminal? E 2, between C 1 and E 2. Between these two points what is the effective resistance?

So this is E 2 and this is the impedance that we want to calculate. Between E 1 and E 2, E 2 is the same as. No, between, I beg your pardon this is not E 1. Yes, this is E 1, C 1 to E 1. Between E 1 and E 2, between E 1 and ground there is a resistance of R E, okay. And in addition from E 1, r pie 1 because we have ignored r 1. R 1 is much less compared to r pie 1 and the potential difference is, which terminal is positive, lower one or upper one? Lower one, that is it, okay. This is the equivalent circuit by ignoring r 1.

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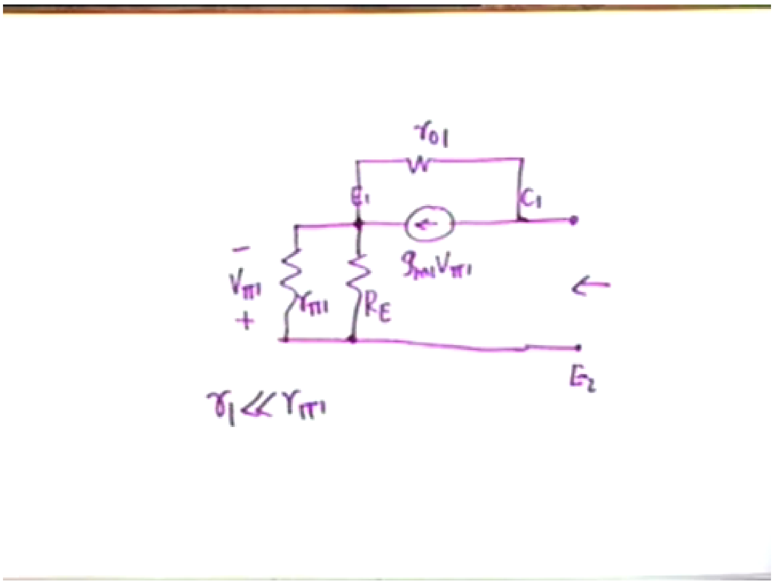

And to be able to calculate the effective impedance what we do is we connect a voltage source V and find the current I. You see the expression can almost be obtained by inspection. As you can see this current I is the same as the current flowing through this parallel combination and this is minus v pie 1. Minus because the polarity is this, divided by r pie 1 parallel R E.

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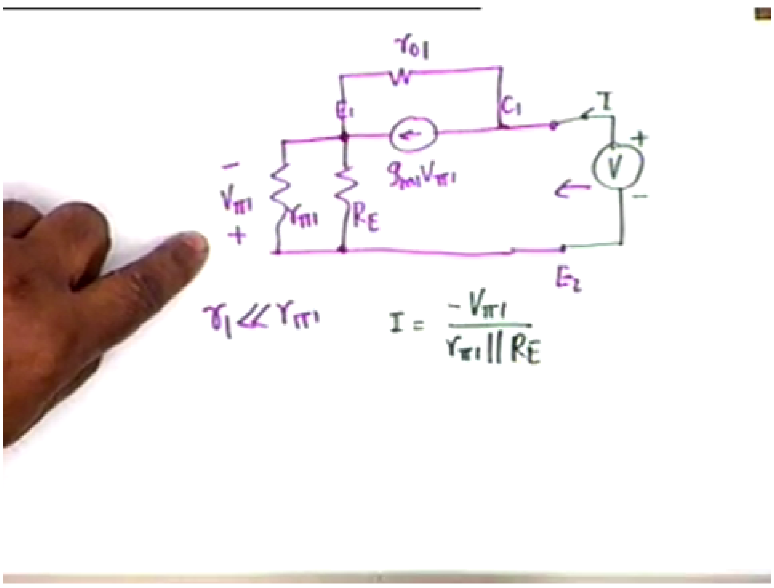

And if we write the KVL, V would be equal to the drop in r 0 1 plus that drop in R E parallel r pie. Therefore V is I minus g m 1 V pie 1. This is the current through r 0 1 multiplied by r 0 1 then minus V pie 1, is that okay? The drop in this plus the drop in this which is minus V pie 1. Therefore you can eliminate V pie 1 from these two equations and obtain the value of effective r 0 which is equal to V by I, a bit of algebra will give you the following expression, r 0 1 plus r pie 1 parallel R E multiplied by 1 plus g m 1 r 0 1. This is what we get.

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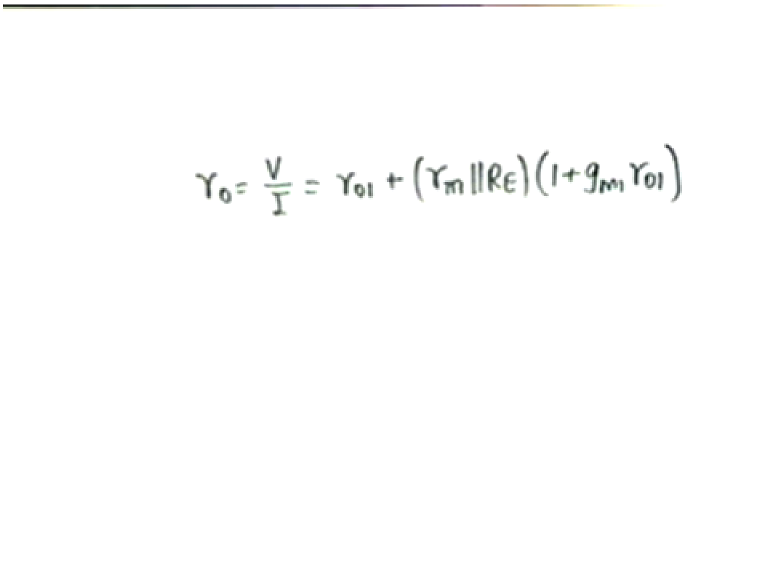

Now, one should notice that r pie 1 would be very large compared to R E. R E is only 1 point 68 K. What is r pie 1? R pie 1 is beta by g m. What is g m? I C 1 was assumed as 50 microampere divided by let us say 25 millivolt. This becomes 2 times 10 to the minus 3 volt. So beta is 100 divided by 2 times 10 to the minus 3 ohms that is equal to 50 K, agreed? So r pie 1 and what is R E? For the numerical example it was 1 point 68 K. Therefore r pie 1 is much greater than R E which means that this quantity is approximately equal to R E, okay.

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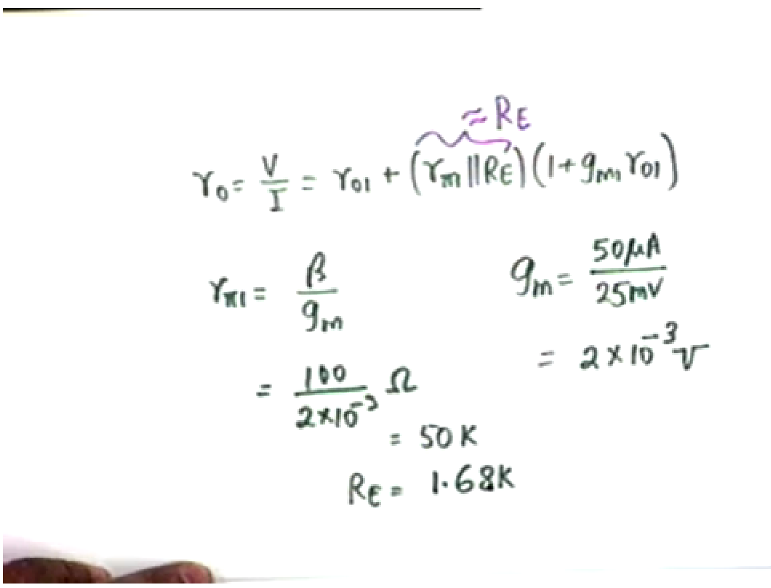

Now g m 1 is this. What is r 0 1? R 0 1 is V A which is 100 volt divided by I sub C 1 which is 50 microampere so this is equal to 2 meg, okay. 2 times 10 to the 6 therefore g m 1 r 0 1 is very large compared in other words this term can be ignored, agreed? From a practical example this term 1 can be ignored and therefore my expression simplifies to a very simple one and this is what is used for design. R 0 becomes equal to r 0 1, 1 plus approximately g m 1 R E. Let us take the values that we have got now.

If we calculate the values this is 2 meg r 0 1, we already calculated, 1 plus g m 1 is 2 times 10 to the minus 3 multiplied by R E is 1 point 68 multiplied by 10 to the 3. That means this is equal to 2 times 1 plus, how much is this? 3 point 26, agreed? So many meg? 3 point 36. How could I make that mistake? Okay. So it is 4 point 36 multiplied by 2, 8 point 72 meg.

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$$r_o \simeq r_{o1}(1 + g_{m1} R_E)$$
$$= 2(1 + 2\times10^{-3} \times 1.68\times10^{3})\,M\Omega$$
$$= 2(1 + 3.36)\,M\Omega$$
$$= 8.72\,M\Omega$$

Now you see the advantage of using a current source. By using two identical transistors which is of no concern in an integrated circuit because you make thousands on a chip. There is no problem on making two extra transistors and the resistors that you require one of them was 10 K and the other was 1 point 68 K which are both manageable within the pressings of integrated circuit.

With that the effective R E E that you have got is 8 point 72 meg and therefore C M R R would be twice g m R E. G m is 2 times 10 to the minus 3 multiplied by 8 point 72 times 10 to the 6. So how much that will become? Greater than 32000, okay. A very large C M R R and this is how this is why.

Student: Sir, (())(13:41).

Okay it is a good point. Actually this has been used wrongly. The actual value should be how much? Half of this. Why? Because I C 1 is I E E and therefore each transistor has half of this current. Each main transistor the differential amplifier is half, therefore it would be 1 time 10 to the minus 3 and this would be 16000. Even then the figure is very large. I am glad you pointed it out.

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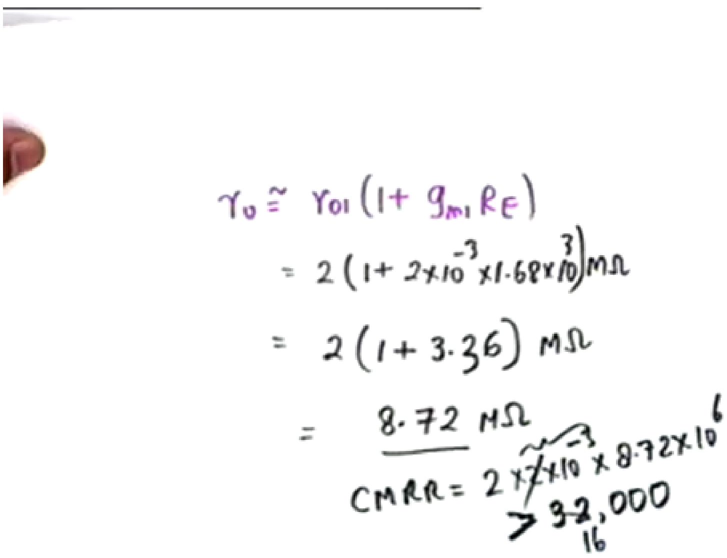

Student: Sir, can you please show the (())(14:27).

Equivalent circuit once again, I will show you twice, alright. The question?

Student: (())(14:37).

That is right. R pie 1 is between the E 2, this is E 2 and E 1. R pie 1 is from this point to this point, right? From base to emitter.

Student: (())(15:05)

See the resistance looking here was approximately zero. Compared to r pie 1 this was zero and therefore it connected to ground, is it okay. Now I just want to briefly recall the circuit. I feel lazy to draw this again. I have this drawn here. Is this coming on the monitor?

Student: No sir.

No? It is not coming, okay, alright. So our circuit how R E E is used is like this. V C C we will draw it quickly, R sub C, R sub C, then we have the two main transistors Q 1 and Q 2.

These are connected together. This is suppose to go to R E E, instead what we do is we take it to a transistor let us say Q 4, R E. This goes to minus V E E.

This is the main transistor of the current mirror and this is the (())(16:24) resistance R E and then from here we have the second transistor which we call Q 3 now, base connected to collector and this terminal comes to the reference resistor which was capital R, 10 K, the value that we used. And where should this go to? This terminal. The bases are connected to the sources R s, R s and whatever source V s 1 and V s 2.

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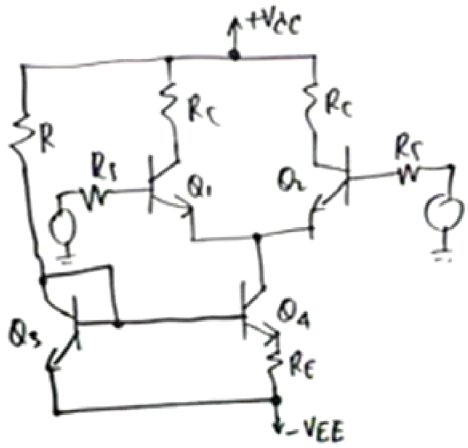

You see what I wanted to show you is how R sub C is used. This is the circuit that is R sub E E, okay. This pink coloured outline that gives you the equivalent to R sub E E. Now the next.

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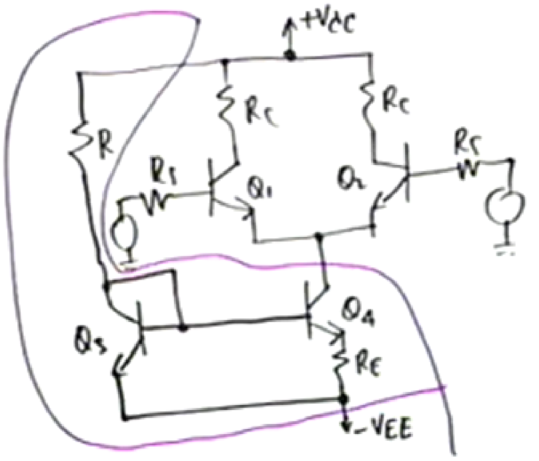

Student: Equivalent of R?

R E E, that is what was 8 point 72 meg in our example. Instead of that lumped resistance we have replaced it by this current reversal. Now the next point that we address ourselves to is the question of the differential gain and the common mode gain. You know the differential gain for a differential amplifier is minus g m R C. Now g m naturally would be a small quantity because the current is very small, current is of the order 50 microampere. G m as we said for this particular example was 2 times 10 to the minus 3 volt and therefore, pardon me.

Student: 1 into 10 is to 3.

Okay, 1 into 10 to the minus 3. So if you want to gain of 1 then R sub C is required to be a K, 1 K. The maximum R sub C that you can use is 50 K. Even that will give you gain of only 1. I am sorry, 50. Agreed? So on the other hand differential amplifiers are required to have a large gain and therefore we play the same trick that is we replace R sub C now by means of a current mirror. That is how the open circuit is being gradually built up.

That lumped resistor R E E has already been replaced by current mirror now we want to replace R C also by a current mirror so that we can use a large effective resistance without increasing the burden on integrated circuit fabrication or on the power dissipation or on the power supply also, okay. So we want to use instead of R sub C a current mirror.

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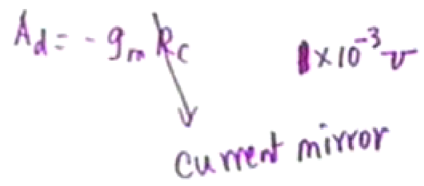

Now you must notice that A sub c, the common mode gain is minus g m R C divided by 1 plus twice g m effective R E E, okay. So if I increase R sub C it increases the common mode gain also, okay. It increases the common mode gain, it increases the differential mode gain but what we are interested in is the differential mode gain. We want it to be as large as possible. The C M R R is not affected thereby.

If you increase the R sub C, C M R R remains the same. C M R R we tackle by R E E, okay, and the absolute levels of gain either differential mode or common mode we take care by increasing R sub C by using a current mirror. Where such a node if we have an amplifier whose load R sub C is replaced by a current mirror obviously the load seizes to be passive, okay, because we are using a current mirror and current mirror is an active circuit. So we say that differential amplifier has active load.

That R sub C is replaced by an active circuit which is equivalent to a large resistance without causing any disturbance in the DC temperatures, okay. Large resistance we require under (()) (21:03) conditions, okay, that is effective R sub C. Now in order to be able to consider the use of an active load in a differential amplifier let us first consider a very simple trick namely a simple common emitter amplifier Q 1 let us say, it goes to minus V E E with an active load. We first consider a single stage C E amplifier with an active load, okay.

Let us say the voltage here is V sub i. We are only showing the AC voltage, okay. The biasing has to be done properly. What we want to do is instead of R sub C we want to use a current mirror. So what we want to do is we have to have a transistor whose collector current would be the same as the current of Q 1, okay. Now Q 1 is an NPN transistor so its collector current flows like this and if it is to flow like this then obviously this transistor cannot be NPN, it must be PNP, okay.

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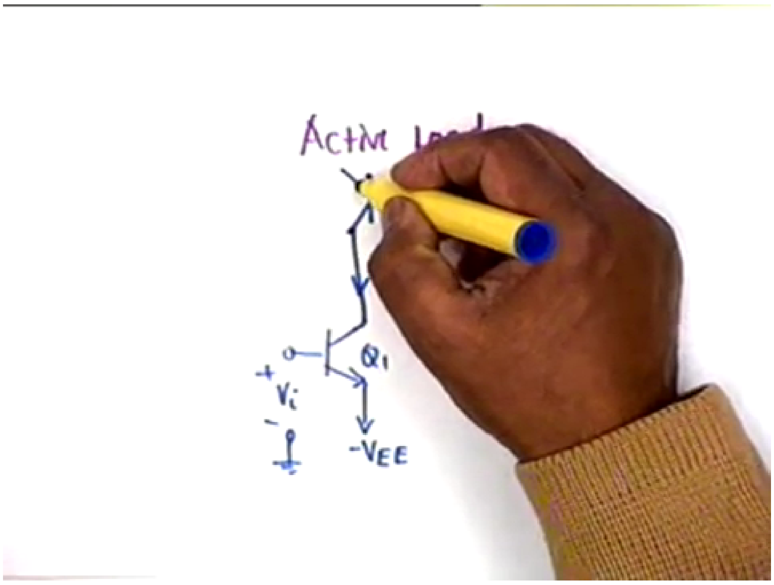

That is the first point we noticed and this will naturally go to plus V C C. This is the main transistor of the current mirror, we require an auxiliary transistor to set the reference. So what we do is we connect this to another transistor. This must also be PNP whose base and collector are connected together, alright. Then this collector must go to a power supply through a reference resistor R, let us call it R 1.

It must go now it cannot go to plus V C C. It must go to minus V E E. What do we do with the emitter here? It must be connected to ground because V B E must be identical. Is the circuit clear?

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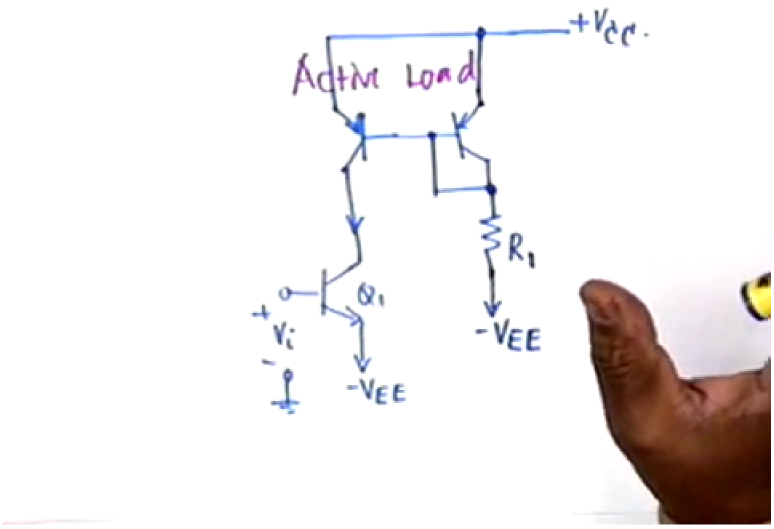

Student: We do not use the (())(23:18) circuit here?

We may if we require much lower current, okay. But if the problem is not of establishing a current here, our main purpose is to use the high valued equivalent resistor. Can you guess by simply looking at this circuit what the equivalent load of Q 1 is? What is the equivalent load of Q 1? One would be r 0 1, okay. Let me name these transistors Q 3 and Q 2. One would be from C 3 to E 3, it would be r 0 3 effective. Now is that all? There will also come in parallel.

Student: R 0 2.

No, not r 0 2. This point is not connected here.

Student: Sir, r pie.

No. R pie also we will not have it. R 0 1, is not it right? The load from here to ground, not plus it will come in parallel. That is what observation is, observation not seeing. Observation from here to ground is r 0 1 offered by Q 1. From here to ground V C C is also ground, r 0 3. So the effective load will be r 0 3 parallel r 0 1 and this is obtained purely by inspection.

I derived the circuit from common sense why PNP and why this connection and now common sense says that the effective load that is R sub C would be approximately equal to. There will be other factors but these two shall definitely be there. Yes?

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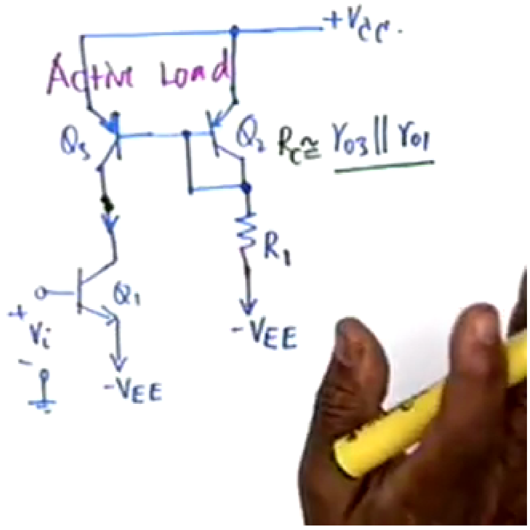

Student: Sir, please explain again why PNP?

Oh! Why PNP? Because the collector current of Q 1 has to flow like this and since our main transistor would be here, Q 3 collector must flow a current like this and.

Student: (())(25:28)

Okay, okay good point. We can invert the collector, we can replace the collector by emitter and emitter by collector. There is a problem. What is the problem?

Student: (())(25:44)

No, no, collector area is much larger than the emitter area. In a fabrication of a transistor since the collector causes the main dissipation, the area of semi conducted silicon area for collector is much larger than the emitter, okay. And therefore this is the natural mode and we shall have a problem if emitter and collector are interchanged. They are interchanged in some circuits where it is not very critical but where it is critical it is better to use a PNP and NPN.

And as I said, NPN and PNP in the same chip is no problem and they can be matched absolutely identical, okay. Now this result that the effective load is r 0 3 parallel r 0 1 has been derived by inspection, by observation. Let us see if this is correct by drawing an exact equivalent circuit. We will see something very funny there and that is why this equivalent circuit should be drawn with caution.

We start from B 1, base 1 of the transistor Q 1, okay. From B 1 it is always a good practice to identify the terminals from B 1 to E 1 you have the resistance r pie 1 and this voltage is V i, the AC voltage, this is V i. Then you have g m 1 V pie 1, okay. This terminal is C 1, collector 1 as well as collector 3, agreed? So this is C 1 and C 3. From C 1 to E 1 we shall have the resistance r 0 1 and from C 3 to E 3 which is the same as ground, from C 3 to E 3 you must do this very carefully.

From C 3 to E 3, E 3 is also grounded and therefore it is the same point, we have r 0 3. In addition from C 3 to E 3 we should have the current generator what? G m 3 times V pie 3 which we have not yet identified, g m 3 V pie 3, okay. Then we go to B 2 and B 3. B 2 and B 3 are tied together, connected together so from B 2 and B 3 to E 3 there shall be r pie 3 and this voltage would be V pie 3 with this polarity. What else should we have between B 2 3 and E 3? What else? We should have r pie 2.

Let me connect this so that I do not forget, okay and I do not have space here so I have brought it here down, okay. Now I am also trying to do something intentionally to confuse you. Do not be confused, okay. R pie 2, what else do I have here? I shall have because B 2 is connected to C 2, B 2 3 is also the same as C 2. So from C 2 to E 2 this is also E 2. We shall have this current generator g m 2 times, V pie 2 is the same as V pie 3, agreed?

So we have g m 2 V pie 3. There is a reason why I am writing this. What else do I have? No, from C 2 to ground we have two other resistors. Can you name them? One is.

Student: R 0 2.

R 0 2 and the other is.

Student: R 1.

R 1, that is absolutely wonderful, okay.

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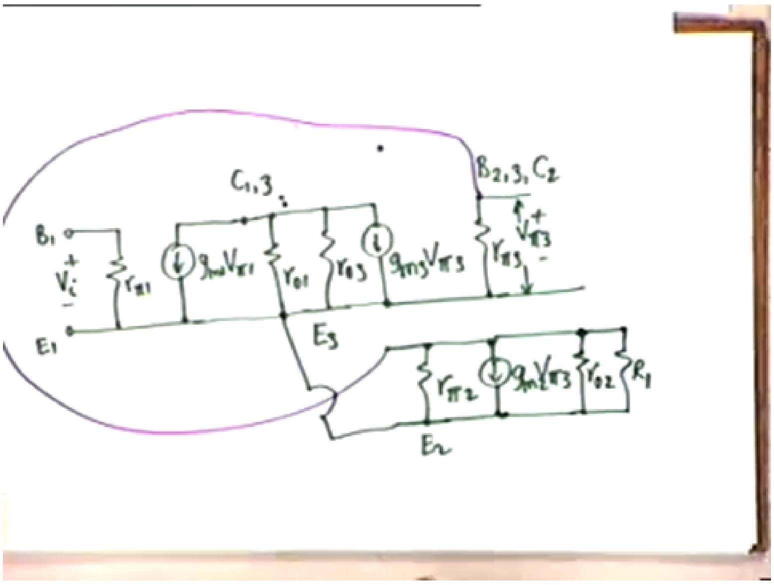

Now once again the point of observation or inspection, you look at this circuit r pie 3 parallel to r pie 2, g m 2 V pie 3, r 0 2 R 1. What is the voltage across this? Voltage across this current generator, V pie 3 and therefore this current generator is equivalent to a resistance 1 over g m 2. What is the voltage V pie 3 then? One, two, three, four, five dumb resistors connected in parallel, no source. So V pie 3 is identically equal to zero which means that this current generator also goes off.

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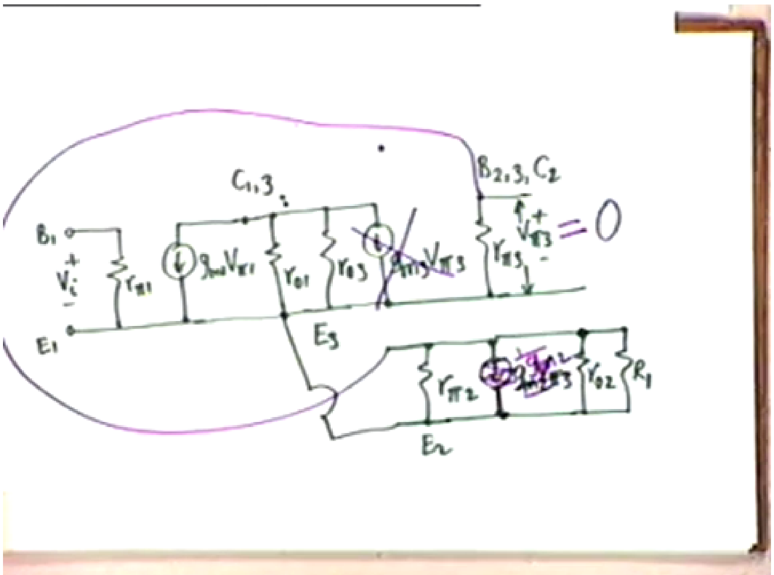

Student: Why is it zero?

Why is it zero? We have r pie 3, r pie 2, 1 by g m 2, r 0 2, R 1. Five, I gave the adjective of dumb, they are passive. Five passive resistors are in parallel, no source. What can be the voltage across this? Zero. If V pie 3 is zero then this current generator goes off and therefore what is the output impedance of this between C 1 and in 3? What would be the output impedance if I look at here?

It is simply r 0 1 parallel r 0 3 because V i equal to zero will mean V pie 1 equal to zero so the equivalent load that Q 1 faces, it is simple C amplifier with (())(32:09). Equivalent load is r 0 3 parallel r 0 1. So r 0 is equal to r 0 3 parallel r 0 1, okay. Which means 1 over r 0 equal to 1 over r 0 3 plus 1 over r 0 1, agreed? Now what is r 0 3? It is V A 3 divided by I sub C 3, agreed?

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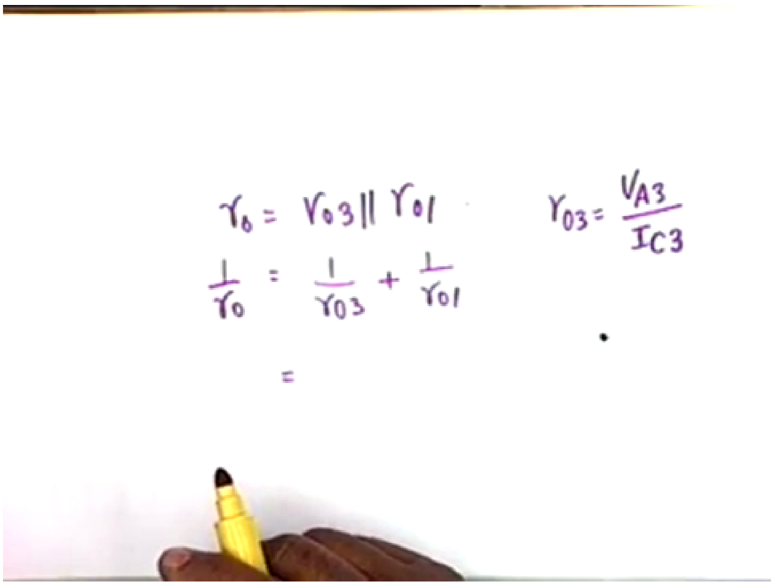

I have to go back to the circuit. What is the relationship between I C 1 and I C 3? They are identical, okay. Therefore I can write this as I sub C divided by V A 3 plus I sub C where I sub C is I C 1 or I C 3, is that okay? I C 1 and I C 3 that is correct because they are in series, the same current flows. So it is I sub C divided by V A 1. That is equal to I sub C, notice something very interesting that is coming up, V A 3 plus V A 1 divided by V A 3 V A 1. It is as if two voltages are connected in parallel, okay, alright.

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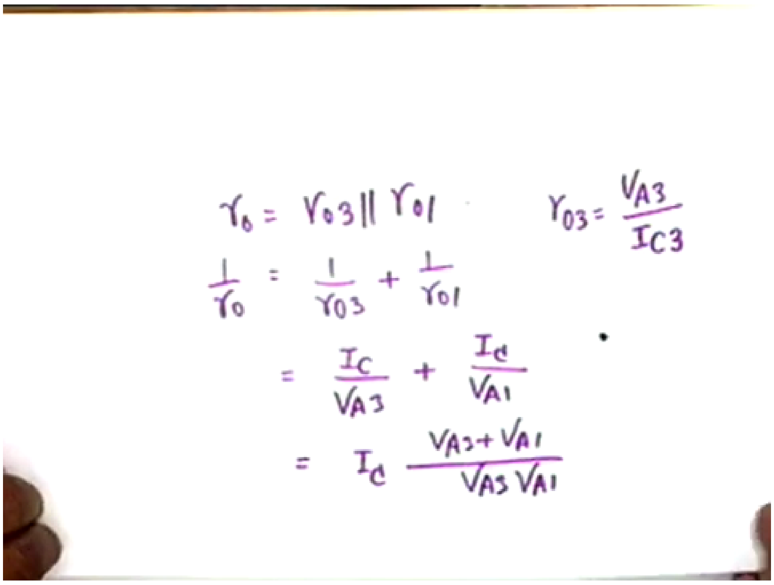

Now therefore r 0 is equal to V A 3 V A 1 divided by V A 3 plus V A 1 divide by I sub C. Therefore the gain A sub d would be minus g m times this load, okay, minus g m times r 0. What is g m? G m is I sub C divided by V T, 26 millivolt. Let us use it as V T for a moment then this multiplies r 0 which is V A 1 V A 3 divided by V A 1 plus V A 3 divided by I sub C and you notice that I sub C cancels.

Gain therefore is simply given in terms of 2 3 voltages which are internal properties of the transistor. Therefore the gain has become independent of external resistors, okay. It is independent of V C C, V E E, R and so on. It is simply determined by minus V A 1 V A 3 divided by V A 1 plus V A 3 multiplied by V T.

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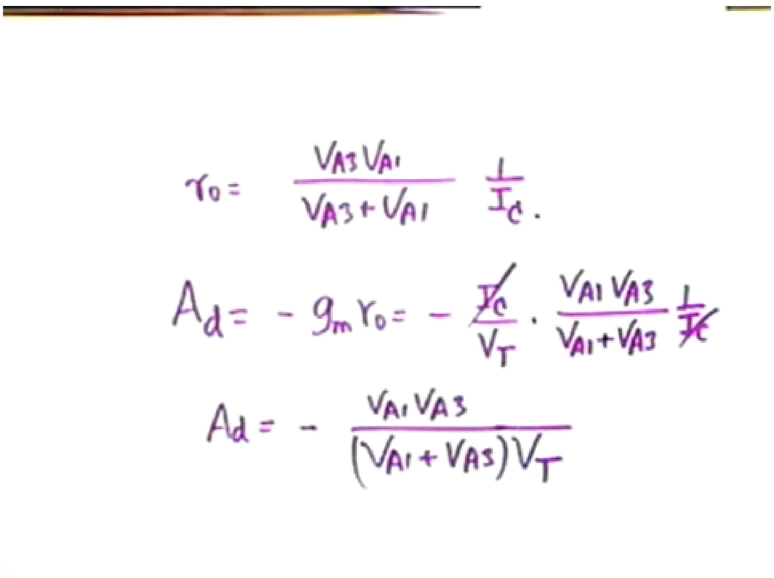

Gain has become independent t I sub C. So even if there is a small change of I sub C due to some other reason it does not affect the gain. The gain has been stabilized provided the early voltages, the thermal voltage of course depends on capital T, okay. So the gain is now determine, if it is a constant temperature in closer as is the case in most of the equipment that are used, well the A sub d becomes independent of all other conditions in the circuit, okay, except for temperature.

Now let us take a simple example. For the example that we have been using V A 1 equal to V A 3 let us say 100 volt and suppose V T equal to 25 millivolt. I want to calculate this in an easy manner. Then A sub d becomes minus 100 times 100 divided by 200 multiplied by 25.

Student: Into 10 to the power 3.

Into 10 to the power 3 which means so this is minus 2000, alright?

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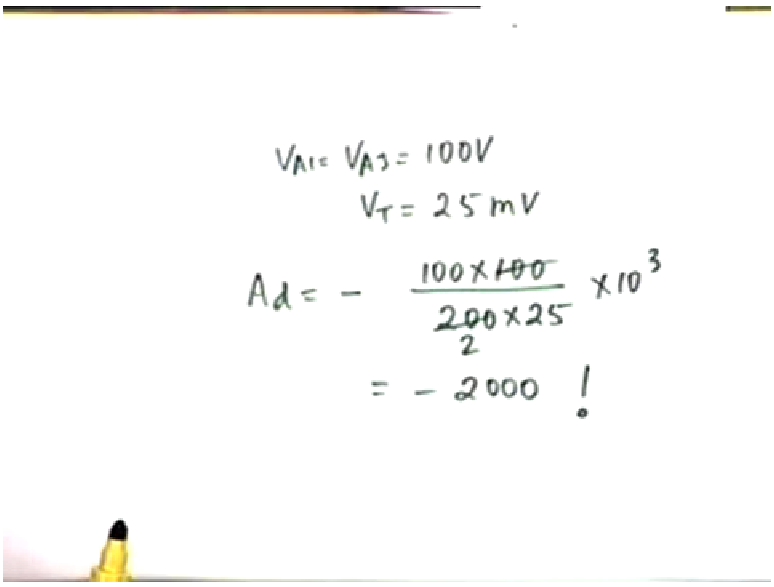

If the collector current is 1 milliampere then what is g m? 1 by 25. So if I have used a lumped resistance R sub C minus 1 over 25 and if this gain is minus 2000, what is R sub C required? How much?

Student: 50 K.

50 K. So what can be achieved by a 50 K resistance I am achieving by two transistors and a resistance. I have a resistance R 1. Now where does this resistance show its tip because the gain is independent of R 1. What does the resistance do? That sets what? The reference current I R.

Do not you see that I will just show the circuit. Here this current I R which will be approximately the same as I C 3 or I C 1, agreed? So this resistance sets the collector current and what we could achieve by a 50 K resistor we have achieved by using two transistors and one resistance.

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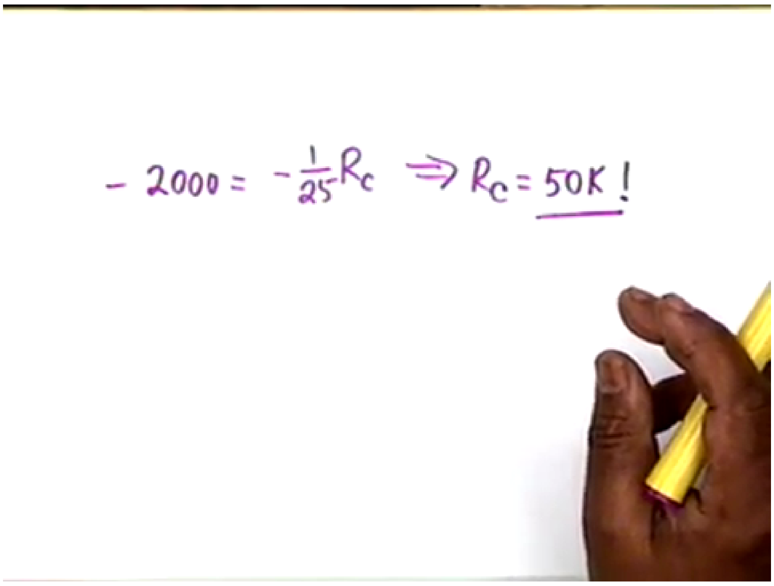

Student: (())(38:04)

How does it matter? You have to set a Q point.

Student: Okay. So that means the resistance is basically used for setting Q point.

That is correct. Q point means I sub C, okay. This is one of the peculiar examples of a case where elaborate equivalent circuit but it simplifies into a very small equivalent circuit, is that clear? Because V pie 3 was equal to zero and one has to be able to see it. Now what I will do is I shall draw a circuit which is very commonly used. A circuit of a differential amplifier with active load which is very commonly used. But in order not to complicate the circuit I shall show R E E as a lumped resistor, okay.

Otherwise I will have to draw R E E also and this size of the paper would not contain it. So I will show it as R E E. We have two main transistors Q 1 and Q 2. This is differential amplifier with active load, okay. We have the two bases. I will not show the base connections. I will show this as I have promised as lumped resistance. Actually this is also a current mirror. You can include this minus V E E and this current is I sub E E. Let me show the input. The input is applied between the two bases. This is V d.

Now the current mirror comes like this, the active load. You see we have two transistors Q 1 and Q 2. Naturally if a single common emitter amplifier requires two transistors for an active load, this should require four. But people are very clever, circuit designers. They deed with two and see how this connection is made. The two transistors in a current mirror circuit because the currents are identical that can be used for Q 1 as well as Q 2. So what one does is the following. This is a PNP transistor and this is a PNP transistor.

We call this Q 4 and Q 3. The reference transistor is now this one. The two bases have to be connected. This collector is connected to this base and the two emitters are now connected to plus V C C. So this is a single current mirror, agreed?

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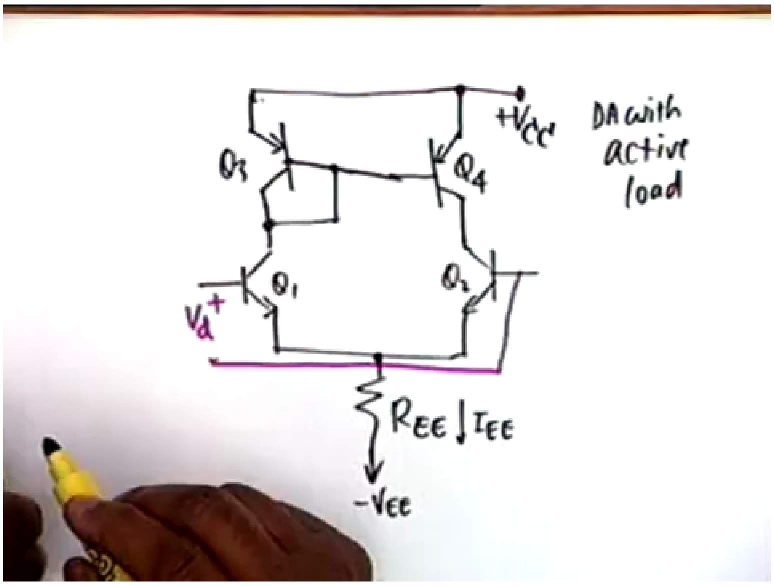

Problem, what is the problem? Who sets the reference for this current mirror? This I sub E E sets the reference. The two collector currents are I E E by 2. So as long as this is constant, as long as I E E is a current source which you achieve by using another current mirror and in that current mirror I E E is determined by a reference resistor, okay. So ultimately it goes back to a resistor but one reference resistor is enough for setting the reference values for Q 3 Q 4 and also Q 5 Q 6 which is used for R E E. Is the point clear?

Student: No sir.

No? You see for a current mirror we require the references resistor. Reference resistor would have been needed if this was referred to a resistance and the source. We do not require it here because I E E is again itself a current source and therefore I E E can act as a reference for Q 3 Q 4 current mirror. The collector current here would be simply I E E by 2. So if I E E is referenced then so is the Q 3 Q 4 current mirror. The current for this circuit is I E E by 2, okay.

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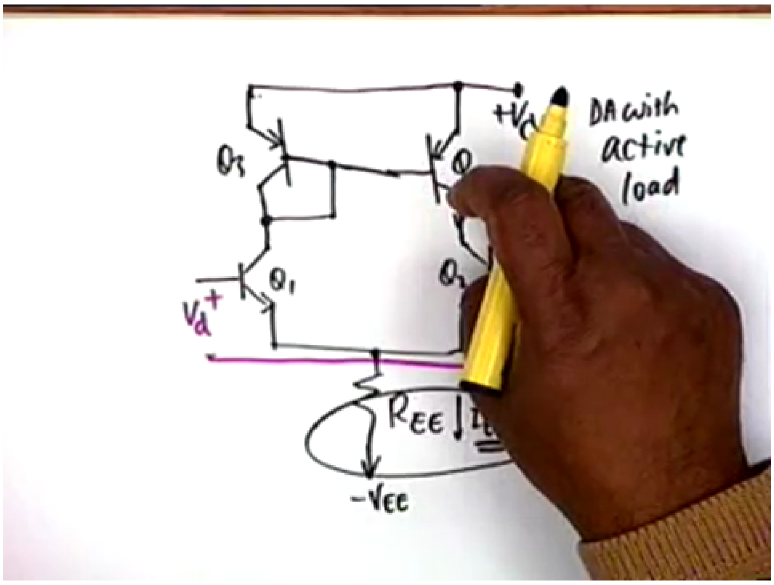

The other thing, the single output is taken from this. That is V 0. Can you tell me why? This is the reference transistor and therefore the output impedance is offered from this point to this point, okay. The effective load of Q 2 is this, r 0 4 in parallel with r 0.

Student: 2.

2 or 3?

Student: 2.

Student: 3.

No, not 3. 3 is the reference transistor therefore the output is taken from here, alright?

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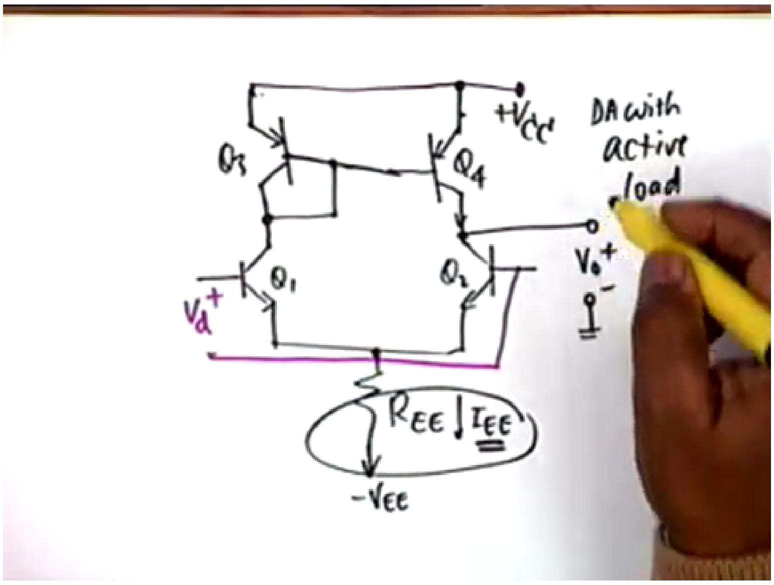

This is the circuit of a commonly used 741 or 5039 or whatever type or 701, whatever type you take this is how the active load is used. One can argue, the question has not arisen yet. I will raise the question and answer it myself. The question is are Q 1 and Q 2 now in a balanced mode of operation? You see Q 2 is supplied by Q 4 and Q 1 is supplied by Q 3 but the two transistors are not connected. Similarly the base is not connected to the collector here. Does that make a difference?

Ultimately it does not but that has to be found out by making an exact analysis which I find it convenient to leave it as a problem and the problem is the following for you. The first thing that I want you to show is that R L 1 that is the effective load of Q 1 is approximately equal to 1 by g m 1, show.

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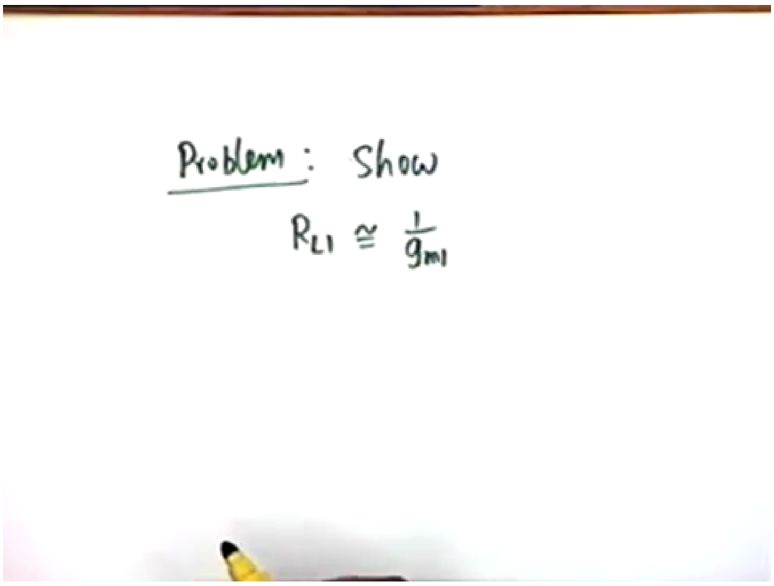

Obviously the effective AC load of Q 1 and Q 2 are not the same. This is approximately 1 by g m 1 for Q 1 and for Q 2 approximately r 0 2 parallel r 0 4 and they are not identical because the two gains are not identical. But still it does not matter. V 0 acts as the output of the differential amplifier and it has to be shown. The two AC loads are not identical, no longer they are R C, R C, okay. This is the first thing I wanted to show and the second thing is that V 0 by V d that is A sub d is approximately equal to g m. Which g m?

Student: G m 2.

G m 2 , does it differ . They are all identical. Q 1, Q 2, Q 3, Q 4, the collector currents are the same. So I am simply writing g m. G m multiplied by r 0 2 parallel r 0 4. This resistance is very high, this resistance is not that high. So the two loads are different. Also notice that there is no negative sign here. Can you guess why?

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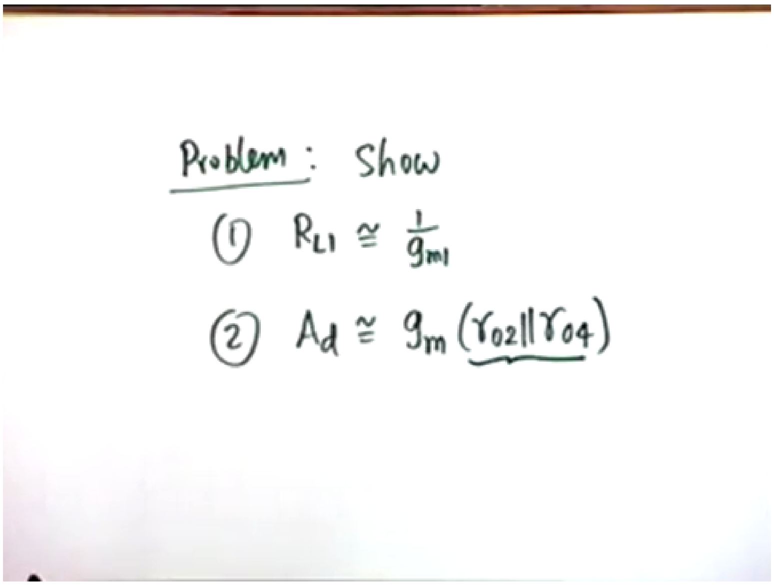

Alright, I also give that as a problem and I wanted to show that this is equal to well obviously this can be shown very easily that it is V A 2 V A 4 divided by V A 2 plus V A 4 multiplied by V T which is now independent of the collector currents and so on, okay. Hint, in showing this you do well to ignore r 0 1. If you do that the equivalent circuit will be simple and you will be able to find both these expressions.

And in many cases justifies the means. The ignoring of r 0 1 ultimately will be justified by seeing the effective load that Q 1 sees is not r 0 1 but 1 by g m 1 which is a small quantity compared to r 0 1 and therefore r 0 1 ignoring is justified, okay. Take this problem seriously and try to work it out.

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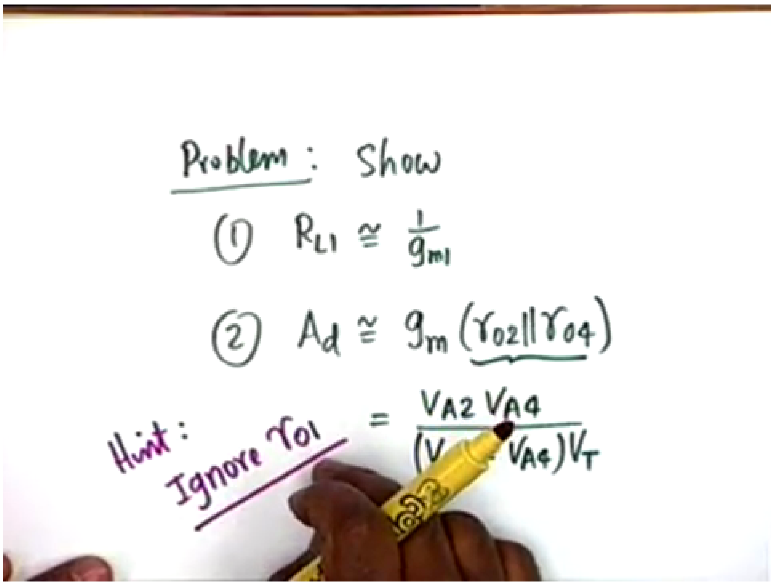

We next consider a differential amplifier using FET, field effect transistors, okay. And we shall see that the analysis is slightly different because of the current voltage characteristics of FET. This satisfies I sub D versus V G S is a square law relationship. However if we move through this jungle by clearing I D S S and V G S and V P we get very similar results. What I want to do now is simply to draw the circuit and continue its analysis tomorrow. The circuit as you can very easily guess is very similar.

We have two transistors Q 1 and Q 2, R s and V s 2, V s 1. Two transistors in which the two sources S 1 and S 2 are connected together instead of two emitters. Then this point goes an ordinary circuit. It will ultimately be replaced by current mirrors but the resistance which we shall now call as R sigma sigma. Instead of R E E it is R sigma sigma and this voltage is minus V, what should be the subscripts? Capital S capital S. Distinguish between this small s and capital S. Or you can use sigma sigma.

That is better so that we do not confuse. Capital S and small s after all capital S should be distinguished from non capital, okay. Q 1 and Q 2 and then we have two resistances R sub D and R sub D, the drain resistances. The two are connected together and goes to plus V D D. There is no confusion here. There is a confusion because the difference voltage you have used is, but there should be no confusion. It is V capital D as the DC difference voltage and V small d as the AC difference voltage.

So I used a double subscript here that is why there should be no confusion here either V S S. But it would be a matter of discipline to write capital S and small s and I strongly suggest that you write it like I sign my name, okay. I always sign my name with an s like this. I am not a capitalist, okay.

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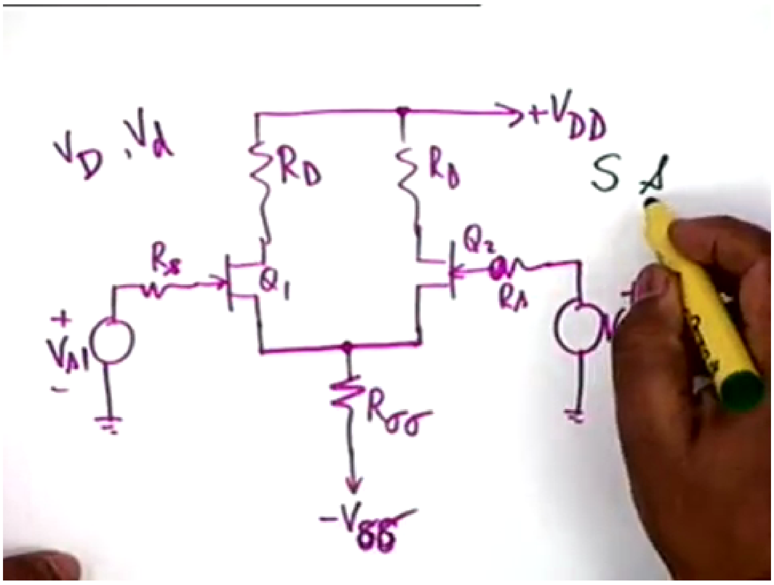

The two voltages are, how did we denote these voltages? V capital D 1, okay, and V capital D 2. There should be no (diff) confusion and this voltage is V O D plus minus. This is the basic circuit and if you know BJT, you know how to draw an FET circuit. The fact that FET operation is unipolar that is only one kind of carrier, the majority carrier device leads to a nonlinear relationship between I sub D, the drain current and the drain to source voltage.

Also the gain to source voltage has a limitation. V D S has to be greater than V G S minus V P, absolute value. So if all those limitations are taken into account we shall be able to show next time that A sub d is equal to minus g m. What do you expect?

Student: R D.

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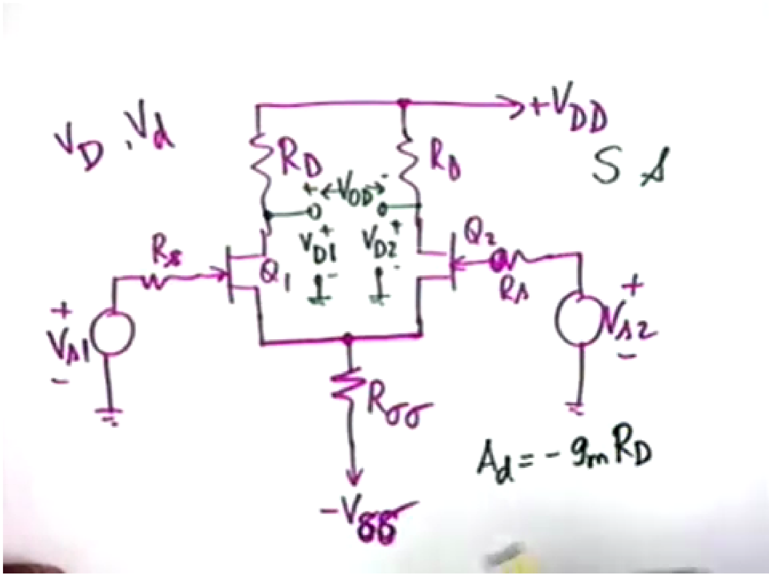

R D. We will be able to show that this is true and once we have established this the rest of the analysis is very similar and therefore I will not continue the analysis. I will leave it to you not completely. Partially I will illustrate this by numerical examples in the problem session. That is all for today.