Analog Electronic Circuits
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Lecture 21
Differential Amplifiers (Continued)

This is the 21st lecture and we continue our discussion on differential amplifiers. To recall the differential amplifier this is the circuit and we calculated the DC quantities. We assumed V B 1 minus V B 2 equal to V B D. And we found out an expression for V O D in terms of V D through the transistor junction relationship that is I sub C equal to I sub S exponential V B E by V T, V subscript capital T.

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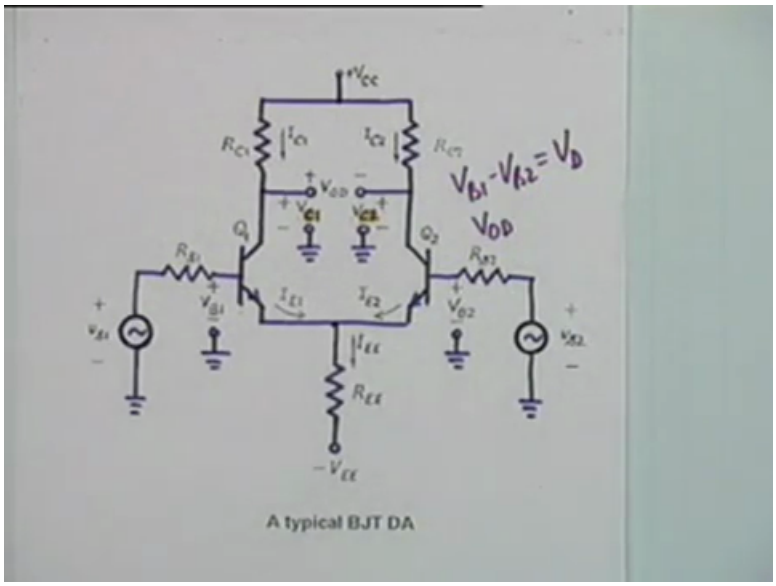

In the process we found out that the two currents I C 1 and I C 2 very exponentially like this that is one is negligible, the other is almost full and therefore there is a possibility of switching from one state to another and I commented that this forms the basis of utilisation of the emitter coupled pair E C P in E C L that is emitter coupled logic. From the two current variations we then went to the voltage variation that is V C 1 and V C 2 and we showed that V C 1 and V C 2 vary in this manner.

The same type of variation because they are linearly to I sub C 1 and I sub C 2 and V O D which is this curve is the difference between the two. V O D is equal to V C 1 minus V C 2 and we showed that when the range of V D by V T is between minus 2 and plus 2 the

variation is approximately linear and this is the range of operation, range of interest to ask in the analog electronics course because we want linear amplification.

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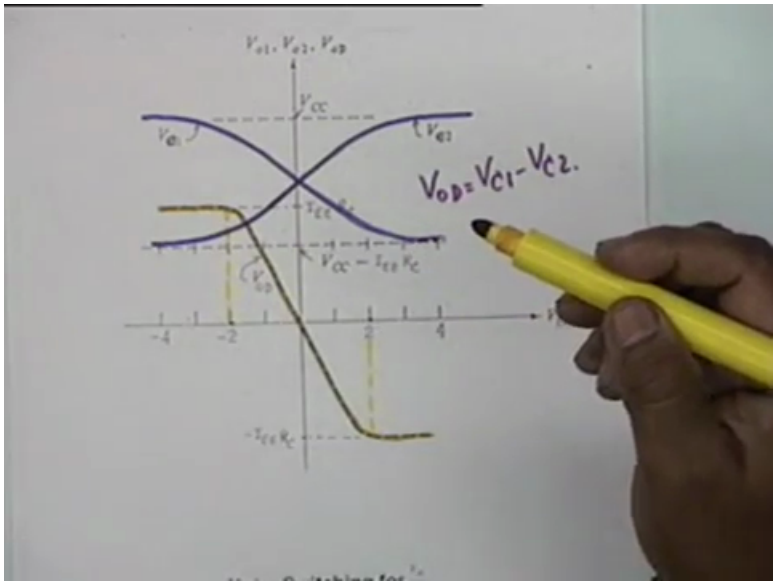

And I also left some algebraic steps to you to show by substituting the expressions for I sub C 1 and I sub C 2 that the voltage V O D is given by this relationship, minus I E E, R C tan hyperbolic V D by 2 V T.

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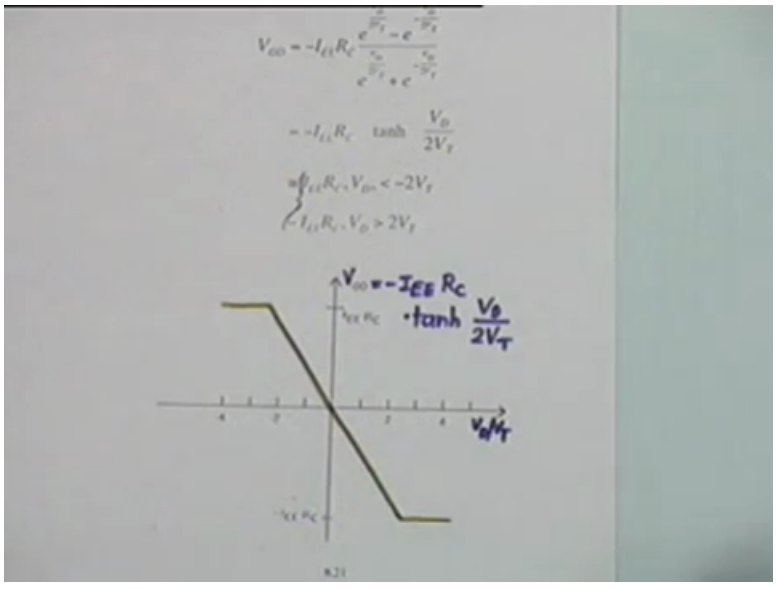

I will write this expression again and this is where we will start from today. V O D, the differential voltage is equal to minus I E E, R C. And you remember why minus comes because it is I C 2 minus I C 1 times R C. I E E, R C tan hyperbolic V D by 2 V T. Was there

any problem in deriving this relationship? Was there a problem or you did not derive? Please do.

If there is a problem let me know. Now the variation of V O D versus V D by V T is approximately linear as I have told you and these values are one is I sub E E, R sub C and the lower value is minus I sub E E, R sub C. Now comes the utility of the DC analysis. You see if I change V D a little bit, V D changes to let us say V D plus delta V D, then delta V D is the perturbation on the Q point on the operating point and therefore this corresponds to a signal, alright?

This corresponds to a signal capital V sub capital D. Under this condition V O D naturally shall change from V O D to delta V O D and this appears in response to an increment in change in the input voltage of V D and therefore this is capital V subscript small o subscript small d. This is the output signal and the ratio of these two V o d by V d shall give you the gain of the amplifier, alright?

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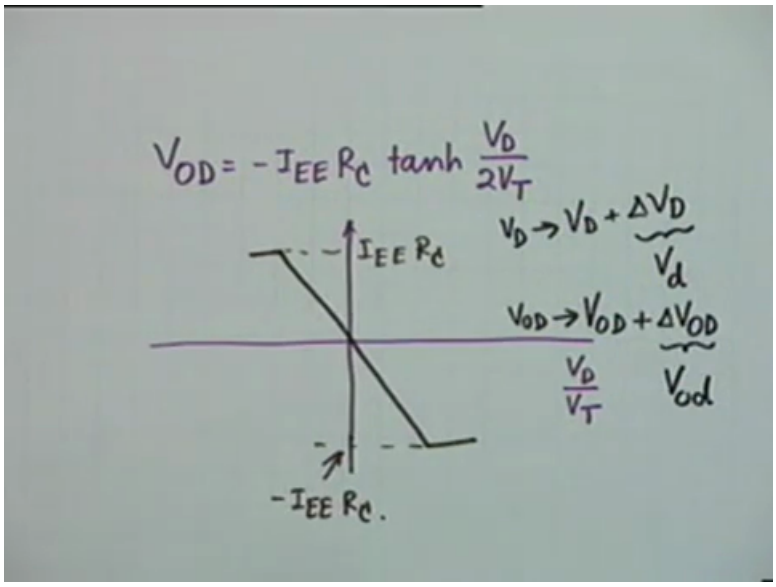

This is the advantage, this is the utility of the DC analysis and the DC analysis incidentally also showed what range you should be concerned with for linear amplification, okay. Now therefore the gain of the amplifier which is A d, the differential gain, would be equal to d V o d. I beg your pardon.

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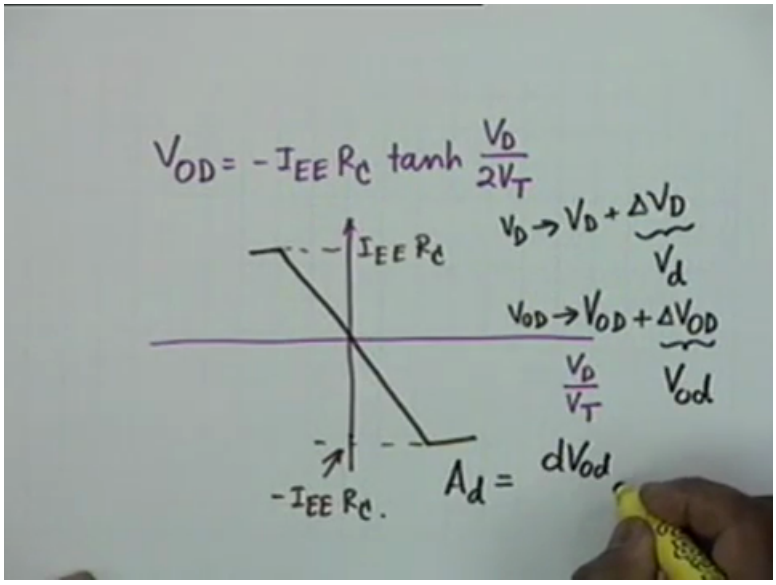

It would be d V O D that is the small change in the DC output due to a small change in the DC input, okay. This ratio shall give you the gain. You recall that this is the output signal and this is the input signal V sub d, okay. And therefore if we differentiate this relationship I should be able to get a gain that is if I differentiate V O D with respect to V d what do I get?

I get I sub E E minus R C tan hyperbolic differentiation gives sec hyperbolic squared, okay. Now sec hyperbolic squared of V D by 2 V T and then this has to be differentiated with respect to V D so 2 V T shall come here, agreed?

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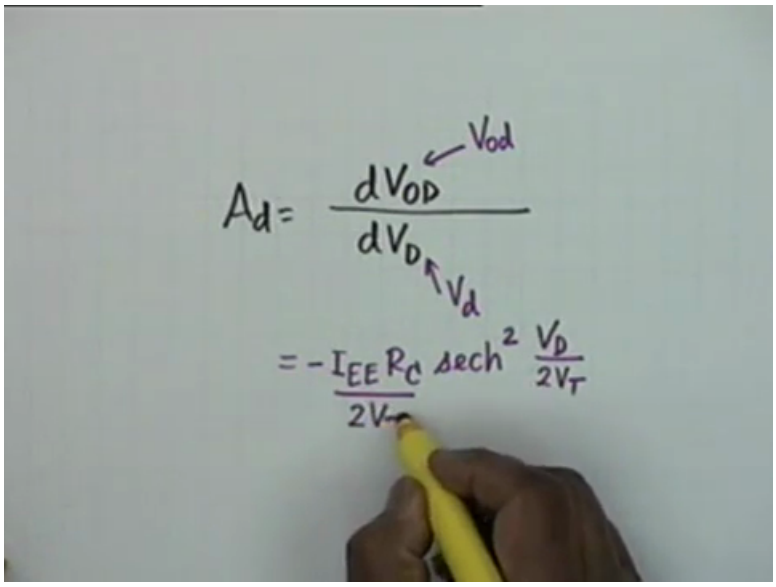

This shall be the gain. Now you notice that the gain is a function of the Q point. The gain is the function of where your V D is that is the DC value V B E 1 minus V B E 2 or V B 1 minus V B 2. However since the curve is approximately linear in this range we can simplify

the gain calculation by taking V D equal to zero. That is obviously the curve will be maximally linear at this point. As you go out from zero either on this side or this side, the curve starts bending and therefore we find the gain at V D equal to zero.

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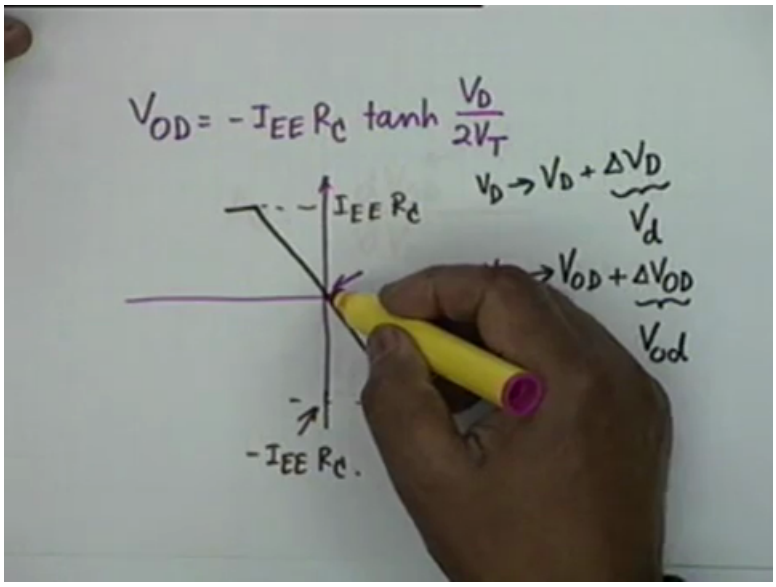

If I put V D equal to zero, sec hyperbolic of zero is unity and therefore A sub d becomes simply equal to minus I E E, R sub C divided by twice V T. This is the gain and the gain has been derived not from the AC equivalent circuit, it just have been derived from simply DC calculations and our purpose was to establish not only the gain but also the range of operation that is what is the dynamic range permitted for the input? If we exceed twice V T about 50 millivolt then we shall not get linear amplification.

So the input signal (())(09:54) must be limited to minus 2 V T to plus 2 V T. That is the total peak to peak swing of 4 times V T approximately 100 millivolt that is it. And which is true for approximately all BJT amplifiers at room temperature. What happens with FET we shall see later. But this expression also is very illuminating. Minus I E E, R sub C divided by twice V T. If we call this circuit after differential amplifier, I sub E E is I E 1 plus I E 2, the two emitter currents and beta was assumed to be very large.

The emitter currents are approximately equal to the collector currents therefore this is twice I sub C, I C 1 and I C 2. They are identically (())(10:53) so there is no reason why the current should be different.

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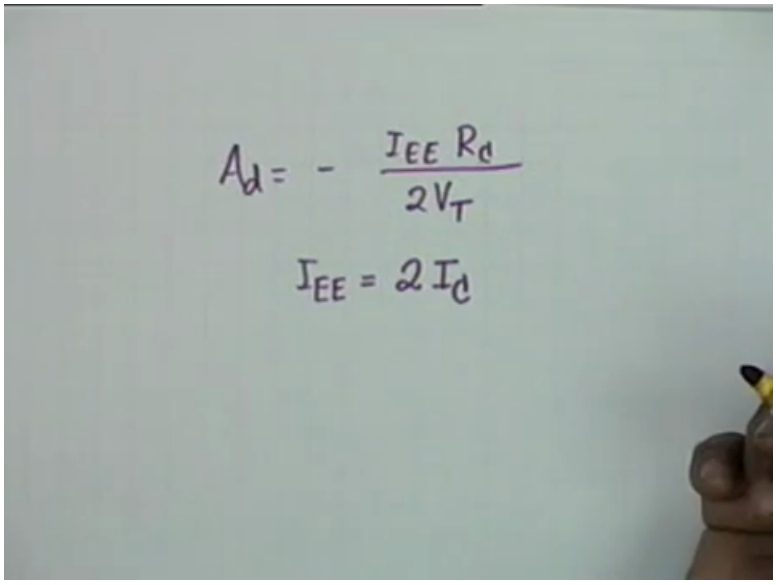

And if I substitute this then I get A d equal to minus I sub C, R sub C divided by V T and we also remember what is I C by V T, g m. So it is minus g m R C which is a very familiar expression. This is the gain of a simple common emitter amplifier with a load of R sub C. If there is another load capacitively coupled there is no capacitive coupling here. So this is the load and therefore by using two transistors in this emitter coupling mode we have not gained much in terms of gain, is that correct? The gain is still minus g m R C.

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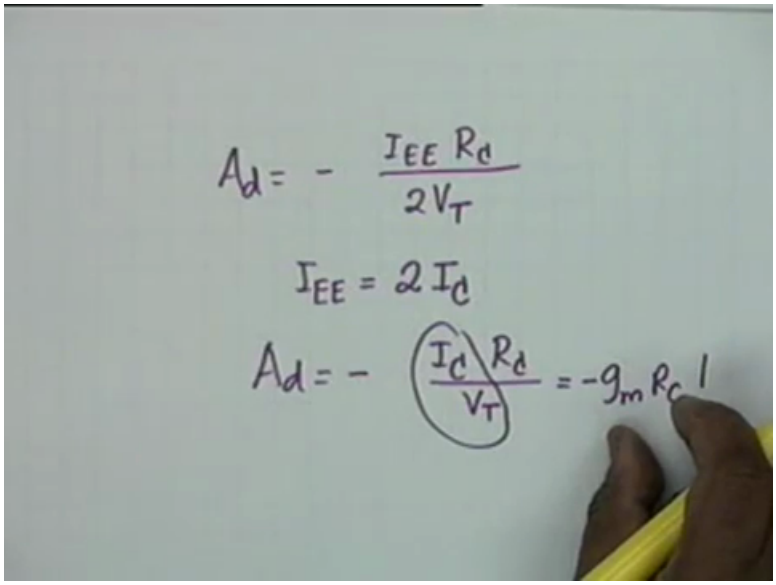

I could have obtained the single BJT instead of two. What is it that you have gained? We have not gained in terms of gain, we must have gained somewhere else. What we have gained is the following fact that V O D equal to zero when V D equal to zero. What does this mean? It

means that when there is no signal, there is no voltage difference between the two collectors which means that the DC offset is zero.

That means if the two bases are at identical voltages, the two collectors shall have identical voltages and these collectors now if you recall these are our output points and there is no reason why these two cannot be applied to the next stage of differential amplifier.

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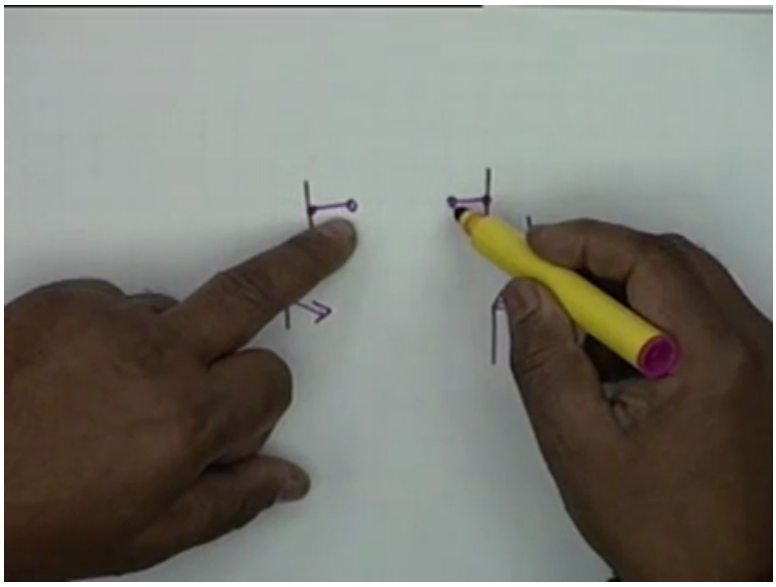

That is I have next stage of the differential amplifier without any DC offset. That is this will not create a signal at the input of the differential amplifier, is that clear? The input to the next differential amplifier will arise only when there is a signal. When there is no signal there will be no DC offset here. In other words V O D shall be equal to zero. This is the major advantage, okay. And we can cascade in number of them to get any gain that we want.

On the other hand if you are in a single stage (())(13:43) amplifier and we want to increase the gain by using cascading we require capacitive coupling. Otherwise the DC will affect the next stage, alright? Obviously V C E cannot be connected directly to the base because the next transistor will then be saturated, is the point clear?

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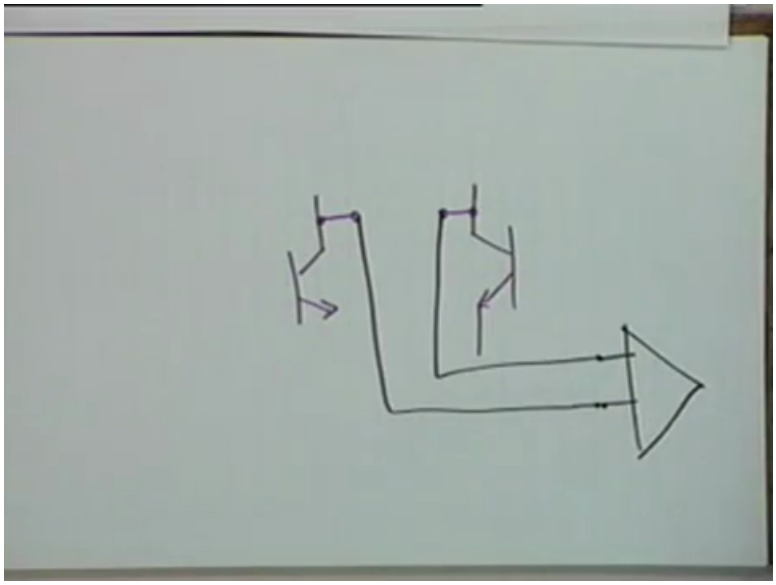

Student: Sir we also have noiseless amplification in this case?

We have yes, we have a signal to noise ratio S by N at output will be much greater than signal to noise ratio at input. I am coming to this advantage a little later when we calculate the C M R R. Okay now we go to the AC analysis, right? Let us see DC analysis is given as gain, is given as the range of operation. Let us see what AC analysis gives. Now in AC analysis we first make analysis for differential mode. For a differential mode what we apply is a differential voltage V sub d.

This is the AC quantity now, capital V subscript small d, AC quantity and we are taking the RMS values. What we do is we apply a differential signal between the two. Now since the two transistors are operated under identical conditions I can look up on this as if I had applied V d by 2 here from the base to the ground and another V d by 2 here from the base to ground but with a reversed polarity that is plus here and minus here, is that clear?

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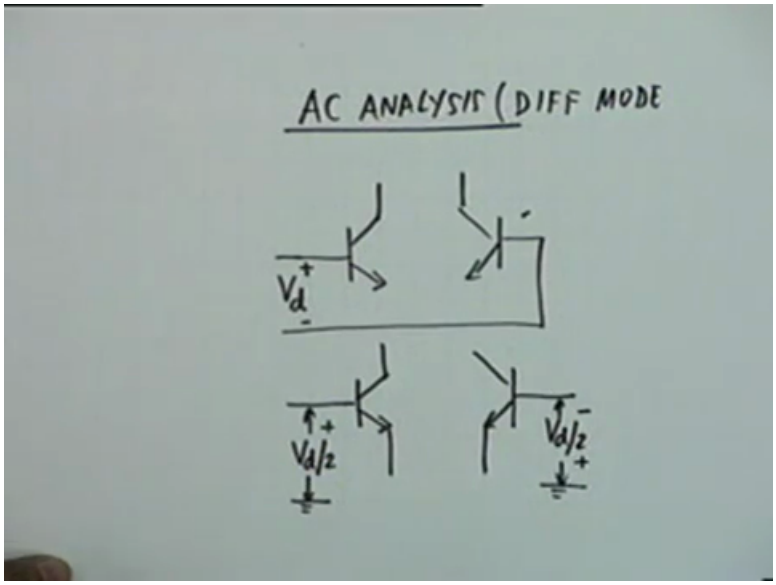

This facilitates the analysis so this is what I shall use that is we apply a differential voltage between the two bases and we look up on this as if equal and opposite voltages are applied to the two bases. This is what is done in practice. In fact one of them will be grounded and the voltage will be applied here. What counts for the differential amplifier is the difference voltage at the input not the absolute voltage. So if this is at zero then this is at V d, if this is at minus V d by 2 then this is plus V d by 2. So that the difference is still V d, okay.

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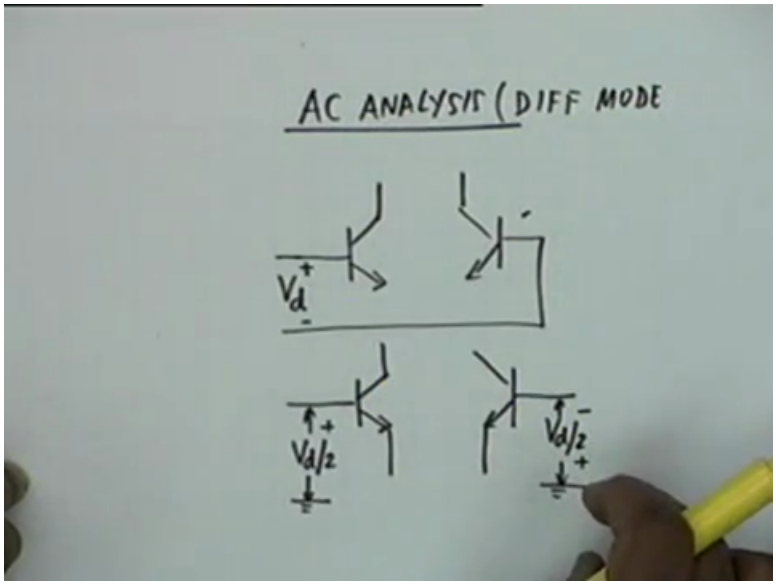

Let us look at the equivalent circuit. If I do that then let me view the signal also. Instead of V s let me view this as V s by 2 with this polarity and V s by 2 with this polarity plus, minus, okay, so that the total voltage applied is V s, the difference voltage. Now V d will be created

by V s by 2, in series we get R s. They are identically is only for the purpose of analysis. We in the actual design we will apply the signal only at one terminal, okay.

We may apply to two terminals also but one terminal suffices. So this voltage is V d by 2 and this voltage is V d by 2 in the opposite polarity plus, minus. This is my base 1 and this is my base 2.

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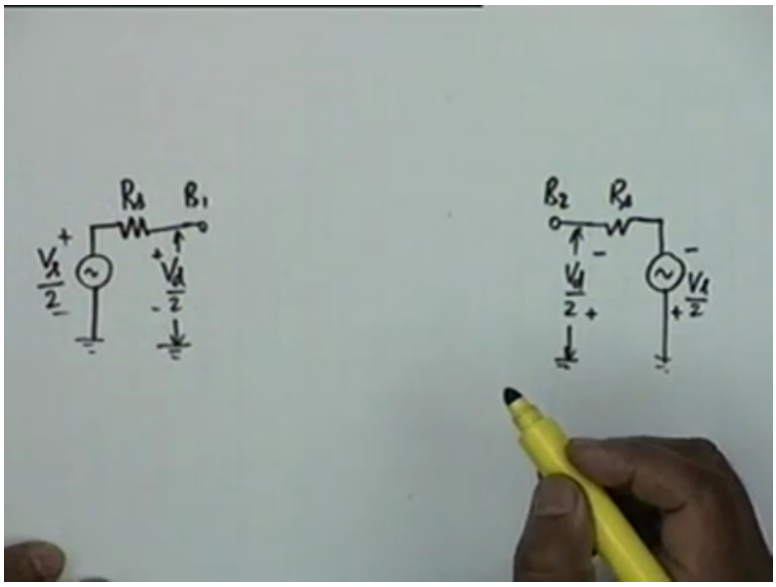

From base 1 if you look at the equivalent circuit we have an r pie 1. Base 1 to emitter is r pie 1 and base 2 to emitter is r pie 2 and the two voltages they are V pie 1 and V pie 2. I will run short of space, V pie 2, okay. Then the two emitters are connected together. This is E 1 E 2. E 1 and this is E 2.

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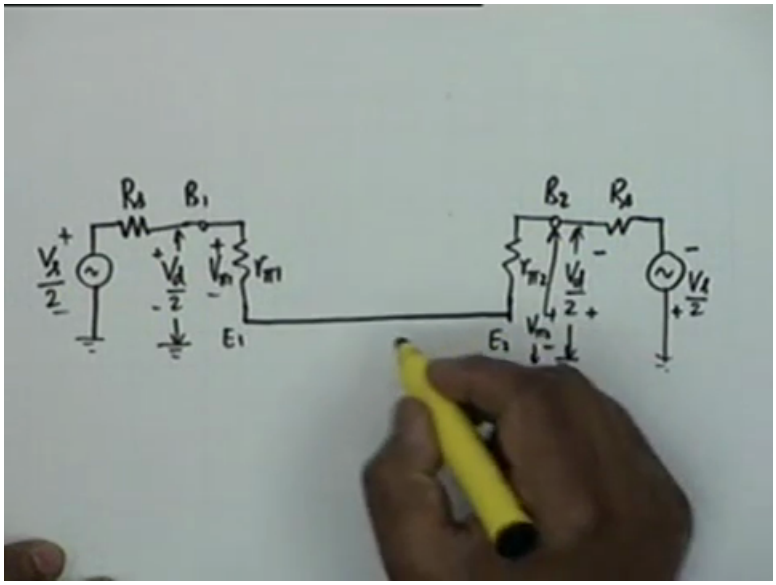

They are connected together and from this common point we get an R E E. As far as AC is concerned, V E E is ground, okay. Now in the collector circuit we had a g m V pie 1. This is collector C 1 and there is a collector C 2. We are ignoring everything else. G m V pie 2, if you wish you can say g m 1, g m 2 but they are identical because I sub Cs are identical. G m V pie 2 and then what do we have?

From collector to V C C there is a resistance of R sub C and from collector 2 to V C C there is another resistance R sub C and these two are connected to ground. You notice that we had ignored r zero, is not it right? Small r zero, it should have come in parallel to C 1 and C 2, R 0 1 and R 0 2 both would be identical because the collector currents are identical, the voltages will be identical because they are made on the same chip. However as we shall see later although we have ignored it, it could be taken into account by a very small trick.

And before I explain this trick let us notice that the AC current that flows here, let us call this I. What should I have the symbol? Small e 1, the current that goes here must be equal and opposite to the current that comes here because the two signals are equal and opposite and therefore I e 2 would be equal to minus I e 1. I e 2 would be equal to minus I e 1 because of symmetry and because of polarity excitation and therefore what virtually happens is I e 1 comes here and goes away like this, okay.

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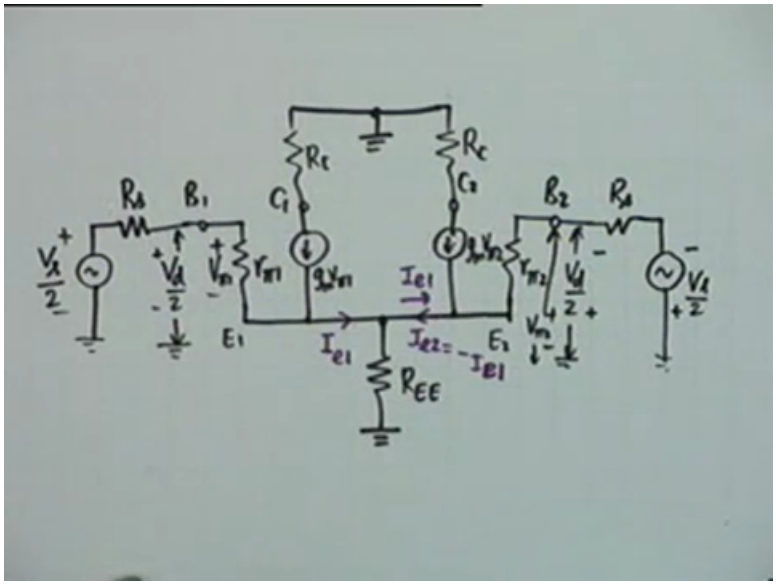

I e 1 comes here and goes away like this. No current flows through R E E which means that this point is virtually ground. This point is grounded and if that is so then the equivalent circuits simplifies greatly.

Student: Sir should not this point be open sir?

Which one?

Student: This point sir which you have (())(21:44)

The potential is zero because.

Student: (())(21:49).

Okay. This point, no current flows to R E E. So what is the potential of this point?

Student: Zero.

Zero that is really ground.

Student: But it is not necessarily zero sir. (())(22:10)

AC signal here is zero, AC voltage here is zero because no AC flows through R E E and therefore the potential is zero.

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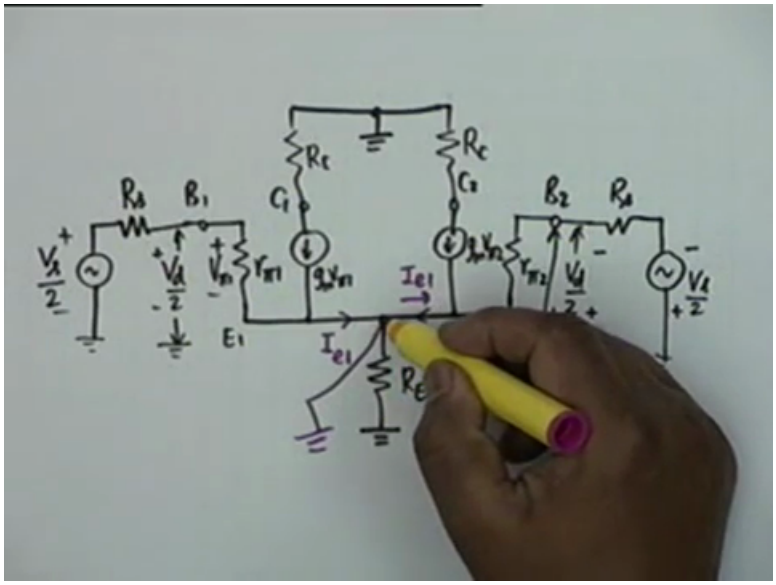

Student: So then V s by 2 is equal to V pie.

V s by 2 is equal to V pie. That is why V d by 2 will be equal to V pie 1. V d by 2 will be equal to V pie 1, V d by 2 here would be minus V pie 2. Yes?

Student: Sir, do we need an R s there?

We need an R s yes.

Student: Sir because we are applying signal at only one base and you said the other base is grounded.

This is the way of looking into a single voltage applied between the two bases. As I said we composed the single voltage into two voltages.

Student: So that means the resistance (())(23:06)

This is only a conceptual simplicity. We assume that identical sources with identical (()) (23:14).

Student: That means the resistance also and source also you (())(23:18).

That is it. When you bring the source you must bring its resistance also. That we have broken at the voltage into two parts V s by 2 and minus V s by 2, okay. Now if this point is grounded then you notice two very interesting things that R 0 1 was to come in parallel with g m V pie

1 and R 0 1 can therefore now be combined with R C, is that clear? And therefore there is no problem. You can combine R C with R 0 1.

And therefore (())(23:53) equivalent circuit all that we are retaining is r pie, R 0 and g m, nothing else. R s and R b are being ignored. Of course this is midband equivalent circuit. At high frequencies things will be different, okay. And there is no more frequency cutter because the amplifier is direct coupled. It is not coupled through a capacitance, okay.

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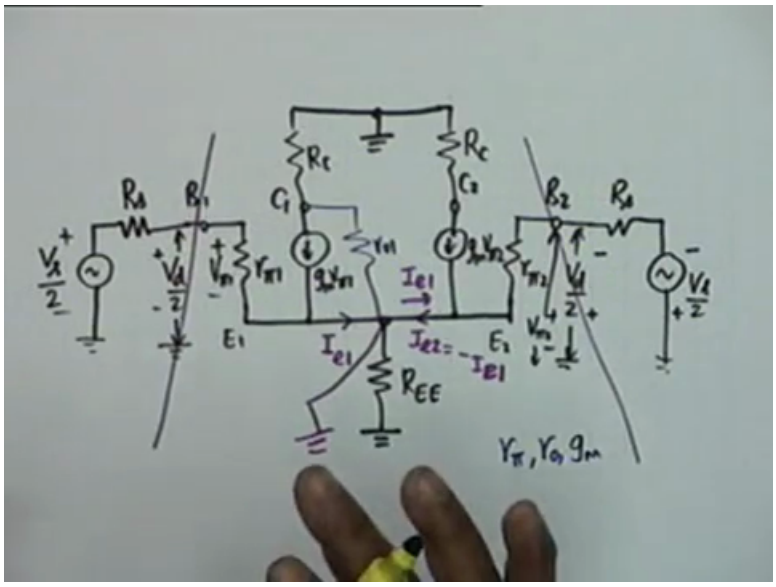

Now we can calculate the gain very simply. I can decouple this ground. I can only consider half of the circuit and this is called the half symmetry analysis. So what we do is we have an R s. We just take one of the transistors V s by 2 and then we have r pie 1 which now goes to ground. This is V pie 1 which is equal to V d by 2 with this polarity. Then we have g m V pie 1, 1 and 2 are the same.

This goes to ground and all I have is an R sub C to ground and I have said it could be R C parallel R 0 1, okay. And this is my voltage capital V o d divided by 2 with this polarity. From the collector to ground the voltage is V o d by 2. This voltage would be V o d by 2 and this voltage would be minus V o d by symmetry, okay.

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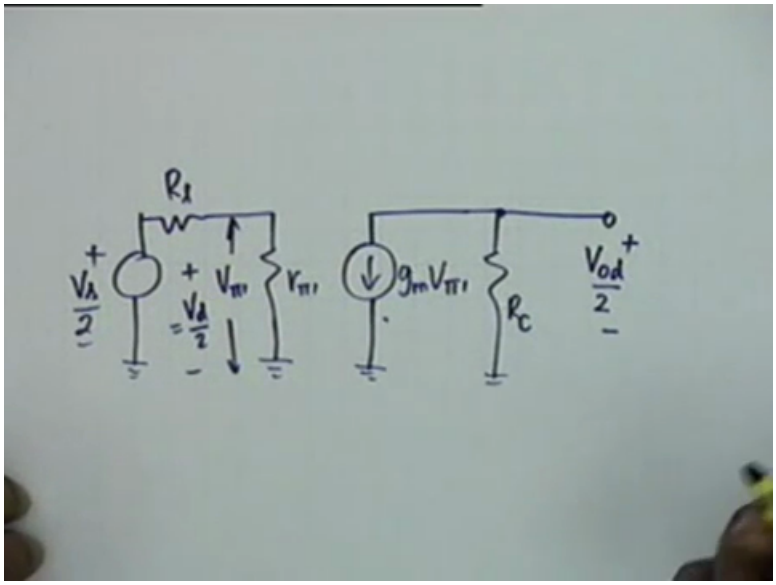

So what is the gain A sub d? It is V o d by 2 divided by V d by 2 and obviously this is equal to minus g m R C. The same result that we have derived from DC analysis, okay, the same result. We do not expect anything different. If it is different then we would have suspected our DC analysis. But it also shows two things that the output is an unbalanced output.

We have taken from the collector to ground, is that clear? We have taken an unbalanced output. The input is balanced the output is unbalanced. So it is a balanced to unbalanced transformer, okay. And the second thing it shows. Yes?

Student: Sir even in r 0 also.

I could take R 0 also. If you desire you call it R C 1.

Student: Sir in that case the DC analysis and AC analysis results could be different.

That is correct, okay. If R 0 is not taken into account in the case of DC analysis then they are slightly different. But R C in practice is very small compared to R 0 therefore for an engineer they are equal, okay. The other thing that you see is if the output is taken from here what is the output resistance R 0? It is simply equal to R C. What is the input resistance? Input resistance is the resistance in here. That is not correct, okay.

This point is a virtual ground so from here from B 1 to B 2 remember the voltage is applied between the two bases. So what will be signal source here? R pie 1 plus r pie 2. This is the input resistance of a differential amplifier. It is not r pie 1. It is r pie 1 plus r pie 2. It goes like

this, okay. And the source is the single source. Sorry. So the input resistance in one stroke of pen I can write this as twice r pie. Excuse me.

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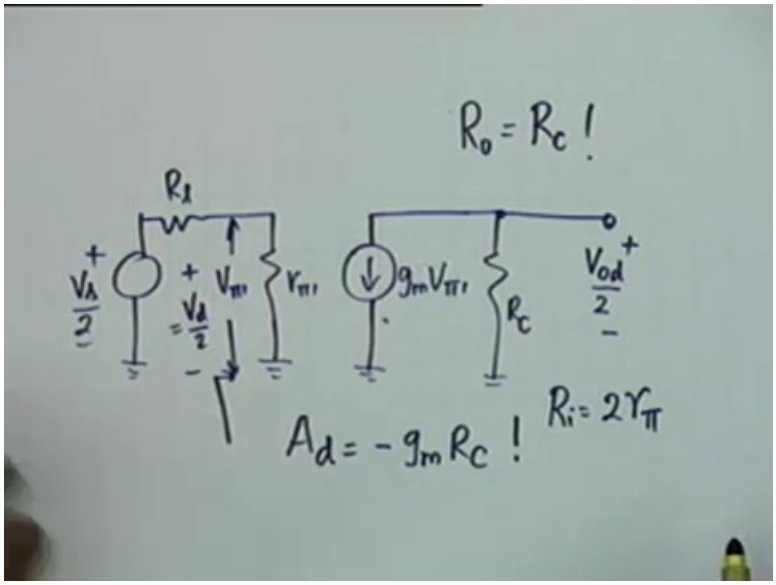

I have computed the gain, I have computed the output resistance, input resistance. Now let us look at the common mould gain.

Student: Sir, please explain again how do you get 2 r pie?

The input that we apply is between the two bases, okay. It is the different matter that one of the bases may be grounded. If it is grounded then it is between B 1 and even if it is grounded it is B 1 and B 2. From B 1 to B 2 the path is r pie 1 plus r pie 2.

Student: So in that case even the output is not taken .

Output is not taken in the differential mode, no. Output is taken across one of them because we want the output to be grounded, alright? If we want to enhance the gain then we take the differential output and connect to the two bases of the next stage. That if this is the final stage we take the output from one of the connectors to ground, okay.

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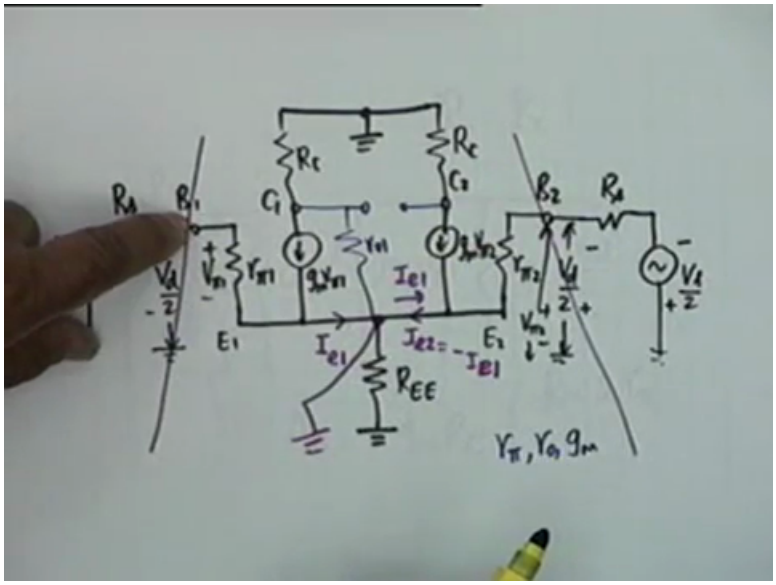

Now let us go to the common mode gain. In common mode, yes?

Student: Sir, using the DC analysis we have considered the output as a differential output and here we are considering it as the unbalanced output.

Right, we also split the voltage. The voltage was V d by 2 and (())(29:46) V o d by 2. So it is factor of two which derives both numerator and denominator. The gain still remains the same, okay. In common mode analysis our circuit would be V s and an R s. The same voltage is applied to the other base B 1 and B 2, okay.

In common mode analysis and we call this voltage as small v sub c and this voltage as small v sub c. The polarity shall be identical common mode. Same voltage is applied to the two bases. The differential output shall be zero. But let us see if there is an output at the collectors.

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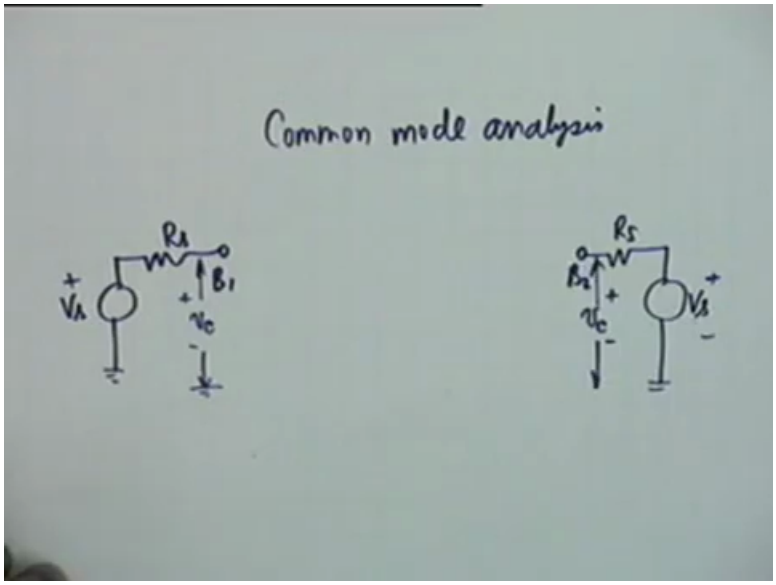

Now the equivalent circuit shall go the same way that is we have an r pie 1 and this voltage is V pie 1, then and r pie 2, this voltage is V pie 2. It will become a bit congested but I hope you can make it. This is V pie 2. The two emitters are connected together and connected to ground through R E E. There is a g m V pie 1 here, current source. This is collector 1. There is a current source here, g m V pie 2, collector 2. And the same story that is R sub C and R sub C these two connect together and are connected to ground, alright?

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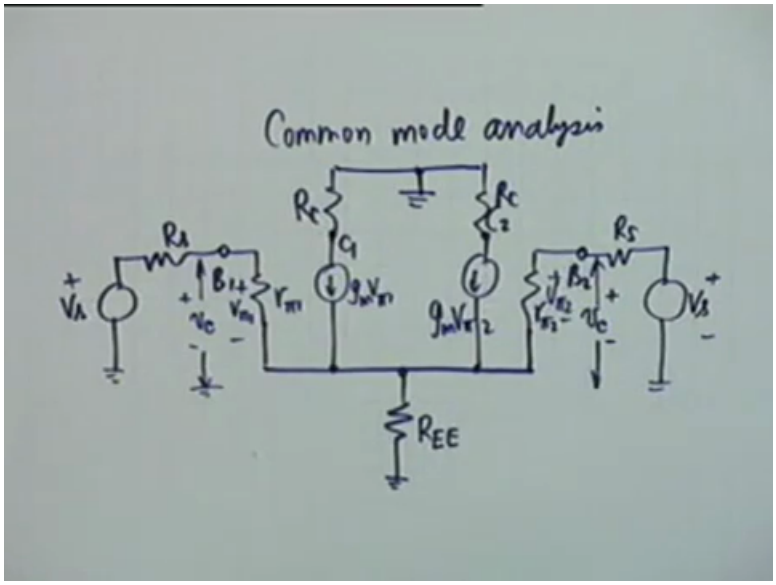

The only thing that we have changed is the sub sources are identical in the two sides and therefore the bass voltages are identical V c and V c. We want to see if there is an output from here to ground. Let us call this output as capital V small o small c, V o c output due to

common mode, okay, with this polarity plus minus. Agreed? Now because of symmetry this current and this current shall be identical. Is not it right? These two currents will be identical now.

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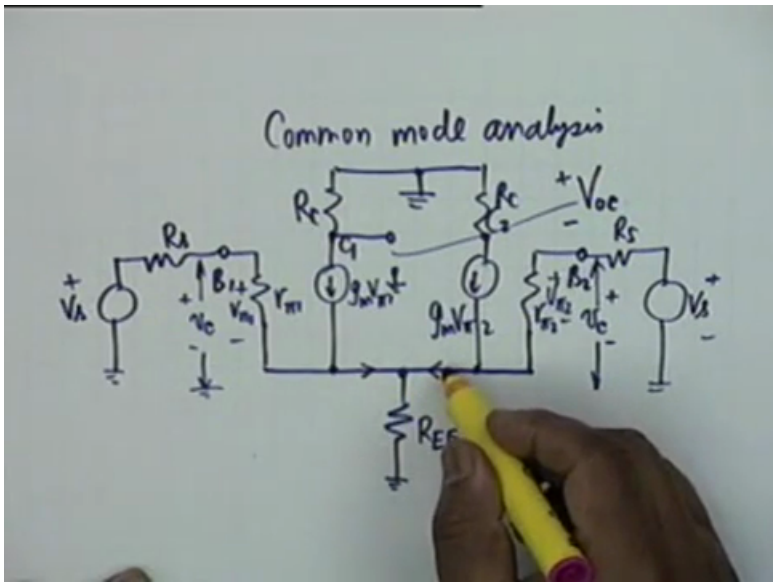

It is not equal and opposite to each other as in the differential mode which means that if this current is I e 1 then this current will be I e 1 plus I e 2 which are identical and therefore this will be twice I e 1 or I e 2. Yes?

Student: Are not these two amplifiers two common emitter amplifiers (())(33:13)?

No, that is a mistake. They are emitter coupled. When two amplifiers are cascaded together the emitters are not common, not necessarily common. Here we have taken to connect the resistance here. There is a great a difference. If they are two common emitters then all these advantages would have been lost and you have to have coupling capacitors and many other things.

Signal to noise ratio would not have been improved. Now the point that I want to mention is as far as transistor 1 is concerned it sees in R E E twice the current that comes here which means that the drop that it sees here is twice I e 1 R E E. So as far is transistor 1 is concerned it is as if it sees instead of the resistance R E E it sees a resistance of twice R E E. And that simplifies the circuit if I draw the circuit once more. V s, R s, this is capital V subscript small C. I have made a mistake here, this is capital V.

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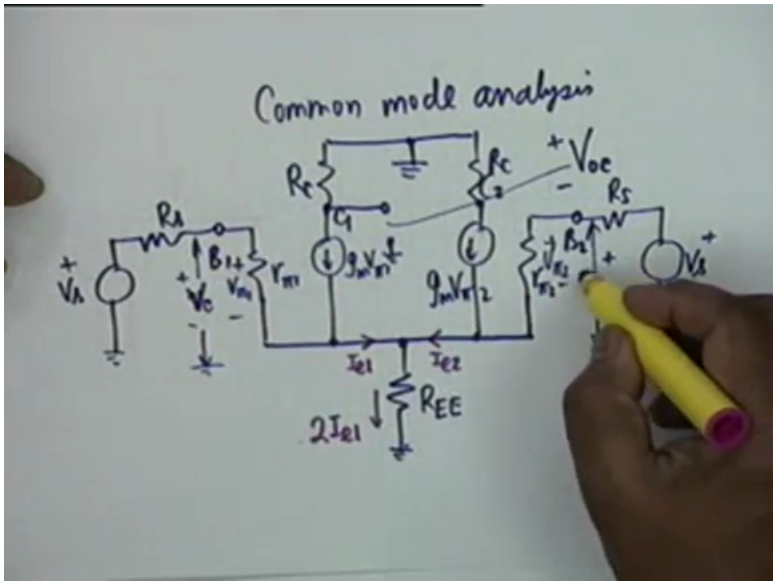

The signal quantity, RMS quantity, subscript is small c, V sub c. Then we have an r pie 1, V pie 1 and instead of R E E we have twice R E E. Then we have g m V pie 1 coming here and I have R sub C, the collector resistance and this voltage is V O C plus minus. If you recall we have analysed this circuit earlier. This is the common emitter circuit with bypass emitter resistance and therefore we did not repeat the analysis. We can write the gain very simply. A sub C, the common mode gain which is the ratio of V O C to V c.

Same way we have taken earlier also V o d divided by V d by 2, the output voltage divided by the input voltage is given by minus g m R C. We did this earlier and if you desire you can carry this out again. It would be 1 plus twice R E E beta plus 1 divided r pie. This is the gain.

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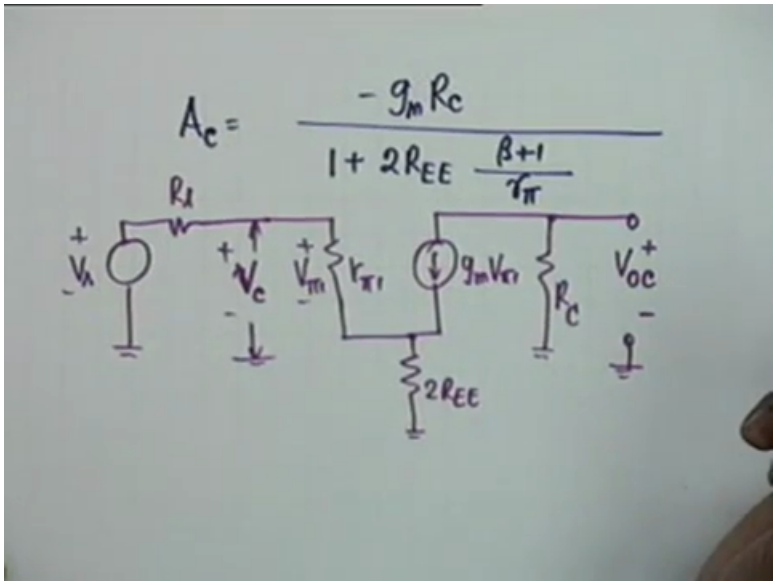

And if beta is much greater than 1 as have been assumed earlier this is simply beta by r pie and therefore g m and therefore this is approximately equal to minus g m R C divided by 1 plus twice g m R E E and initially twice g m R E E is much greater than 1 so the gain is simply minus R C divided by twice R E E. In condolence with what we have found out earlier. That in case of bypass emitter resistance the gain is controlled by the collector resistance and the emitter resistance.

It is only the ratio of the two, okay. Now let us keep it like this. Then one thing is also obvious that the output resistance here, what is the output resistance? It is the range R sub C. Why? Because this is where there is a current generated here, okay. R 0 is again R sub C as in the differential mode but there occurs a change in R i. What is the input resistance? R pie 1 plus beta plus 1 twice R E E.

So in the differential mode because simply twice r pie. In the common mode the large resistance is added to r pie. So the common mode the input resistance is high, alright? Yes.

Student: In re coupling output resistance how did you get the output resistance with R C?

Okay, if V s is termed zero then V pie 1 will also be zero, no.

Student: Some of the current may flow through it.

Okay, we did calculated this earlier, is not it? G m V pie 1, 2 R E E is parallel with r pie 1 and R s, okay. Alright, this is R C, V and I. The question is good. I do not know the end but the answer would be good. This comes to twice R E E, then what? From twice R E E you have an r pie 1 plus R s. Oh! I made a mistake. It is r pie 1 plus R s. I must write V pie 1. V pie 1 would be minus here and plus here.

Student: Sir the opposite, minus plus.

Yes that is correct, minus plus.

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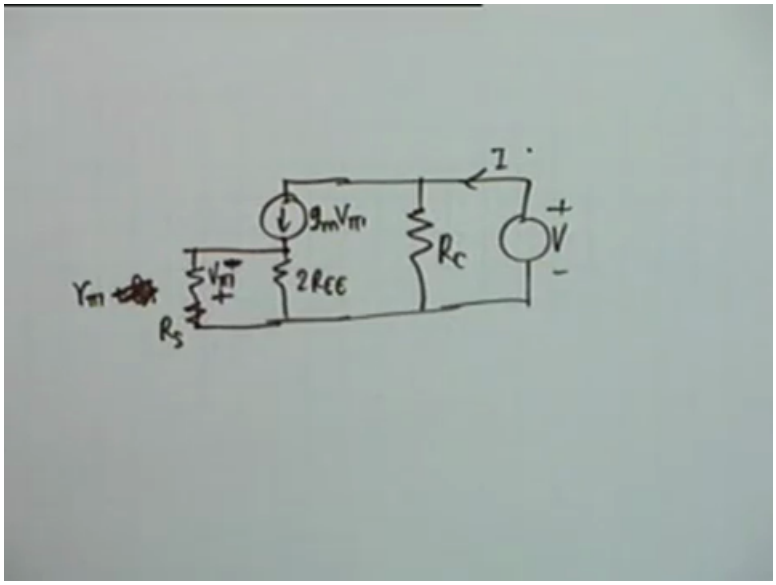

Now the question is this current can you (())(39:44) a component here? Yes? Can this current flow here? What is the input impeding? What is the impedance at current generated? And there is no source on the left hand side.

Student: Sir how can you say that?

How can you say that, okay. I leave this to you to sort it out. You assume a voltage here and you need to write two node equations, okay, and find out what the result is and let me know in the problem session, okay, alright. Have we calculated the input resistance? Yes, input resistance we have calculated. Now I go back to my two gains. A d is minus g m R C and A c, the common mode gain is minus g m R C divided by 1 plus twice g m R E E, okay.

Therefore the C M R R is a positive quantity. It is A d by A c and this is equal to 1 plus twice g m R E E. Agreed? Which is approximately equal to twice g m R E E. What is g m? G m is twice I C divided by V T, R E E. Okay, and what is twice I C? It is equal to I E E R E E divided by V T.

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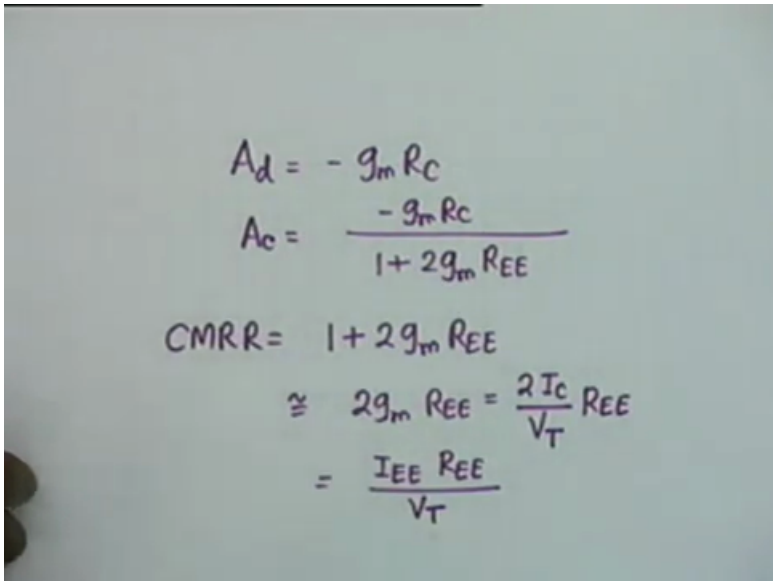

Now, our purpose in a differential mode amplifier is to make this signal to noise ratio at output as large as possible. Is there any question on this? To make the signal to noise ratio at the output as large as possible we wanted A sub c to be equal to zero and we wanted A sub d to be as large as possible. In other words we want to increase C M R R to as large a value as possible. It depends on an internal property of the transistor that is (())(42:19) which is an universal constant V T which you cannot change.

You cannot lower this down. V T cannot be changed. What you can change is you can change I E E. You can use a large current or you can use a large resistance or you can use large current as well as large resistance. In either of the two cases the casualty becomes V E E. It has to be increased. If you increase I E E, how do we increase I E E? We increase the source voltage that is V E E. If you increase R E E then with the same current there is a large drop across R E E and therefore we have to increase V E E, okay.

This is not permissible. It is not feasible in an integrated circuit. What are the advantages of IC is that it can operate at low voltages. If you want to increase the voltages to high value not only you lose the advantage but you also run the risk of burning the chip because it cannot take more than a certain amount of dissipation.

Very small space heat cannot go out. Large current means large dissipation, alright, and therefore we remove that advantage. So we have to derive something to increase this factor I E E R E E. And what is done is to increase R E E by an indirect means that is replace R E E that lumped resistance by a current source.

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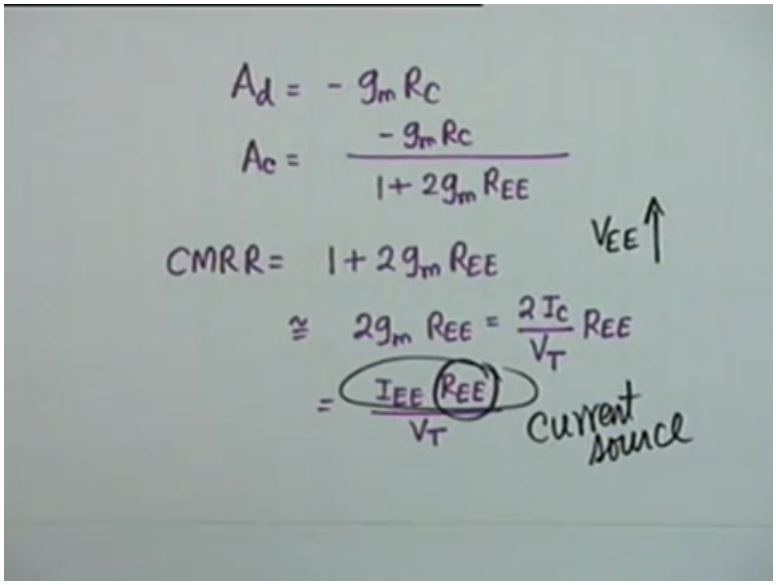

If I can replace R E E by a current source and if the current source is an ideal current source then R E E is approximately infinity and therefore C M R R can go to infinity and we have an ideal differential amplifier. That is the common mode gain would be equal to zero. That since nothing in this world is ideal and transistor circuits are no exception we have to settle with what we get. Let us see what we can get. That before I make an analysis let me show you how the current sources are connected, okay.

Let us draw the differential amplifier, plus V C C, then these two are connected together. This is where the question comes. We want to connect not R E E but the current source, okay. And then of course you have to show the base circuit, okay. Let us show. Suppose we have connected a V s and R s and perhaps nothing is connected here but truly a differential mode, okay. We have connected a voltage here. Nothing is connected, this is connected to ground.

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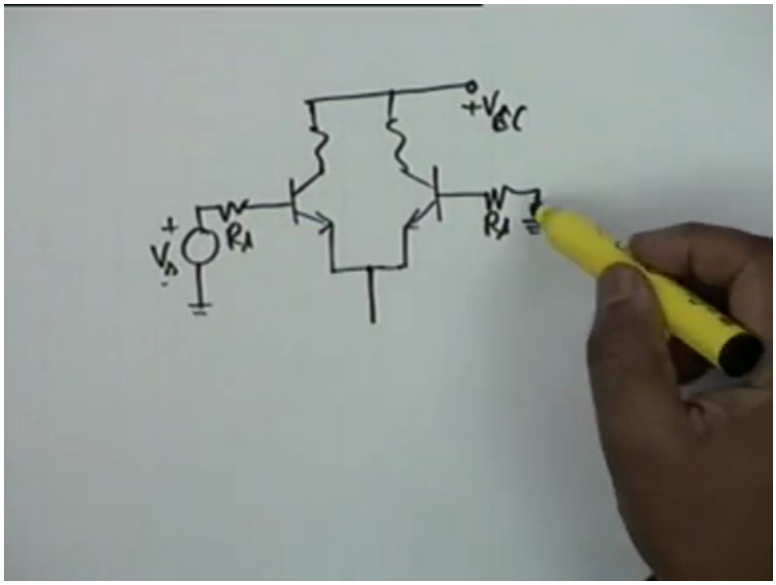

But I have connected to ground through a resistance R s. Can you guess why? Why could not I connect it directly to R s, directly to ground?

Student: For the cut off.

No, that is not.

Student: Preserve the symmetry.

Preserve the symmetry of biasing?

Student: Yes.

DC biasing that is why DC is concerned, V s is assured. Therefore this base is connected to R s, this base should also be connected to R s. Otherwise there shall be a DC offset. Is that clear? And any change in the DC voltages between the two bases shall be interpreted by this dump amplifier as a signal, is not it right? Any change in DC therefore I connect an R s here.

Now the point is I do not want to connect a resistance here, I want to connect a current source or a current mirror and you know what a current mirror looks like, okay. What you have to do is two transistors, the reference transistor has to have its collector connected to the base and these two emitters should come together if it is a simple current source.

But the current that we want here we want to control this current and therefore we use instead of a simple current source, what? (())(47:29) current source. So we include a resistance here, connect these two and this goes to either ground or to minus V E E, okay.

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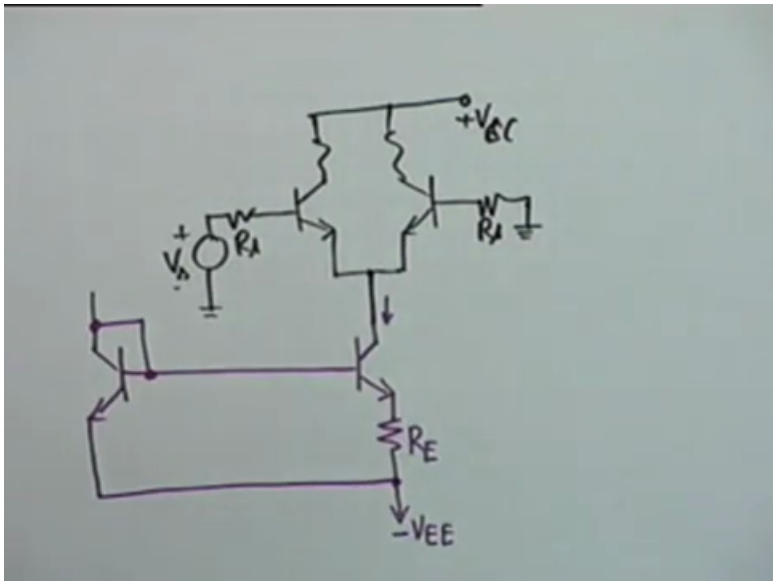

Instead of that R E E you see the complication. We have two transistors here and then I have to set up a reference current. How do I set this up? I had to have a resistance R here and this resistance is to be connected to plus V C C. So this is a differential amplifier R C, R C ,this is a differential amplifier with R E E replaced by a current source, alright?

Now let us look at this current source. You remember that I R, if I call this transistor as Q 2 and this transistor as Q 1, we had called this earlier let us call this Q 3 and Q 4, okay, since we are concentrating on the current source and its effect on R E E. The effective R E E that is offered by Q 1 and R E and the current source mode is the AC impedance looking from here. That is the output impedance of Q 1 in series with R E, okay. This is the effective R E E and we shall see that it can be increased tremendously.

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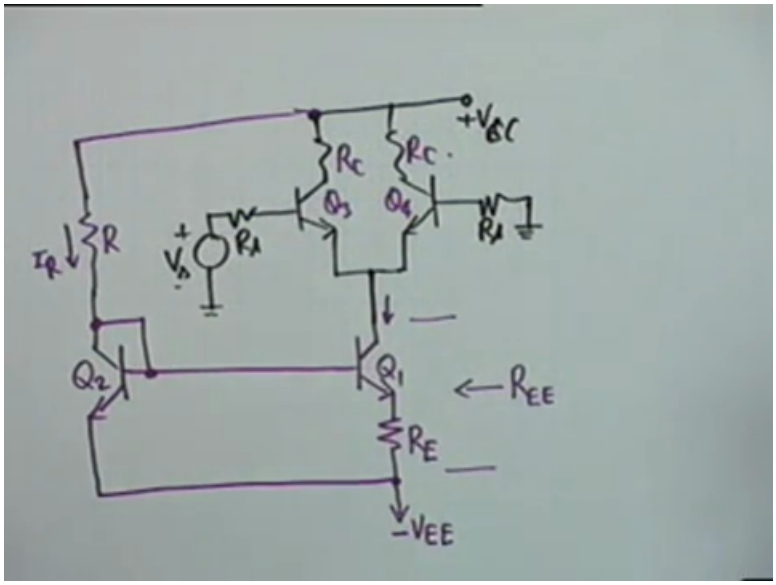

We have not increased V E E. We have kept V E E and V C C in the tolerable range. Effectively we want to increase R E E. If this transistor is ideal that is if its r 0 was infinity, if V sub a, the only voltage was infinite then obviously R E E would have been infinite, okay. But since there is an r 0 and V a is not infinity therefore R E E shall be a finite quantity but much larger than what we have physically connected here R E E.

We should show this that you recall the design equations of a (())(49:58) current source. I sub R is strictly equal to V C C minus V B E 2 which is point 7 divided by R and since these transistors are high beta transistors, I sub R is the same as I C 2 is the same as I C 1. Yes or no?

Student: Yes sir.

That was the purpose of including R E here that I C 1 can be made different from I C 2, okay. And they are related by an exponential relationship. What you do is V B E 2 is equal to V B E 1 plus I C 1 R E. From that we find out the relationship between I C 1 and I C 2. I shall repeat this relationship.

Student: There should be a plus V E E?

Plus V E E, no. V B E 2 from here to here is the same as V B E 1 plus I C 1 R E.

Student: Sir, the expression for I R.

Expression for I R, okay. That is right. Plus V E E, quite right, okay.

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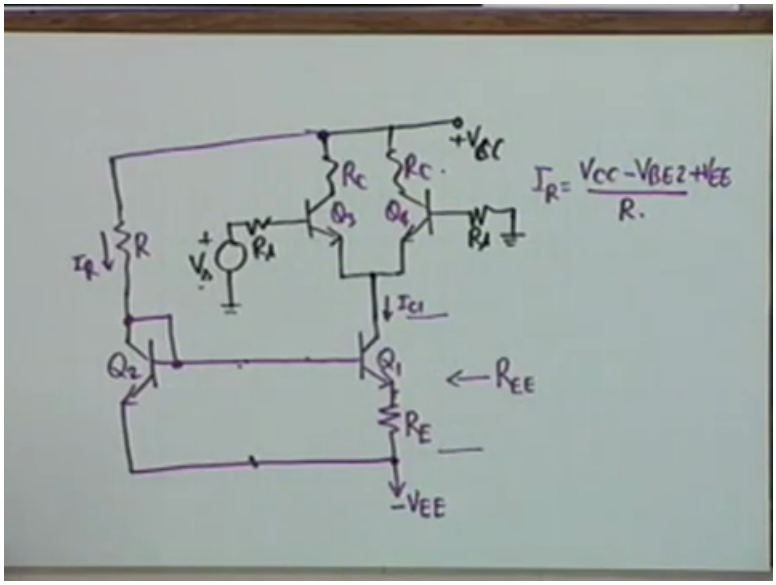

Now the equation that gives R E the required value of the resistance is the following. This is simply recalling it is V T divided by I C 1, the desired I C 1 multiplied by 1 plus beta inverse which you can replace by 1 times log of I C 2 divided by I C 1, alright? For example let us go here. I sub R equal to V C C plus V E E minus V B E 2 divided by R and R E the resistance required is V T divided by I C 1. Let us ignore beta. I C 1 log of I C 2 divided by I C 1 and I R is equal to I C 2 because of large beta.

Suppose I C 1 we require is 50 microamperes. This is a typical value because we want to keep the power dissipation as small as possible. Transistors usually are operated at very low currents. Suppose I C 1 is 50 microampere and R is 10 K. This value can be fabricated in IC technology. The highest resistance that can be fabricated is about 50 K. 50 is the limit. Do not go beyond 20. You will make the chip costlier because it will use more resistance. But 50 is approximately the limit.

If R is 10 K and V C C plus V E E is 15 volt let us say then I C 2 or I R becomes 15 minus point 7 divided by 10 K which is 1 point 43 milliampere and R E it calculates as 1 point 68 K which is indeed a low resistance, 1 point 68 K.

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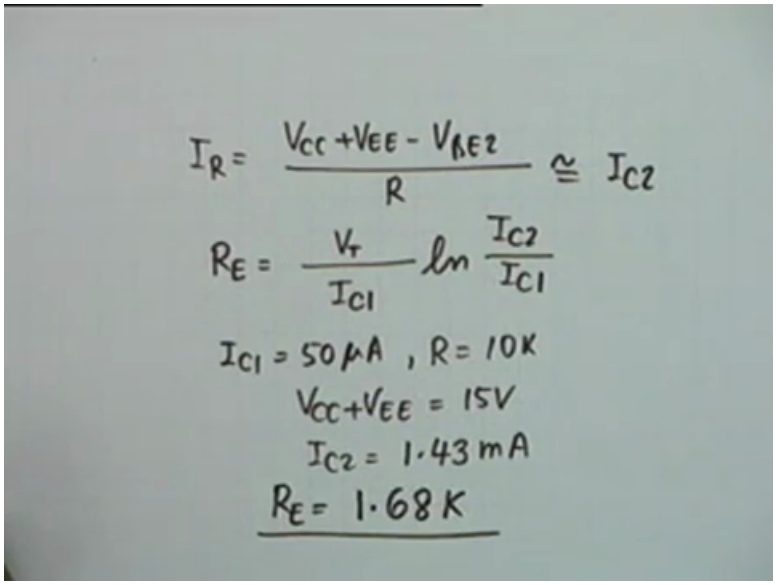

We shall show that with these values the effective R E E that can be generated is of the order of a (())(54:13). Even with R E E equal to 1 point 68 K, a small resistance, V C C plus V E E, the 2 combined there is no except 15 volts. The effective R E E generated is of the order of a (())(54:31), okay. Let us see how this comes about. In order to show this obviously what we have to do is to calculate the output resistance of this transistor when it is operated in the current source mode that is its V B E is controlled by a reference current and a reference transistor V B E.

We have to calculate the output impedance of this circuit. Let us take a simpler current source with V C C plus V E E lumped into one, alright. That will not a make a difference as far as output resistance is concerned because output resistance is AC. So we take the ordinary transistor. This is connected to the base and then we have this is I sub C 1, this is I R, this we will call Q 2 and this is Q 1. Then there is a resistance R E.

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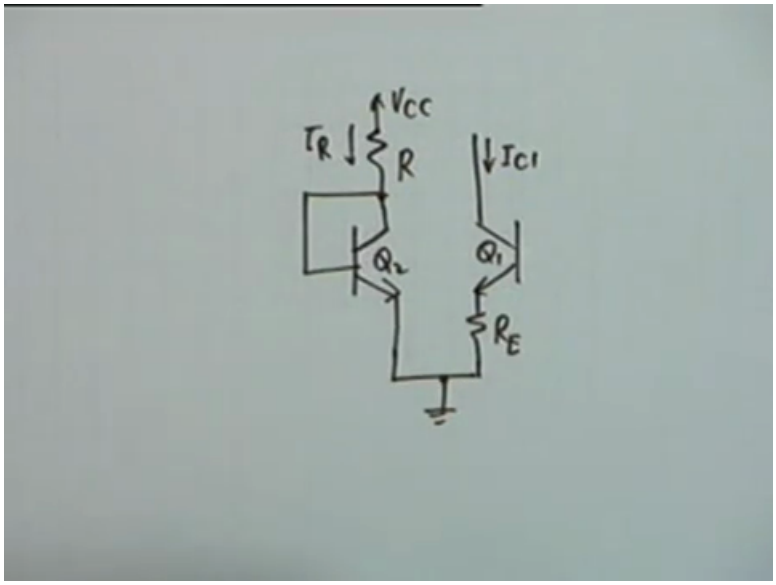

Now what we have to do now is to carefully draw its equivalent circuit and calculate what impedance is offered between this point and this point. Short the base. Yes, how could I draw it without short in the base?

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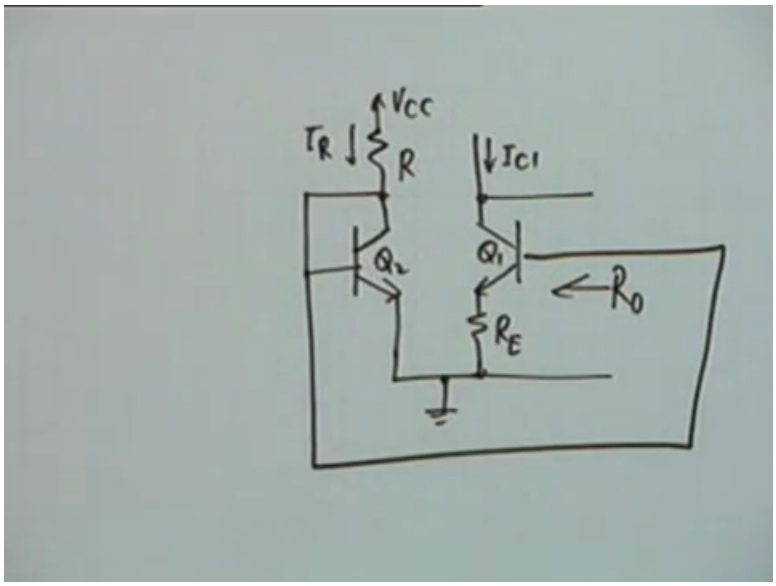

Actually I forgot the orientations so I had to draw this long line. So we need to draw the equivalent circuit and calculate the output resistance carefully which task we shall do next time.