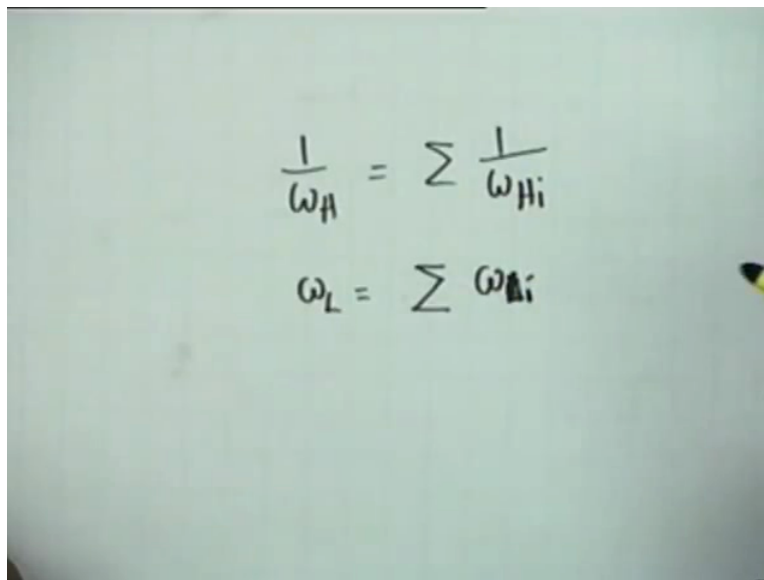


Analog Electronic Circuits
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Lecture no 20
Module no 01
Differential Amplifiers

We start our discussion on a different kind of amplifiers, so far we have talked about only single transistor amplifiers, we did work out 1 or 2 problems on multiple stages but this is the 1st serious discussion on multiple transistor circuits and the circuit is that of a differential amplifier. Before we take up this topic I wish to recall what we did last time, last time I said that in a multiple transistor circuit or even in a single transistor circuit where there are many capacitances, exact nodal analyses may be difficult, application of Miller effect may also be difficult and therefore the methods that are available are the methods of short-circuit time constants and open circuit time constants, open circuit time constants apply to high frequency gain and short-circuit time pass and apply to low frequency gains.

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$$\frac{1}{\omega_H} = \sum \frac{1}{\omega_{Hi}}$$
$$\omega_L = \sum \omega_{Li}$$

And if you have several Critical sequences Ω_{H1} , Ω_{H2} and so on then the overall high frequency critical frequency or the 3 dB cut-off frequency is given $\frac{1}{\Omega_H} = \frac{1}{\Omega_{Hi}}$, in other words the time constant and I have also sold you how to calculate the time constant it is the capacitance multiplied by resistance seen by the capacitance

in the Thevenin sense. This is for high frequency and for the low frequency the method of short-circuit time constant it is simply the submission of the individual $\Omega_{L i}$ individual cut-off frequencies.

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The image shows a handwritten equation on a whiteboard. The equation is:

$$A_{vA}(j\omega) \approx \frac{A_{vA0}}{\left[\left(1 - j \frac{\omega_{L1}}{\omega}\right) \left(1 - j \frac{\omega_{L2}}{\omega}\right) \dots \right.}$$

$$\left. \cdot \left(1 + j \frac{\omega}{\omega_{H1}}\right) \left(1 + j \frac{\omega}{\omega_{H2}}\right) \dots \right]}$$

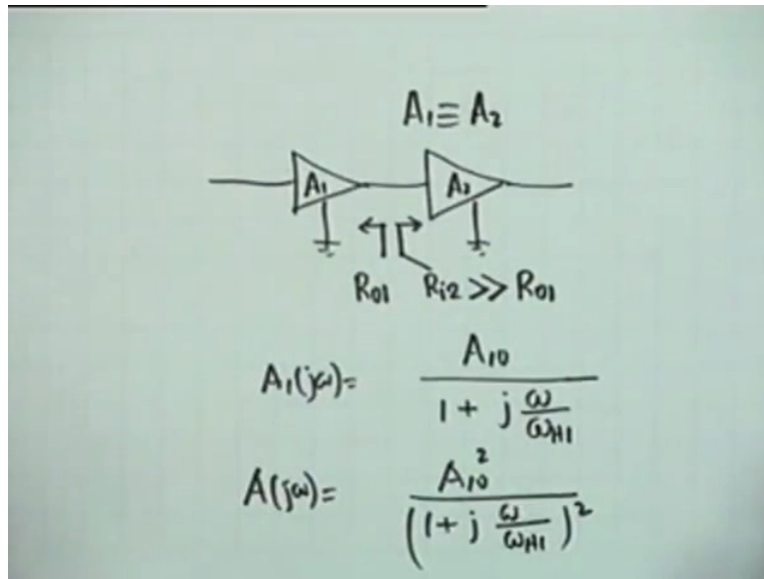
Below the main equation, there are two additional equations:

$$\frac{1}{\omega_H} = \sum \frac{1}{\omega_{Hi}}$$

$$\omega_L = \sum \omega_{Li}$$

In general therefore the transfer functions A vs $j\Omega$ is of the form A vs 0 the mid band gain divided by $1 - j\Omega L_1$ by Ω this is the low frequency critical frequency multiply by $1 - j\Omega L_2$ by Ω and so on multiplied by high frequency terms which will be of the form $1 + j\Omega$ by Ω_{H1} multiplied by $1 + j\Omega$ by Ω_{H2} and so on okay, this is the general expression for the gain of an amplifier containing many transistors, many capacitances and so on and so forth and this calculation is as I said approximate calculation based on the method of time constants. And this relationship that is $1/\Omega_H$ is the submission of $1/\Omega_{Hi}$ and the other relationship is Ω_L is submission of Ω_{Li} these are also approximate calculations. We would like to illustrate how approximate these are by taking 2 very simple examples.

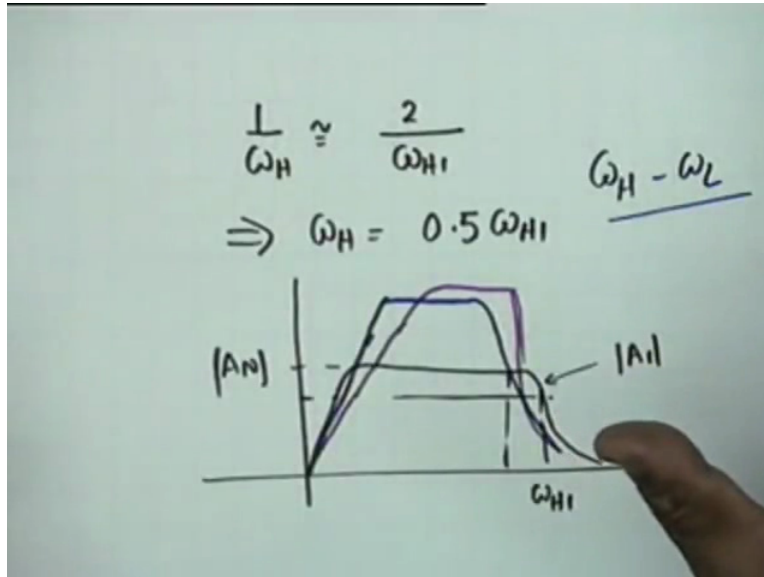
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We consider 2 amplifiers, this is the symbol for an amplifier you must have noted by now, 2 amplifiers which are identical let us say A_1 and A_2 ; A_1 is identical to A_2 , two identical amplifiers cascaded together in such a manner that the output impedance of the 1st stage R_{o1} is much lower compared to the input impedance of the 2nd stage okay so that whatever voltage appears across the output of A_1 does appear across the input of A_2 also okay, this is the condition for non-interacting stages that is A_2 does not affect the gain of A_1 , R_{i2} we assume that it is much greater than R_{o1} this is the condition to be satisfied, if it is not satisfied then what do we do? We put a buffer in between an emitter follower, which transforms a high impedance into a low impedance okay.

If that is so then A_1 of $j\omega$ is of the form A_{10} divided by let us say $1 + j\omega$ by ω_{H1} , if each amplifier at high frequencies can be described by such a relationship then obviously the overall gain will be the square of this, A_{10}^2 divided by $1 + j\omega$ by ω_{H1} square.

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And by our approximate calculation 1 by Ω_H should be $= 1$ by $\Omega_{H1} + 1$ by Ω_{H1} which is 2 by Ω_{H1} that is Ω_H should be $= 0.5$ of Ω_{H1} alright. In other words, if my gain of individual stage is like this okay this is A_1 magnitude, this is A_{10} and the high frequency cut-off point is Ω_{H1} then by cascading 2 stages what I get is what we will get a something like this, the gain would be, no I have not been able to draw it correctly let us see let us use a different color, it will come like this. Ω_H for the overall amplifier will be lower that is this amplifier this cascaded amplifier can go up to not as high frequency as the individual stage.

The point to be remembered is if you increase the gain, the bandwidth comes down, Ω_{H1} the bandwidth is a $\Omega_H - \Omega_L$ the high frequency cut-off – the low frequency cut-off so if Ω_H goes down naturally the bandwidth goes down, at the cost of bandwidth we increase the gain okay. Now this is a very simple case where we can calculate the high frequency 3 dB point exactly okay.

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$$\begin{aligned}\frac{A_{10}^2}{\left| \left(1 + j \frac{\omega_H}{\omega_{H1}} \right)^2 \right|} &= \frac{A_{10}^2}{\sqrt{2}} \\ 1 + \frac{\omega_H^2}{\omega_{H1}^2} &= \sqrt{2} \\ \Rightarrow \omega_H^2 &= \sqrt{(\sqrt{2}-1)} \omega_{H1}^2 \\ \omega_H &\approx 0.64 \omega_{H1}\end{aligned}$$

It is not very difficult because the relationship to be satisfied is A_{10} square divided by magnitude $1 + j \Omega$ by ΩH_1 square if the overall high frequency 3 dB point is ΩH then I put ΩH this should be = how much? A_{10} square divided by for the 3 dB frequency this should be divided by root 2 that is the 3 dB point and therefore I can solve this very simply $1 + \Omega H$ square divided by ΩH_1 square = root 2, if I take the magnitude take the square or take the square and then take the magnitude it will be the same thing this is what we will get and therefore from this you get ΩH square as = root 2 - 1 times ΩH_1 square or if I take the square root of both sides I shall get this and you can easily verify that root 2 - 1, 0.412 - 1 that is the square root of 0.412 this is approximately 0.64 ΩH_1 , which means that our estimate by method of open circuit time constants what are the estimates?

Estimate was 0.5 ΩH_1 so our estimate was pessimistic is not that right, it was pessimistic we anticipated more danger than what it is actually, it is not half it is 0.64 times ΩH_1 and there is a deviation but when there is large number of capacitor and a large number of such time constants this is the only method that is available to an engineer, of course it can make your life miserable by writing the exact load equations, trying to solve the equation but you will spend a lot more time than is really called for okay that is an engineering approximation. The point at this question is that our estimate by the method of open circuit time constant is pessimistic that is what we get will be the actual situation will be brighter than what we get by this estimate.

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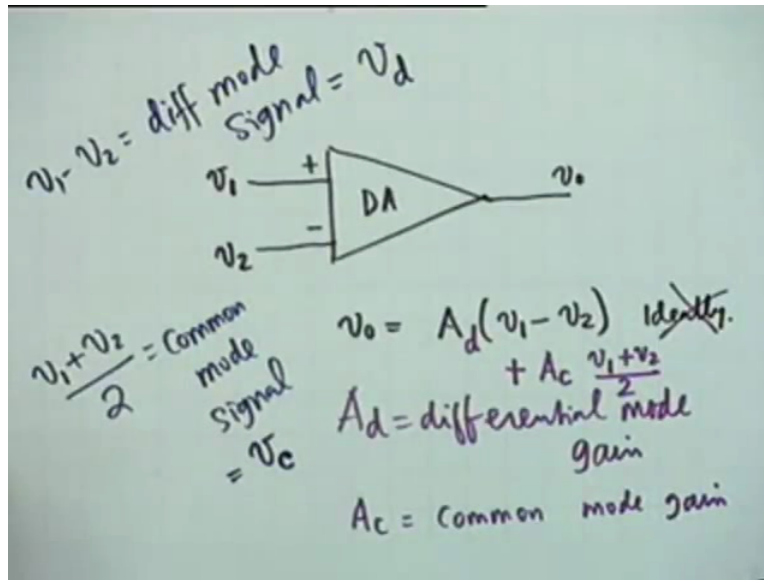
$$A(j\omega) = \frac{A_{10}^2}{\left(1 - j \frac{\omega_{L1}}{\omega}\right)^2}$$
$$1 + \frac{\omega_{L1}^2}{\omega_L^2} = \sqrt{2}$$
$$\omega_L = \frac{\omega_{L1}}{\sqrt{\sqrt{2} - 1}} \approx 1.56 \omega_{L1}$$

Similarly suppose we consider the low-frequency gain and at the low-frequency condition A_j Ω will be of the form A_{10} divided by $1 - j \Omega L_1$ by Ω whole square agreed and 2 stages are cascaded, this is at the low-frequency. And you can see that the equation describing the 3 dB frequency low-frequency 3 dB cut-off would be $1 + \Omega L_1$ square divided by ΩL square and this should be $= \sqrt{2}$ and therefore ΩL , is this point clear? Magnitude $= A_{10}$ I have made a mistake, this is A_{10} square it will be A_{10} square divided by $\sqrt{2}$ by simplifying this, this is what you get and ΩL therefore shall be $= \Omega L_1$ divided by square root of $\sqrt{2} - 1$ and this is approximately $1.56 \Omega L_1$.

What is our estimate by the method of short-circuit time constant? Our estimate is twice ΩL_1 and therefore what we get is instead of twice ΩL_1 I get a smaller value I get a smaller value that means our estimate is again pessimistic alright. So these estimates are very much favored by engineers because what you are going to get in practice is a better situation a brighter situation alright. Okay with this we close the discussion on amplifier frequency response, we shall come back to this topic after we discuss the differential amplifiers and power amplifiers that is when you consider wide banding techniques given an amplifier a common emitter amplifier it is a certain bandwidth, now we want to increase the gain and you also want to increase the bandwidth so what do we do, how to be wideband an amplifier?

And you shall see that we will encounter more than 2 transistors and we will see that the method of open circuit and short-circuit time constant are very-very handy methods for calculation of the performance of such amplifiers. Now on the topic of differential amplifiers 1st what is differential amplifier?

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The symbol of any amplifier is this triangle, for a differential amplifier we write DA differential amplifier and for an operational amplifier we write OA okay, for any other kind of amplifier we do not write anything we simply write we simply draw this box. Now a differential amplifier has 2 inputs; one is a non-inverting input and other is an inverting input, now this voltage we shall call V 1 and this voltage we shall call V 2 okay V 2 is the inverting input it is not an Opamp though it is not an Opamp it is a differential amplifier and the definition of differential amplifier is that the output voltage single ended output, output voltage Ideally some gain A multiplied by V 1 – V 2 okay ideally, this is the ideal situation.

Now it turns out that ideally is V 1 and V 2 are equal if these 2 terminals are clipped together and the same voltage is applied the output should be 0, it turns out that in practice the output is not = 0 and therefore the gain that we get here we call this a differential mode gain okay A sub d is called differential mode gain and no longer ideal, it turns out that if V 1 and V 2 are identical, the output is not 0 and therefore to this we must add another term which is the common mode gain A sub c, c for common mode that is only two voltages are identical and we put V 1 + V 2 divided

by 2 okay. You can see that if V_1 and V_2 are identical then this term would be 0 and output would be A_c multiplied by V_1 is that clear that is how the division by 2 okay, A_c is called the common mode gain common mode gain.

And accordingly these 2 voltages that is $V_1 - V_2$ is called differential mode signal and we use the term V_d for this and $V_1 + V_2$ divided by 2 is called the common mode signal and the term for this is V_c common mode signal. Ideally what we want is when V_1 and V_2 are equal the output should be = 0, the output should only be proportional to the difference between the 2 signals, the practical situation is that there is a common mode signal there is a common mode component in the output.

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$$v_o = A_c v_c + A_d v_d$$

$$v_o = A_1 v_1 + A_2 v_2$$

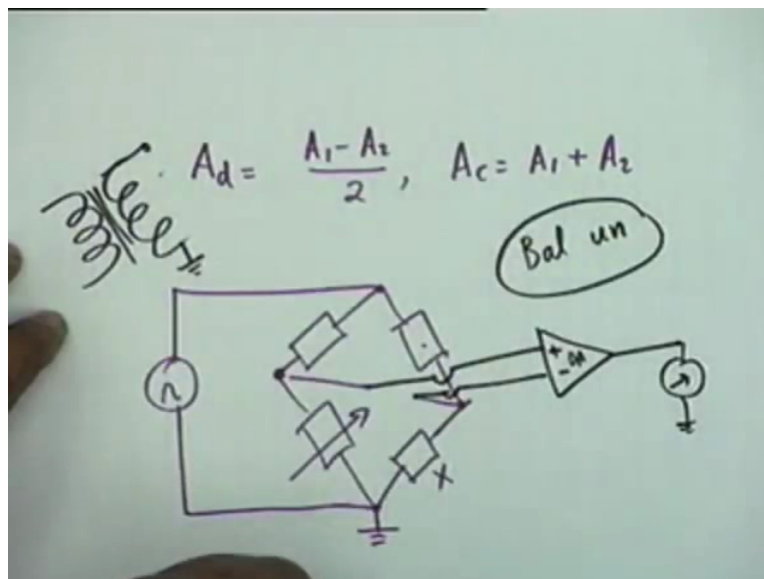
$$A_c = \left. \frac{v_o}{v_1} \right|_{v_1 = v_2}, \quad A_d = \left. \frac{v_o}{2v_1} \right|_{v_1 = -v_2}$$

$$A_1 = \left. \frac{v_o}{v_1} \right|_{v_2 = 0}, \quad A_2 = \left. \frac{v_o}{v_2} \right|_{v_1 = 0}$$

And therefore for a non-ideal differential amplifier the output voltage is given by A_c V_c the common mode signal + A_d the differential mode gain multiplied by the differential mode signal. The definitions are that $V_d = V_1 - V_2$ and V_c is $V_1 + V_2$ by 2, obviously we should be able to write V_o in terms of V_1 and V_2 also instead of V_c and V_d you can expand this and therefore you can get $V_o = A_1 V_1 + A_2 V_2$ and the definitions are clear, this is another way of writing the same equation the definitions are clear, measurements can also be made for example if you want to find out A_c the common mode gain obviously, this is V_o divided by you want to make this term = 0 so V_o by V_1 let $V_1 = V_2$ agreed.

So you clip the 2 together, apply the voltage measure the output then V_0 by $V_1 =$ this. Similarly, $A_{sub d}$ would be V_0 by $2 V_1$ but you want to kill the common mode signal so you make $V_1 = -V_2$, if you make $V_1 = -V_2$ than $V_{sub c}$ would be 0 and this would be twice V_1 and therefore V_0 by $2 V_1$ under the condition $V_1 = -V_2$, so given a differential given a differential amplifier you can measure $A_{sub c}$ and $A_{sub d}$ very easily in the laboratory, these are all small signals these are signal quantities not DC quantities okay. Similarly, if you want to measure A_1 and A_2 it is obvious V_0 by V_1 with $V_2 = 0$ that is the inverting terminal you connect to ground, apply V_1 and measure the output. Similarly, $A_2 = V_0$ by V_2 under the condition $V_1 = 0$ so all of them can be measured in practice.

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You also notice that $A_{sub c}$ and $A_{sub d}$ can be expressed in terms of A_1 and A_2 right by simple algebra and I shall not repeat this, I simply write down the expression. A_d well $A_d = \frac{A_1 - A_2}{2}$ and $A_c = A_1 + A_2$ they are very simply related so measuring any 2 of these parameters of the 4 suffices to characterise the differential amplifier. Question; why should we bother about differential amplifier why should we bother about amplifying the difference between 2 signals? Take a very simple measurement situation a Wheatstone bridge which we use to measure impedances, there are 4 impedance is like this there is a source let say from here to here and there is a detector between the other 2 ends now you see the source is usually grounded so the

detector that we use you can use a CRO for example because CRO one terminal is grounded okay.

You can use a meter, an ammeter or voltmeter but ammeters and voltmeter are not as sensitive as we want them to be in modern instrumentations situations. Since you are testing for null, you are trying to find out you see 2 of them will be standard resistors standard impedances, the 3rd would also be a standard the 4th the 3rd would be a variable the 4th is unknown and you want to measure you want to check the null that is under which conditions the voltage between these 2 points becomes = 0 so you should for sensitive measurement you should be able to measure very small signals, signals of the order of microvolts and that can be done only when this signal is amplified and then put to ammeter so what we do is we apply this to a differential amplifier.

And the output then we can measure by means of a meter, output can be connected output detector can be corrected to ground one terminal can be connected to ground now because this has caused a transformation from a balanced voltage, balanced voltage is one neither of whose terminals are grounded to an unbalanced voltage in which one of the terminals is grounded. So what we have done is balance to unbalance transformation by means of a differential amplifier and this helps us in checking the null condition of the bridge, this is one of the one of the very prominent uses of the differential amplifier. And any such transformation just a side comment, any such transformation which transforms balanced voltage to an unbalanced voltage is called a loan Bal-un balance to unbalance, can you give me another example of Bal-un very common example?

“Professor–student conversation starts”

Student: (())(24:30)

Professor: (())(24:33) Yes there is a Bal–un there, a more common you must have seen it in the laboratory many times. A transformer an ordinary transformer this voltage can be balanced, the output can be unbalanced okay, you could apply a less voltage here and an unbalanced because there is electrical isolation there is only magnetic coupling, a transformer is a Bal-un balance to unbalanced or vice versa, you can also transform there is no reason why this cannot be primary and this cannot be secondary so balanced to unbalanced or unbalanced to balance.

Student: Both are called Bal-un?

Professor: Okay, the one is called Bal-un, the other is called Un-bal okay that is not a very common term.

“Professor–student conversation ends”

But our interest is not simply in measurements, our interest is in electronic circuits of all kinds and differential amplifier forms the input stage of most of analog integrated circuits most analog integrated circuits chips with it is a phase detector or an amplifier or whatever it is, the input stage is a differential amplifier, differential amplifier forms the heart of the operational amplifier which you have known for far as a block. Inside the Opamp the 1st stage and the few subsequent stages they are all differential amplifiers, differential amplifier forms the input end of almost all analog integrated circuits and of course we cannot do without it in an Opamp the gain is basically obtained from a differential amplifier, the gain of an Opamp is high gain 10 to the 6 of the order of 10 to the 6 is obtained from differential amplifier.

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$$v_o = A_d v_d + A_c v_c$$
$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB.}$$
$$A_d \gg A_c$$
$$(S/N)_o \gg (S/N)_i$$

Now desirability is I told you that output $A_d v_d + A_c v_c$, ideally we want A_c to be = 0 ideally, so measure of performance measure of goodness of a differential amplifier is obtained as the ratio A_d by A_c and if it is ideal then this ratio should be infinity so we want this ratio to be as large as possible and to be able to ignore the phase inversion which

may occur we take the magnitude of this and this ratio is called the CMRR Common Mode Rejection Ratio CMRR is defined as this as the ratio, now this ratio can be very large let us say 1000 a typical value. Instead of expressing this as a number sometimes we express this in terms of decibels so we multiply by 20 then take the log with respect to base 10 and express this in dB. A CMRR of 60 dB corresponds to a number of 1000 alright so CMRR is often expressed in decibels.

Now what we want is therefore that A_{sd} must be much greater than A_{sc} okay so if the signal to noise ratio at the output is denoted by S/N_o and a signal-to-noise ratio at the input is denoted by S/N_i then since A_d is much greater than A_c , the signal to noise ratio at the output will be much greater than the signal to noise ratio at the input, why? Noise is the common mode, if you have 2 terminals here the same amount of noise will be picked up by both alright but the differential amplifier discriminates against common mode signals and therefore the noise at the output noise at the input will not be amplified, will be amplified only by A_c the common mode gain, the signal component will be amplified by A_d and if A_d is much greater than A_c , naturally this ratio at the output will be much greater than the ratio at the input, so signal-to-noise ratio is improved by differential amplifier, this is another bright feature of differential amplifier.

Student: Sir it sounds very good but it is not understood.

Professor: Okay.

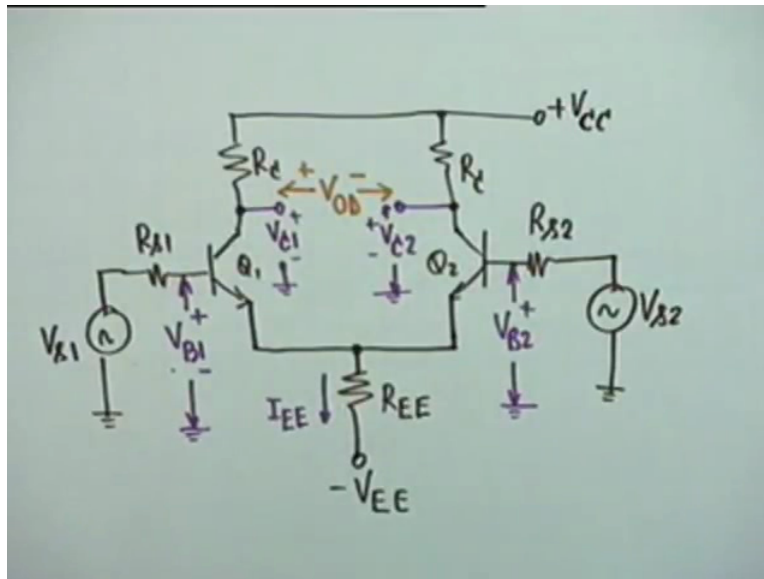
My signal is the differential signal $V_1 - V_2$ alright, where each terminal picks up some noise, this may be noise due to device may be noise due to external circumstances and so on, so at the input we shall have signal and also noise, at output also we shall have signal as well as noise, signal will be amplified by much larger quantity than the noise and therefore signal to noise ratio at output shall be much larger than signal-to-noise ratio at input alright because A_d is much greater than A_c , noise is a common mode signal that is the fundamental result.

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$$\begin{aligned}v_o &= A_d v_d + A_c v_c \\ &= A_d v_d \left(1 + \frac{v_c/v_d}{\text{CMRR}} \right) \\ v_o &\rightarrow A_d v_d \text{ if } \text{CMRR} \gg \frac{v_c}{v_d}\end{aligned}$$

I can write this relation in a slightly different form, $A_d v_d + A_c v_c$, I can write this as $A_d v_d$ is the ideal value, and the deviation I can put in the form $1 + v_c/v_d$ divided by CMRR if it is a positive quantity, CMRR is taken as the magnitude so we will consider this as a positive quantity. And naturally if v_o is to tend to $A_d v_d$ then CMRR must be much greater than the ratio of the common mode signal to the differential mode signal, this is another way of expressing the same relationship. Now so far about the general terminology, let us look at the practical circuit.

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The circuit has 2 identical transistors Q 1 and Q 2 identical transistors biased Identically that is you have R sub c here and R sub c here and these 2 are taken to + V cc alright, the emitters of the 2 transistors are coupled together coupled directly they are connected together so differential amplifier will also sometimes known as an emitter coupled pair ECP emitter coupled pair, 2 transistors whose chemicals are tied together alright. In the current mirror, can we give another name to current mirror?

Student: Collector Base.

Professor: Base coupled, 2 bases are tied together so base coupled pair.

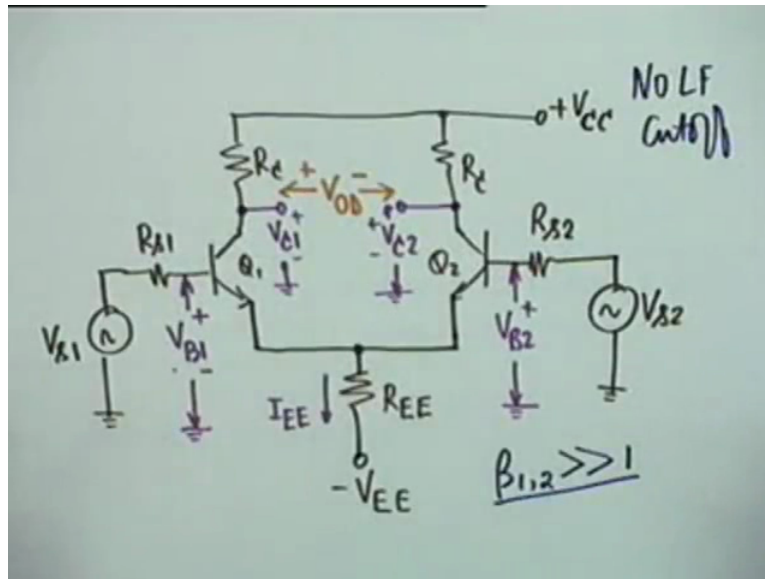
This is an emitter coupled pair and one of the circuits is there is a resistance here we call this R EE resistance from the common emitter terminal and this goes to - V EE negative supply, we will see that in integrated circuits one always uses a positive as well as negative supply, usually it is same value + 12 0 - 12 okay it is a usual thing but there is no nothing sacred about then the equal, you can have you can have a different story, but if you usually + V cc 0 - V cc so that the common point can act as a what? Ground... 0 connection that sets the reference otherwise integrated circuits are available as package, you can connect any terminal to ground your choice but this reference of 0 potential is set by the common point of the power supply okay.

Then you have to the input to the base you have an R_{s2} 2nd transistor, a voltage source V_{s2} , this is the signal this is the RMS value V_{S2} and similarly you have R_{s1} , these are the 2 inputs inverting and non-inverting, we will see which one is inverting which one is non-inverting later, they can be interchanged in fact depending on where you take the output, the output voltages now we shall 1st make DC analysis, this is the circuit this is the total circuit we shall 1st make DC analysis of this circuit, we will call this current as I_{EE} the DC current, we will call this voltage as V_{B1} between this point and ground, this voltage we will call V_{B2} this point and ground, this voltage we will call V_{c1} between this point and ground, the collector 2 voltage we will call V_{c2} + – again between ground.

And in addition and in addition I will take another colour, in addition this voltage, voltage between these 2 we shall call as V_{OD} with this polarity V_{OD} alright. You notice a very interesting thing that we have not used any capacitor in the circuit, we have not used any coupling or bypass capacitor and therefore what would be its low frequency cut-off? DC, so this amplifier would be able to amplify right from DC up to some high frequency determined by the capacitors inherent to Q_1 and Q_2 so no low frequency cut-off that is a very important characteristic of this amplifier No LF cut-off and I have already said Q_1 and Q_2 are identical.

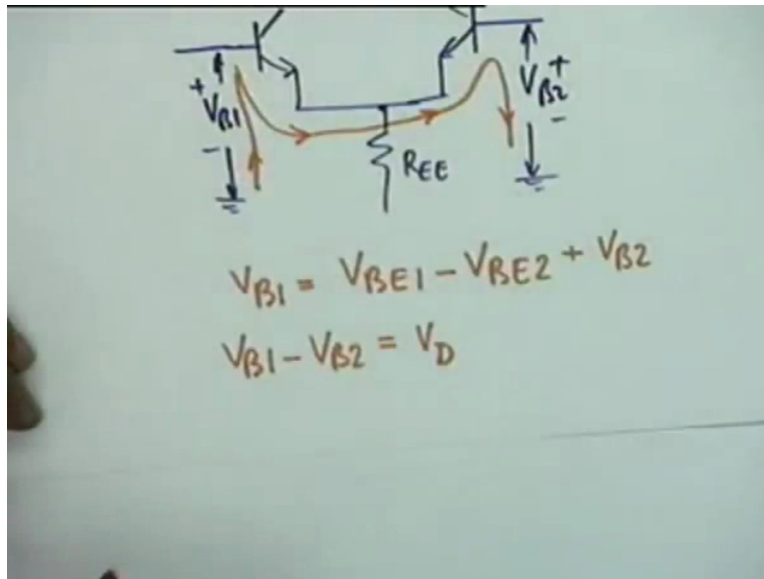
In the analysis we assume that $\beta_1, 2$ are much greater than 1 for both the transistors, in integrated circuit making 2 identical transistors is absolutely no problem, in fact we makes thousands in the same chip identical transistors, identical does not mean that beta shall be equal, beta can be spread but nevertheless if one of them has beta of 150, the other cannot be beta of 10, it will be 149 or at the most let say 151, it will have a spread small spread but nevertheless we assume that $\beta_1, 2$ is much larger than 1 which means that I_{c} for both the transistors 1, 2 would be approximately = I_{E} 1, 2 that is the base current can be ignored alright base current can be ignored.

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Now if I look at this part of the circuit, forget about what we connected there this is $V_{B1} + -$, this is $V_{B2} + -$, I want to look at this part of the circuit from here to here, I want to come from ground and go like this, ground to ground I make a complete loop in other way I can write KVL and you notice that V_{B1} would be $= V_{BE1} - V_{BE2} + V_{B2}$ agreed, is that clear? Okay so I can write V_{B1} the base voltage of transistor 1 - the base voltage of transistor 2, which obviously is the input differential voltage input differential voltage so I will call this, instead of writing V_{ID} , I shall simply write it as V_D I will not use I.

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“Professor–student conversation starts”

Student: Sir the last analysis we did was totally for A c.

Professor: No this is totally for DC.

Student: $V_0 = A c$.

Professor: We will come back to that we will come back to that, from DC we shall go to AC okay from DC we shall go to AC okay.

“Professor–student conversation ends”

These are all DC quantities now, $V_{B1} - V_{B2} = V_D$, I define this as V_D therefore this = $V_{BE1} - V_{BE2}$ okay, the differential voltage is simply = $V_{BE1} - V_{BE2}$.

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$$\begin{aligned}V_D &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{I_{C1}}{I_{C2}} \\ \frac{I_{C1}}{I_{C2}} &= e^{V_D/V_T} \quad (1) \\ I_{C1} + I_{C2} &= I_{EE}\end{aligned}$$

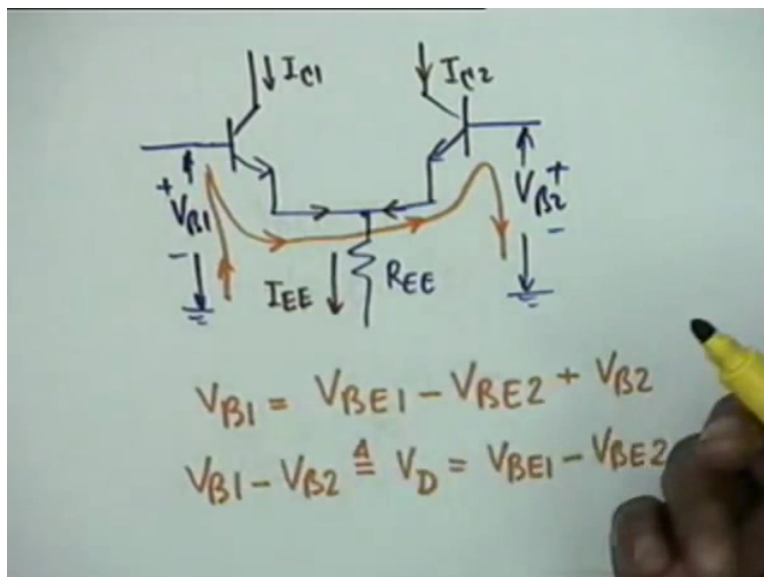
We also know that the collector current I_{C1} = the reverse saturation current I_S multiplied by e to the power base to emitter voltage divided by V_T , this T is not threshold for FET it is thermal voltage that is approximately 25 or 26 millivolts at room temperature. And when the transistor is in the active region, V_{BE} is a positive quantity and this becomes approximately I_S the exponential term dominates so I get V_{BE} divided by V_T , which means that $V_{BE} = V_T$ multiplied by \ln of I_{C1} divided by I_S alright. I can now introduce the subscript $V_{BE1, 2}$ shall be V_T the 2 transistors are identical so V_T shall be identical and therefore the $I_{C1, 2}$ alright.

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$$\begin{aligned}V_D &= V_{BE1} - V_{BE2} \\ &= V_T \ln \frac{I_{C1}}{I_{C2}} \\ \frac{I_{C1}}{I_{C2}} &= e^{V_D/V_T}\end{aligned}$$

And therefore V_D which $= V_{BE1} - V_{BE2}$ shall be $= V_T \log$ of I_{C1} divided by I_{C2} , now we take the exponential on both sides that is I_{C1} divided by I_{C2} would be $= e$ to the power V_D by V_T alright.

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We go back to the same circuit we go back to the last one slide and we notice that this current is I_{C1} and this current is I_{C2} since we have ignored the base current, the same current must flow here and here I_{C2} so emitter current the current through R_{EE} is $I_{EE} = I_{C1} + I_{C2}$

therefore this gives us the 2nd relation that is $I_{c1} + I_{c2} = I_{EE}$ we shall see later that we will try to maintain I_{EE} as a constant the total current, there can be a sharing between 2 transistors, I_{c1} and I_{c2} may be different because of different voltages applied to their bases but the total current we shall try to keep constant, so these 2 equations from which you can solve I_{c1} and I_{c2} .

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The image shows two handwritten equations on a light green background. The first equation is $I_{c1} = \frac{I_{EE}}{1 + e^{-V_D/V_T}}$ and the second equation is $I_{c2} = \frac{I_{EE}}{1 + e^{V_D/V_T}}$. A yellow highlighter is visible at the bottom center of the image.

A little bit of algebra will show that $I_{c1} = I_{sub EE}$ divided by $1 + e$ to the power $-V_D$ by V_T and I_{c2} shall be $= I_{sub EE}$ divided by $1 + e$ to the power $+V_D$ by V_T alright, let us try to draw these expressions.

“Professor–student conversation starts”

Student: Sir if we apply the same signal there...

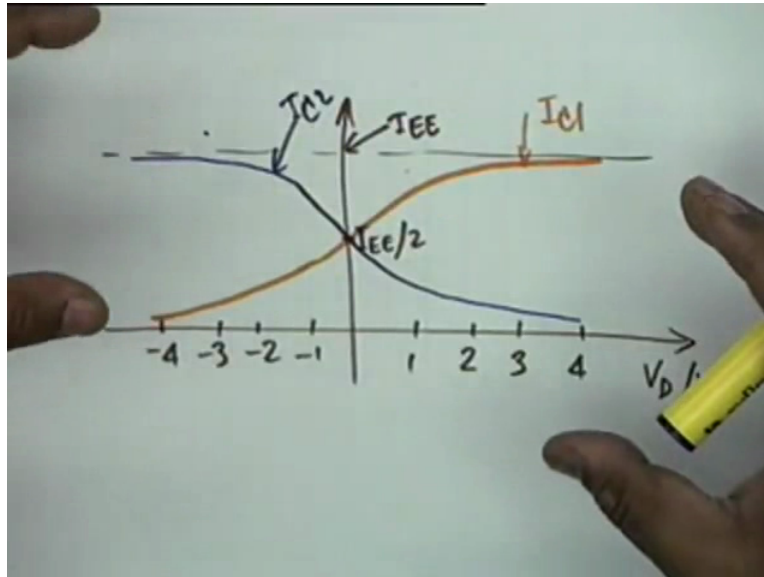
Professor: Same signal, I am not talking about signal at all, I am talking about the DC quantity, signal will come little later.

Student: Sir, why do V_{B1} and V_{B2} be different?

Professor: Why do V_{B1} and V_{B2} be different, because... the reason is clear, R_{s1} and R_{s2} we did not make them equal, we did not make V_{s1} and V_{s2} equal so there can be a difference

voltage between the 2 bases alright okay, if they are absolutely identical then of course our purpose is served, we have an ideal differential amplifier, it is to take care of non-ideality that we are going into this analysis.

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Now suppose we plot I_{c1} and I_{c2} versus V_D by V_T and let us say -4, -2, -1, -3. V_D as you can see is a difference between V_{BE1} and V_{BE2} , it can be positive as well as negative depending on which one is higher, so we go up to 4, 2, 1, 3 okay and let us say what is the maximum value that I_{c1} or I_{c2} can have? I_{EE} is not that right both of them, when V_D is not 0 when V_D is infinity very large then this term drops out and we get I_{EE} , similarly when V_D is negative infinity, I get I_{c2} maximum I_{EE} so the maximum value is I_{EE} . You also notice that when the differential voltage is 0 V_D is 0 then what the currents are equal I_{EE} by 2 so both the curves must pass through this point I_{EE} by 2 and it is very easy to see because of the exponential nature that one of them on of them will rise like this, which one is this?

Student: I_{c1} .

Student: I_{c1} .

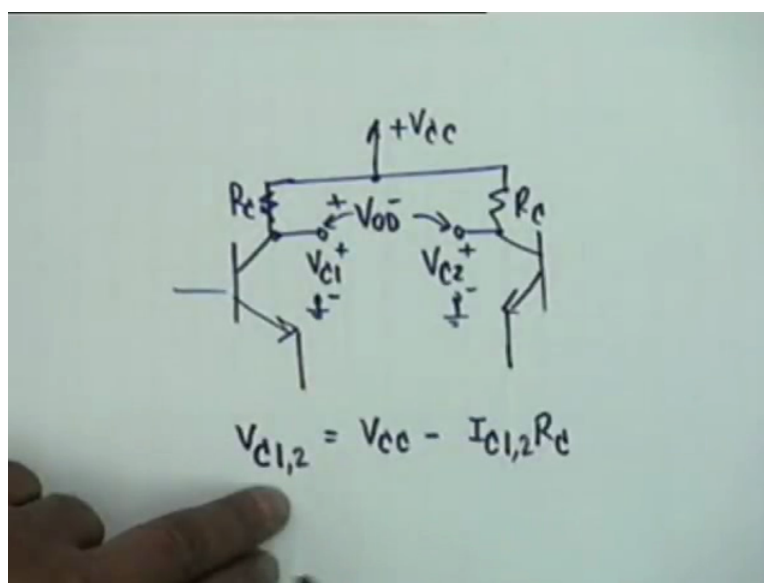
Professor: I_{c1} or I_{c2} ?

Student: I_{c1} .

This is I_{c1} , and I_{c2} naturally shall be like this and they would be perfectly symmetrical because the factors are the same e^{-V_D/V_T} . You notice that if V_D/V_T exceeds 4, I_{c1} is approximately I_{EE} and I_{c2} is approximately 0, what does this mean? It means that when V_{BE1} is greater than V_{BE2} by 4 times the thermal voltage that is approximately 25 millivolts or 100 millivolts, 100 millivolts is 0.1 volts then $(I_{c1}/I_{c2}) = e^{(V_{BE1}-V_{BE2})/V_T} = e^{4} \approx 55$ and what will be the condition of Q1 then, it will be in saturation because it passes maximum available current okay and therefore Q1 will be in saturation and Q2 will be cut off.

On the other hand, when V_D/V_T exceeds is less than -4 that is when V_D is less than -0.1 volts okay approximately Q2 becomes ON and saturated and Q1 becomes OFF and you can see the root of the reason why a differential amplifier can also work as a digital circuit, there is switching with this differential voltage swings between -0.1 and +0.1, there is switching of the state of the circuit, one transistor ON the other OFF, now becomes the former one OFF the latter one ON and therefore this circuit differential amplifier arrangement is also used in digital circuit and this is what is known as emitter coupled logic ECL emitter coupled logic, our purpose is however analog and therefore we want to see we want to see if we can have linear relationship between the output voltage and the input voltage okay.

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This is obviously non-linear relationship, we do not want any transistor to be cut off we do not want any transistor to be in saturation for you must avoid them, let us see how to avoid them.

Now if you go back to the circuit once more let me draw this; V_{CC} , there is R_C , R_C they are identical, this was $= V_{C1} + -$ between this point and ground and this voltage was $V_{C2} +$ and $-$ and this voltage was $V_{OD} +$ and minus. You can very easily see I am not drawing the rest of the circuit because that is not of concern, you can easily see that $V_{C1} = V_{CC} - I_{C1} \text{ times } R_C$ sub c alright. Similarly, V_{C2} is $V_{CC} - I_{C2}$ multiply by R_C , we know the plots of I_{C1} and I_{C2} therefore we can plot V_{C1} and V_{C2} , tell me what will be the maximum value of V_{C1} ?

“Professor–student conversation starts”

Student: V_{CC} .

Professor: And the minimum value?

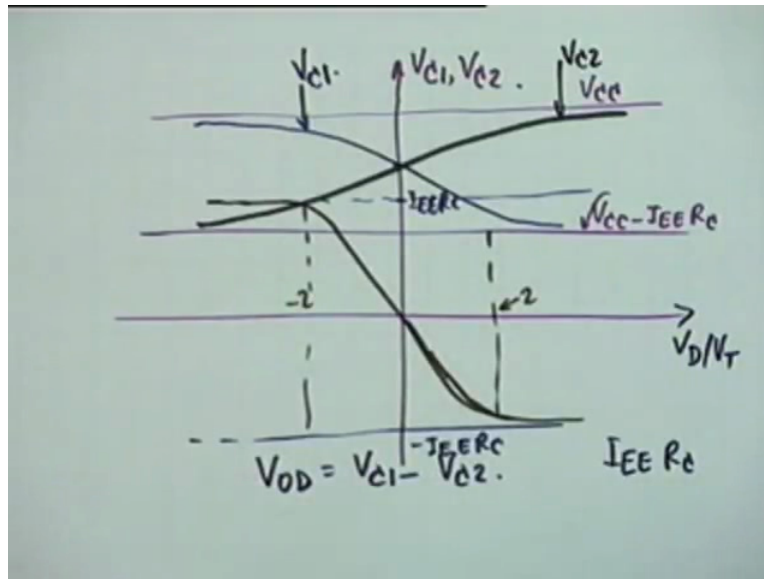
Student: $V_{CC} - I_{EE} R_C$.

Professor: That is it, it not 0, $V_{CC} - I_{EE} R_C$ so that would be the variation, when current is a maximum...

Student: Sir what about V_E ?

Professor: That is not a concern because the output is taken from this point to ground, V_E does not come into the picture alright, V_E comes into the picture later we will see this. But you notice that when the collector current is maximum this voltage is minimum, when collector current is minimum this voltage is maximum now let us see what these spots are like.

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We are plotting V_{C1} and V_{C2} , the maximum value is V_{CC} and the minimum value somewhere here is $V_{CC} - I_{EE} R_C$ this is the minimum value okay. And the voltages shall vary like this, which voltage is this? V_{C2} and other one would be like this, this is V_{C1} . Now this is V_D by V_T okay, these are the 2 voltages. If I take the output voltage V_{OD} which = $V_{C1} - V_{C2}$ okay, now what is the maximum value of this? Maximum value is $I_{EE} R_C$. And what is the minimum value? $-I_{EE} R_C$, so the output voltage shall swing between $+I_{EE} R_C$ and $-I_{EE} R_C$ and therefore let us find out let us draw a line of $I_{EE} R_C$ here, then I must go to $-I_{EE} R_C$ also okay and the plot shall look like this, it will swing between $+I_{EE} R_C$ to $-I_{EE} R_C$ and this range very approximate, I should have drawn like this.

This range is 2 and -2 approximately, the range in which the curve of V_{OD} versus V_D by V_T is approximately linear that is if this V_{DE1} and V_{DE2} are such that the differential voltage lies between $-2 V_T$ approximately -50 millivolts to $+2 V_T$ approximately $+50$ millivolts then the variation of V_{OD} versus V_D is approximately linear. What I have shown here is a degraded picture, actually it is highly linear between these 2 points okay and that can be obtained that it is highly linear can be obtained by an exact analysis for V_{OD} okay.

