Analog Electronic Circuits
Professor S. C. Dutta Roy
Department of Electrical Engineering
Indian Institute of Technology Delhi
Lecture no 14
Module no 01
Midband analysis of FET Amplifiers

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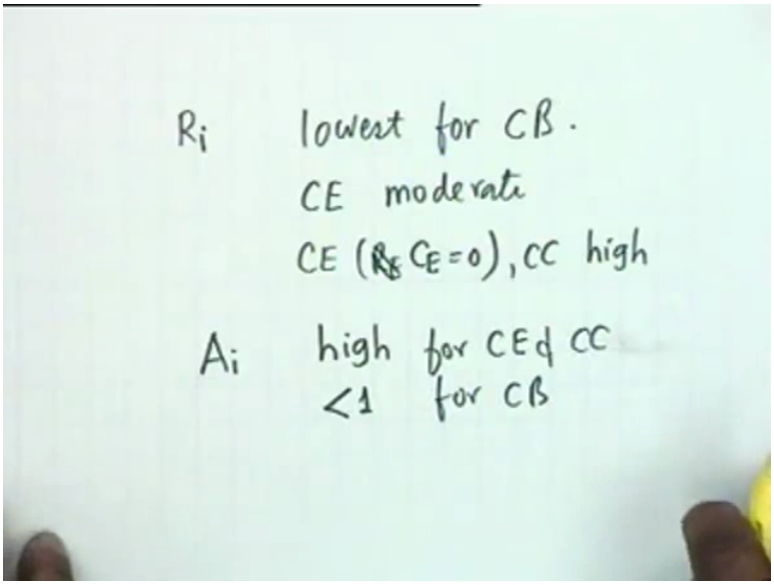

14th lecture and we are going to do midband analysis of FET amplifiers. So far we are concerned with BJT and BJT we discussed the CE connection, the CB connection common base and the CC connection common collector or the emitter follower. And you shall see that FET amplifiers are very similar in analysis and performance characteristics, for example, CE is comparable to common source CS, emitter terminal is comparable to the source terminal, common base is comparable to CG common gate, and common collector is comparable to common drain. Now what are these characteristics?

If I take voltage gain A v then is the same for CE and CB that is g m minus... No, there is a difference there is difference of phase, in CE there is an inversion, in CB there is no inversion but the again magnitude is the same g m times R L parallel R C okay. However, if CE is unbypassed R E then the gain drops down drastically agreed, unbypassed emitter resistance the gain drops down drastically. Whereas for CC, A v the voltage gain is less than 1 but very close to

unity very close to unity. These characteristics as you shall see will be the same if E is substituted by S, D is substituted by G in the case of the FET amplifier.

As far as the input resistance is concerned, the lowest input resistance is for which connection, C B common base connection is the lowest, for CE it is moderate and CE with R E unbypassed how do I indicate this, let us put C E = 0 that indicates that R E is unbypassed and CC input resistance is very high, it is of the order of r Pi + beta + 1 times R E. The current gain current gain is high for CE and CC but it is less than 1 for common base CB.

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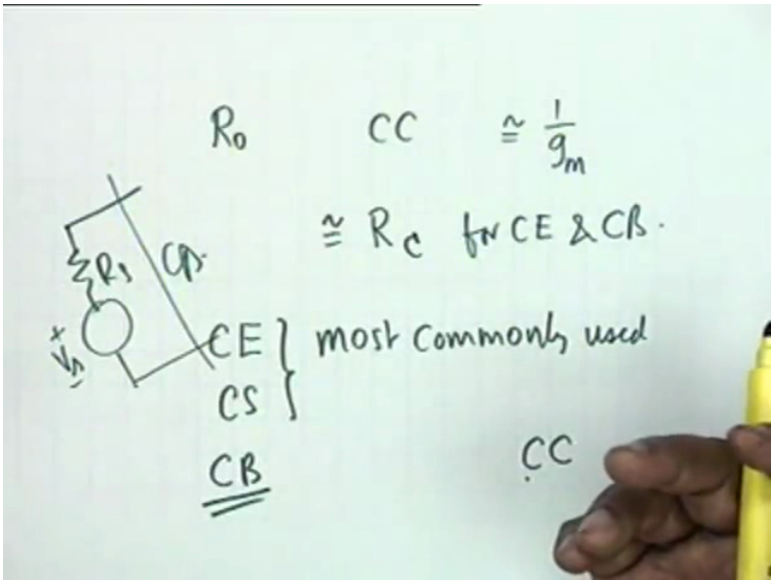

As far as R 0 is concerned which configuration has the lowest R 0? Common collector, and R 0 is of the order of 1 over g m, or the other 2 configurations they are approximately = R sub C for CE and CB, and whatever we have said so far about common emitter also applies to common source, common base also applies to common gate and common collector also applies to common gate. Of the 3 configurations the most generally used configuration is the common emitter, common emitter is the general-purpose configuration because it has moderate voltage gain, moderate current gain, its input impedance is neither very large nor very low, output impedance is of the order of R sub C so it is at your choice, this is the most commonly used. In FET it would be the common source okay, most commonly used.

Now there are 2 special uses of the common base, one special use for common base, one special use for common collector, what is this for common base? If you are driving if your signal source is high impedance then you apply to the common base because the input impedance is low. On the other hand, if your signal source has high impedance V s R s okay then you apply to a common base so that it is a current I basically, a source having high impedance is a current source okay more than a voltage source so it is at the apply a common base circuit, where as a common collector circuit is used where the source is a voltage source that means input impedance is low okay. And the common collector circuit the other use is that it acts as a buffer from a high impedance source to a low impedance load okay.

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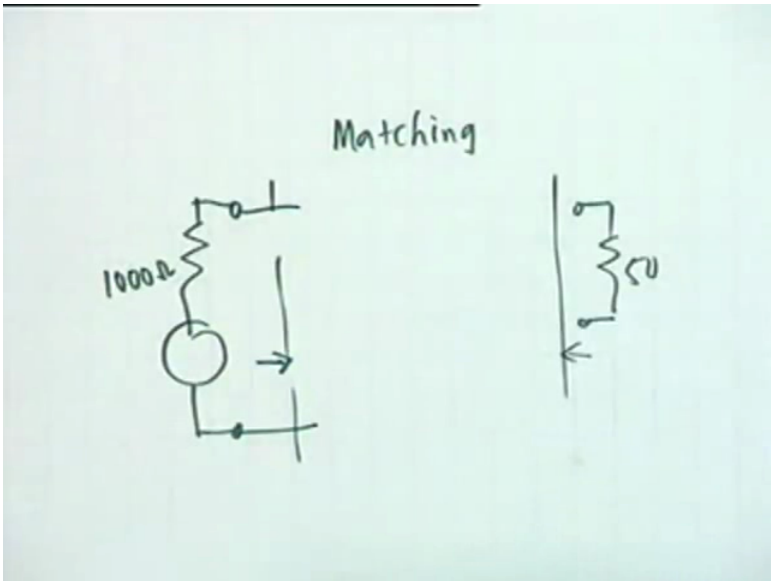

In the in the tutorial class this week there is a problem of there is a problem that is given for matching a source to a load alright. The source impedance is 1000 ohms and the load impedance is 50 ohms, obviously if we connect directly if we connect the source to the load directly there may be mismatch, so if you want to deliver maximum power to the load then what you do is, you insert an amplifier in between such that the input impedance is 1000 ohms and the output impedance is 50 ohms okay, so this is the problem of matching and an amplifier can very well fit the purpose, the problem you shall do yourself.

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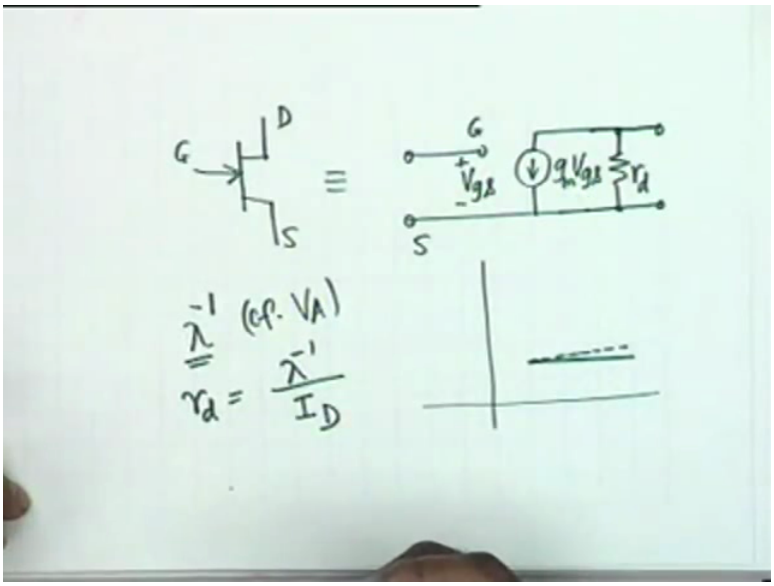

Now let us take an FET amplifier, the basic equivalent circuit basic equivalent circuit that we shall use for an FET, this is the gate, this is the drain, this is the source, basic equivalent circuit would be the gate is open, this is the source this voltage is V gs the phasor voltage and then you have a current generator g m times V gs g m times V gs and it is parallel by a dynamic drain resistance r sub d which occurs due to non-parallel nature of the characteristics with respect to the voltage axis. If you draw the FET characteristics, these are not perfectly parallel but they are slightly inclined and this slight inclination and the BJT this was called early effect, in the FET there is no special name for it but there is a voltage comparable to the early voltage and for reasons to be made clear in another course this is denoted by Lambda inverse okay.

Lambda inverse is comparable C F V sub a, the early voltage in BJT, it is for pecularisms it is called Lambda inverse okay. And r sub d you can find from the characteristics, you find its slope okay that is you extend this on the negative axis and find out where it cuts and that voltage divided by the current, you can do it that way or the Lambda inverse is given then r sub d is given by Lambda inverse divided by i sub D the drain current, in the previous case it was V A divided by I sub C okay, it is very comparable very much comparable, r d is the dynamic drain resistance.

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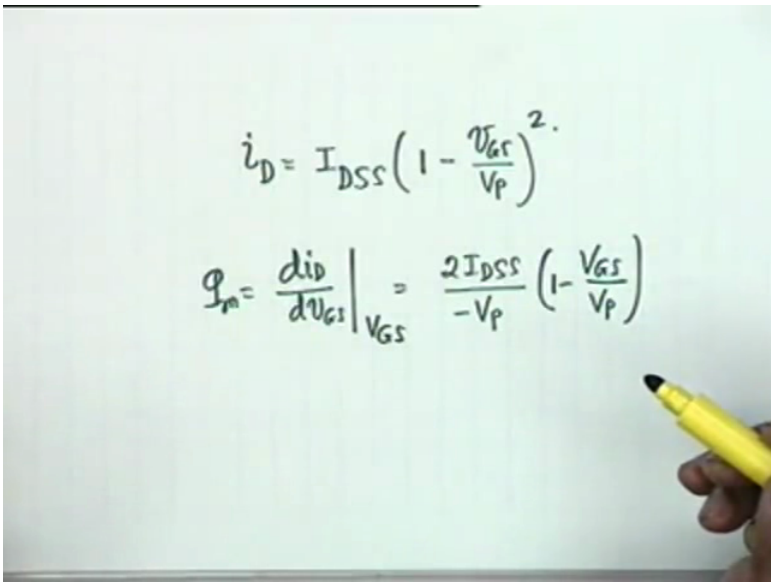

As far as g m is concerned, g m can no longer be calculated by a simple formula like the one that you had used that is I sub C divided by 26 no, no longer that because your drain current i sub D is not a linear relationship, it is a relationship like this it is a square log 1 - V gs divided by V P whole square where V P will be replaced by VT if it is an enhancement mode MOSFET. And g m has to be found out as di D dV gs at the operating point at the operating point, and you can see that this is twice I DSS divided by miners V P times 1 – V GS divided by V P, did you notice that I have changed the total voltage to the DC voltage because you shall have to find this g m at the operating point and every time you shall have to find this therefore for the transistor that is specified you must be given V P the pinch off voltage or V T the threshold voltage, we shall see how these are calculated when you take an example.

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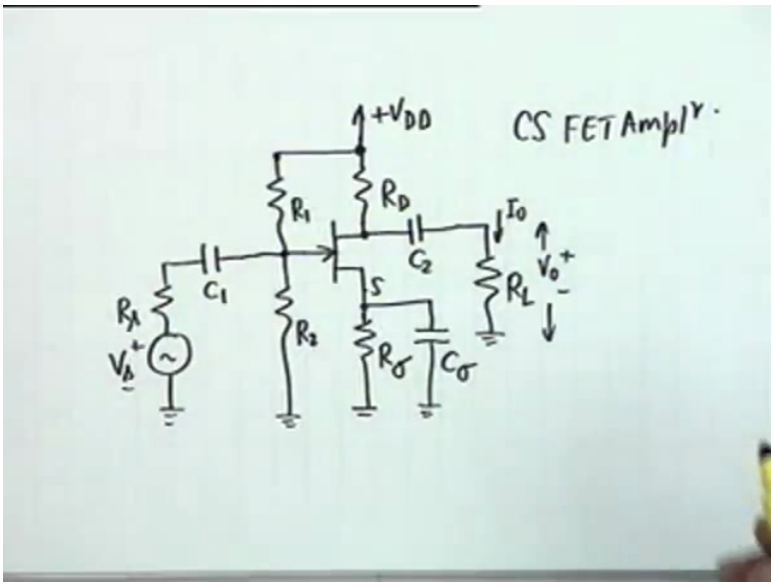

Now the analysis is very routine and similar to what we had done for BJT so we will go a little hurriedly, not quite hurriedly we will miss we will meet some of the algebraic steps okay. I will simply say this is how the equation is written and you simplify and find out the result alright, but as far as you are concerned I suggest that you do it yourself very carefully. 1st of common source amplifier, you have a V DD and usual story R sub D you have the... I am drawing the FET always as a JFET but it should be clear that the same circuit applies to MOSFET also, only the symbol shall differ okay, was simplicity I am drawing it like this okay.

This is the source and the source as you know is connected for biasing reason is connected to resistance R Sigma and you know why Sigma was used because R s is reserved for source resistance alright. And as usual R Sigma has to be bypassed by a C Sigma alright, the output is taken from the drain through a coupling capacitor C 2 and you go to a load R L, the voltage across R L is the output voltage V 0 and the current in R L is the output current I 0. As far as the the what is the nature of the channel for the FET that I have drawn? N channel therefore, what I need is a biasing through R 1 and R 2 the usual story however, I want V gs to be positive or negative? Negative, I want V gs to be negative and therefore V G must be less than V s alright, we will see how this is done then you have the coupling capacitor C 1 and the source R s and the source voltage V s once again it is the phasor, this is the common source FET amplifier alright.

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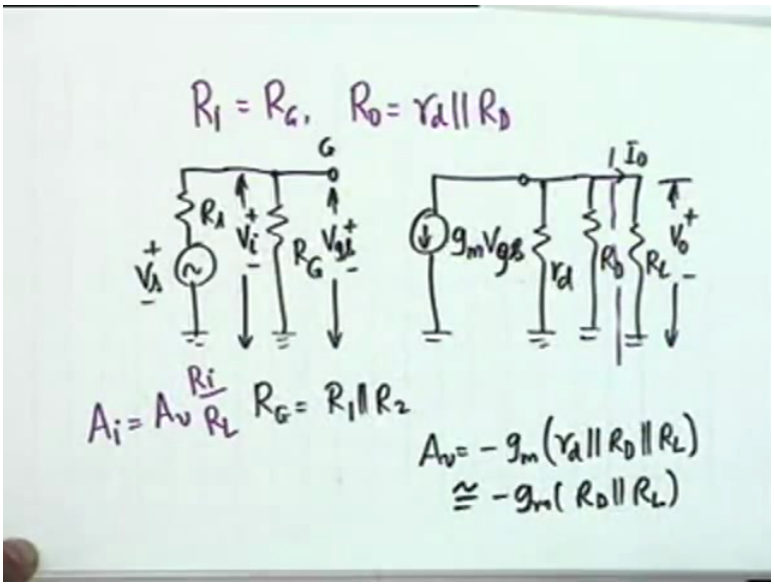

The equivalent circuit AC equivalent circuit can be drawn is the best that, we start with R s, V s, C 1 is a short, R 1 and R 2 in parallel shall give you a resistance of recall this R G, R G = R 1 parallel R 2 okay. And the gate is now open alright, the gate is now open, the source is shorted to ground as far as AC is concerned the source is shorted to ground so the only other terminal that we need is the drain and the drain has a current generator g m V gs is this voltage which is also = be V i in our usual terminology, the actual voltage that is applied to the gate between the gate and ground okay, so V i = V gs g m V gs, then we have the drain dynamic drain resistance r sub d and the 2 resistances capital R D and capital R L, it is this voltage which is the output voltage and the current through R L is the output current I 0.

It is very easy to see that the gain because V gs is the same as V i, V 0 by V i shall be simply – g m because this current does not agree with voltage, times r d parallel R D parallel R L that is it very simple the voltage gain, and usually small r d is a very large quantity therefore the gain in approximately – g m R D parallel R L, if you so desire you can denote this resistance by R L prime as we did in the BJT. Also, you looking at the circuit itself you can see that the input resistance R i is simply = R G, no complications no r Pi, no r x no further feedback so R i = R G and what about R 0? If you look from here it is simply the parallel combination of r d parallel R D because the current generator is a 0 current generator and it has internal impedance of infinity.

0 because V s is 0 then V i shall be = 0 alright, and therefore we have found out the gain and the 2 impedances by inspection, the only thing that remains to find out is A i which is a current gain is given by A v times R i by R L and it is very easy to see what this expression would be.

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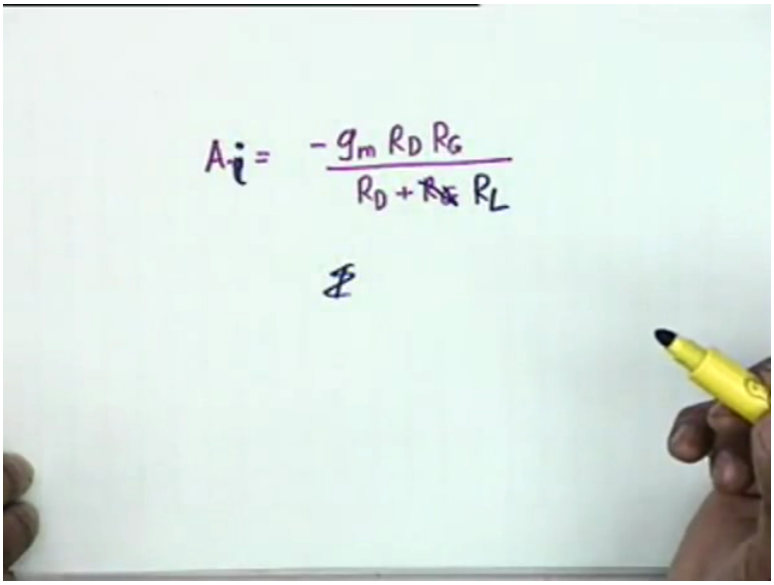

"Professor–student conversation starts"

Professor: This would be =, A v would be = – g m R D R G divided by R D + R G is that correct?

Student: R L.

Professor: R L that is correct, this should be R L.

Student: In the numerator also.

Professor: No, in the numerator R L cancels out.

Student: This is A i sir.

Professor: Oh this is A i this is A i, now it is correct? Fine we will take an example. See analyses is very simple, it is much simpler than BJT why, because the gate is isolated from the source and the drain okay, gate does not have the forward feedback path so the analysis is very simple and it can be done by inspection

“Professor–student conversation ends”

Let us take an example, we have a common source FET amplifier please look at this carefully, I DSS, the calculation is a little complicated more involved than BJT because of the trouble of finding g m okay, and because V gs is V G – V s, you have to make sure that V gs is negative, you have to make sure that V DS is greater than V gs - V P alright, so you have to make all these things clear otherwise the transistor will not work as an amplifier, all these checks were not needed. As long as Q point is found out in a BJT, a Q point which is reasonably a good Q point you have to worry about nothing else, in an FET you do have to, let us see.

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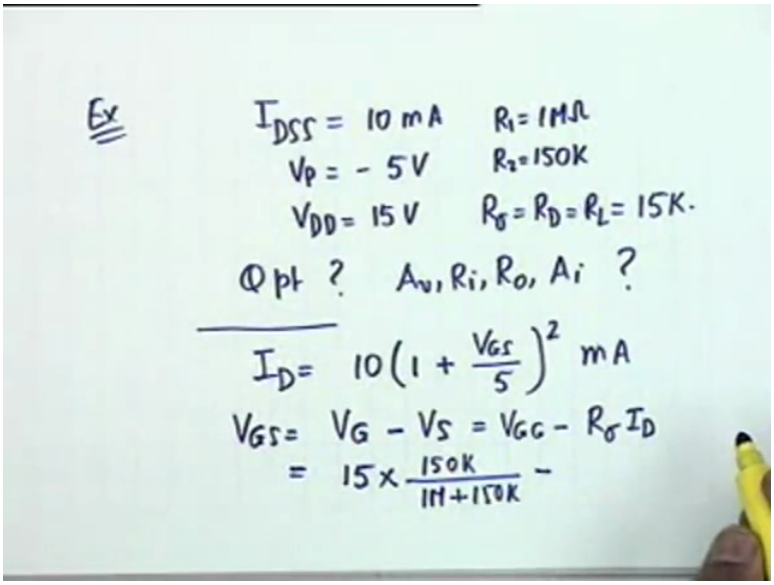

I DSS is 10 milliampere given, V P is given as - 5 volt, VDD is 15 volt, R 1 is 1 Megh, R 2 is 150 K and R Sigma = R D = R L, all these 3 resistors are equal and value is 15 K alright. The question is to find the Q point and also the values of A v, R i, R 0, and A i, these are the things to be found out in common source amplifier. Now the 1st thing you do is to find out the drain current the Q point drain current and you know the drain current I sub D is I DSS that is 10 milliampere, 1 – V GS divided by V P so that is 1 + V gs divided by 5 whole square milliampere is that clear, because V P is - 5 so the sign has become positive okay.

Also you see V GS = V G – V s, what is V G? VG is V GG V G is V GG - R Sigma times I D therefore V GS what is V GG, this is 15 multiplied by R 2 that is 150 K divided by 1 megh +

150K – R Sigma is 15 K time I D. Substitute this here, then you get an equation in I D which is not a linear equation which is not a linear equation which is quadratic.

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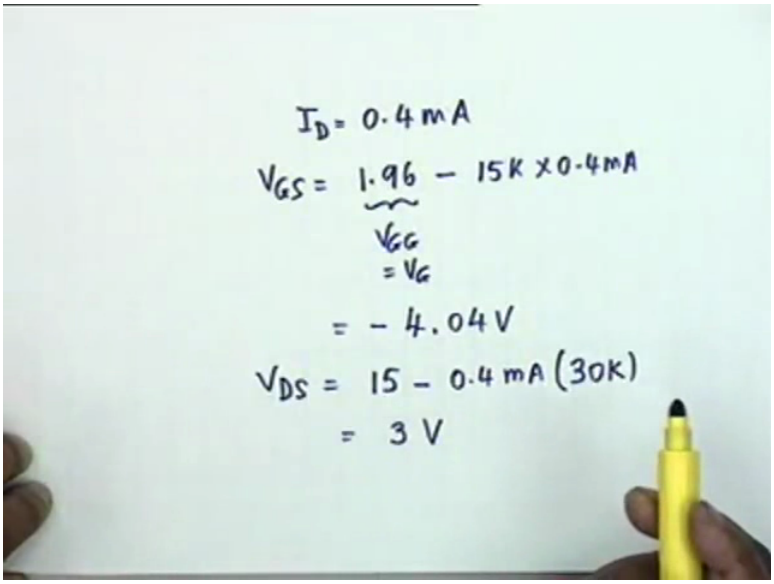

And the equation after you clear the algebra and solve it okay, I will skip all this arithmetic you get I sub D = 0.4 milliampere. Now a quadratic has 2 solutions, you must be careful in choosing the solution, the other solution will make the FET not operate in the linear region alright, the other solution would not be acceptable therefore V GS if ID is 0.4 milliampere, you will get V GS as 1.96 – 15K this is V GG Incidentally, which is also = V G 15K multiplied by 0.4 milliampere, this 6 volts and therefore V GS is - 4.04 volts. And under this condition V DS is his V DD that is 15 - 0.4 milliampere multiplied by R D + R Sigma that means 30 K alright 15 + 15 and this comes out as 3 volts, 3 volts and 0.4 milliampere is the Q point. Finally you have to check whether this V DS is greater than V GS – V P, obviously it is so okay alright that you check yourself.

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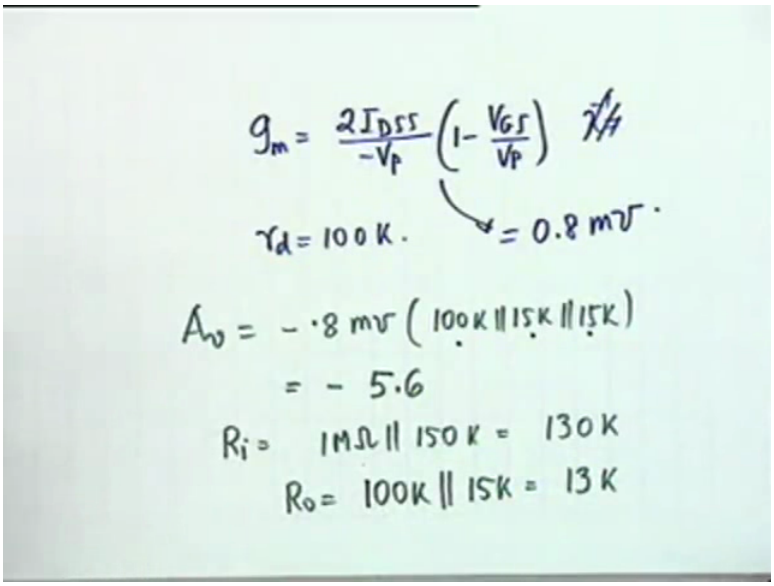

Now other thing that you needs to be found out is g m and r d, it is given that Lambda inverse for this no... r d is given I will take the Lambda inverse case later, r d is given as 100 K, how do you find g m? g m is twice I DSS divided by – V P then 1 – V GS upon V P, everything is known you can substitute the values and get g m as = 0.8 millimho be careful in this calculation. And then once you have found this out, the other things are simply putting down the formula or just looking at the circuit, you can write down the equation by looking at the circuit. A v would be – g m that is 0.8 millimho parallel combination of 100 K, 15 K and 15 K, R D, R L, r d this comes out as - 5.6.

R sub i which is R G is 1 megh parallel 150 K and this comes as 130 K. R 0 would be if you take small r d into account, 100 K parallel 15 K and this becomes 13 K alright, now let us complicate matters, is there any question on this? If I can proceed at this rate we will be in good business.

“Professor–student conversation starts”

Student: Excuse me sir.

Professor: Yes.

Student: When you have a resistance R E, will not that change the equation for I D (())(26:18)

Professor: Small r d?

Student: Yes.

Professor: Small r d comes only in the AC equivalent circuit, not in the DC. Small r d comes only in the AC equivalent circuit (())(26:36).

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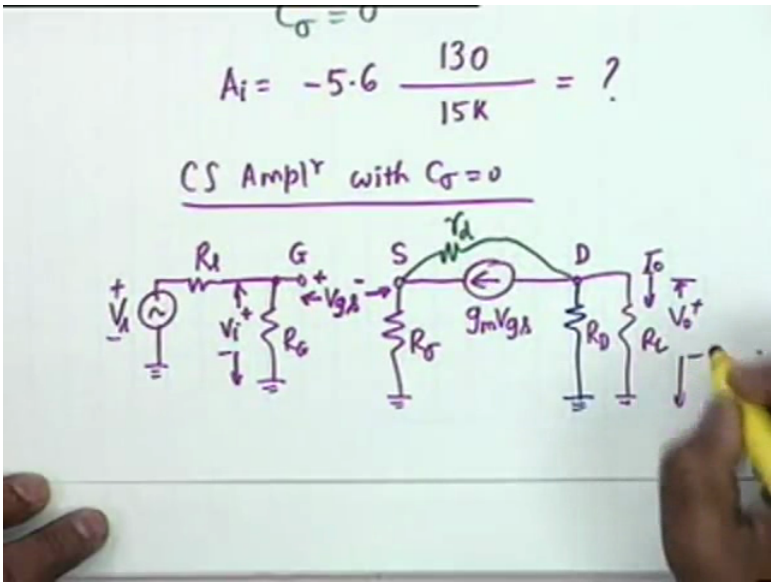

We next consider next complicate matter, let us put C Sigma = 0 that is an unbypassed source resistance, now what will be the... Yes.

Student: Sir we have not found the current gain.

Professor: We have not found the current gain oh, A sub i is A v that is - 5.6 multiplied by R i, R i is 130 K divided by R L is 15 K, you calculate what this value is okay.

“Professor–student conversation ends”

Okay so let us consider a CS amplifier, C Sigma = 0 and all that we have to do now is to draw the equivalent circuit carefully and that solves the problem as you shall see. The equivalent circuit if we proceed in the usual manner, V s, R s then you shall have R G the same circuit this is the gate, then since the source is not bypassed we must include R Sigma agreed, and this is the voltage which is V gs + - . No longer it is to ground no longer V gs = V i, no V gs is not = V i

agreed, oh one thing that I did not calculate was A vs which you can very easily find out as A v multiplied by R i divided by R i + R i that is very simple so I do not have to repeat that, let me go to only procedures which are new.

Then from the drain to the source we have g m V gs and to complicate matters there is an r d, we will see what happens when r d is included what happens when r d is not included, and I find it convenient to leave all complicated matters to students so including the effect of r d I will ask you to calculate yourself, we will have occasion to look at this. And in this particular case in this particular example that we took, r d cannot be ignored and we shall see in a moment, that we shall do it we will make a rough calculation. From the drain then we have 2 resistances R sub D and R sub L, this is I 0 and this voltage is V 0 alright. Now you see look at the circuit it is said that if you can observe a problem carefully, half of it is solved.

If you observe this circuit carefully the calculations will be very simple, g m V gs now no longer supplies only the parallel combination of R D and R L and small r d, small r d is not in parallel at all so this current source must supply 2 parallel paths; one is r d and the other is the parallel combination of R D R L and in series with R Sigma okay, if you recognise this fact then the calculation including the effect of r d shall be simple but we will find it convenient to ignore it.

Student: Sir (())(30:43)

It supplies... You see across g m V gs there are 2 resistors; one is r d and the other is R D parallel R L + R Sigma okay because these points are the same these points are the same they are all ground, so what I have is R D parallel R L + R Sigma. If you recognise this is the only single fact that has to be recognised to include the effect of r d. Now can we ignore the effect of r d in this case? r d was given to be 100 K, the parallel combination of R D and R L is 7.5 K and this is 15 so the parallel part is 22.5 K approximately one fifth of this part because the current shall be varying into the same ratio 1 is to 5 is that clear?

Student: Yes, how does g m V gs provides current to r d?

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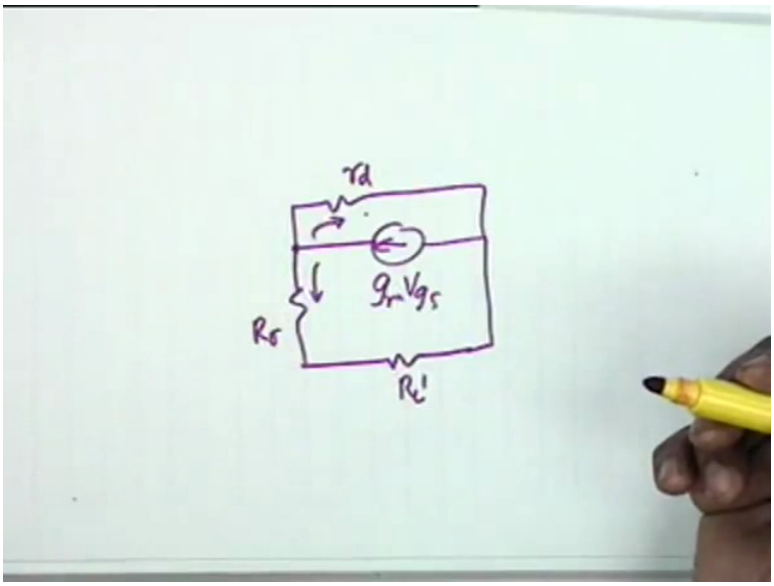

Oh there is a current source let me draw this, g m V gs which is in parallel with small r d okay, this point then we have R Sigma + R L prime therefore this current has 2 paths; one is through this and the other is through this, is not that right this current after coming here where can it go, it has to flow like this and like this. Now if this part was very low resistant as compared to small r d you could have ignored small r d, but the current now divides into approximately 1 is to 5 alright so we cannot ignore r d but we will make our calculation excluding r d and leave r d effect to you.

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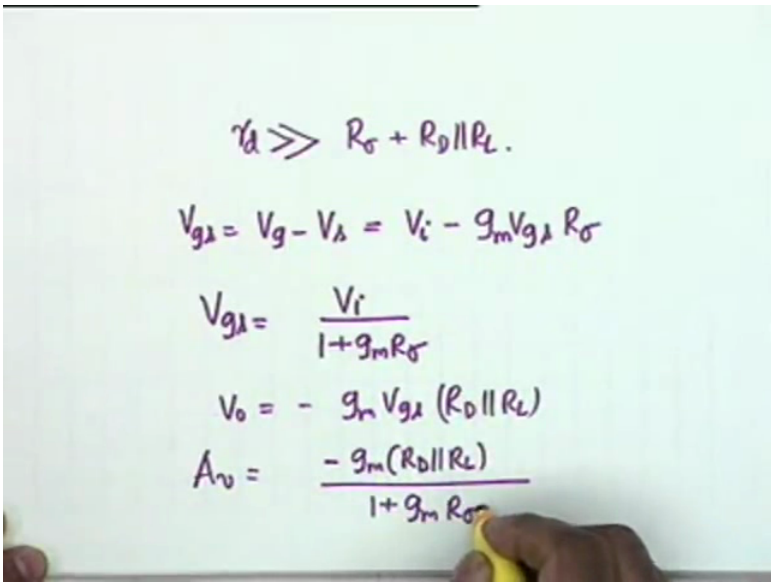

So we assume that r d is much greater than R Sigma + R D parallel R L okay, we assume we have derived our formula by assuming this. If that is so then you see then you see that V 0 is simply – g m V gs multiplied by R D parallel R L so on that 1st thing found out is V gs, let us see what V gs is. V gs is V g – V s that = V g is V i right V g is V i and V s is if we ignore small r d then g m V gs flows through R Sigma therefore it would be simply g m V gs multiplied by R Sigma okay, this is an involved equation V gs occurs in the right side and also in the left side so you can find out V gs as = V i divided by 1 + g m R Sigma agreed, this is how V gs has to be found out. And once V gs is found out, V 0 is – g m V gs R D parallel R L and therefore the voltage A sub v shall be = – g m R D parallel R L divided by 1 + g m R Sigma.

What was g m in the previous example? 0.8 millimho and R Sigma was 15 K so this is 12, is that right? 12 is much larger compared to 1 by approximately the gain would be, if g m R Sigma is much greater than 1 then approximately the gain would be – R D parallel R L divided by R Sigma. You recall we had a similar formula in the case of a common emitter amplifier with unbypassed R E, the inverse approximately negative of the ratio of the effective load to R E, it is the same formula that applies here okay.

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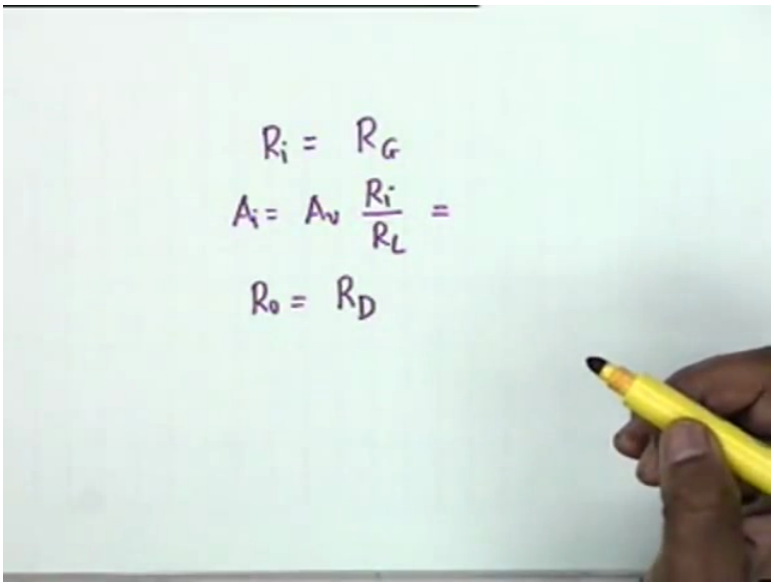

What is R i? Input resistance, it = R sub G agreed and A sub i can be calculated as A v R i divided by R L in the usual manner you can write the expression. What is R 0? If small r d is ignored then R 0 is simply R D but if it is not ignored then complications arise and you have to solve a circuit, let me indicate the circuit the solution would be left to you.

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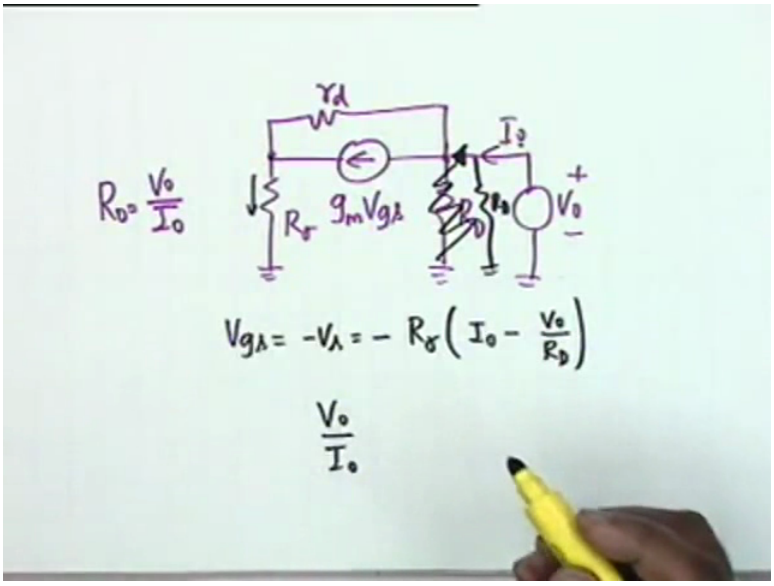

What you have to do is we have an R Sigma then g m V gs okay g m V gs alright parallel r d and there is a resistance R subscript D, you have to correct a voltage generator here and the current I

0 has to be found out. R 0 would not be = V 0 by I 0 alright, but what is V gs? – V s okay. And what is – V s? This is minus, what is the current flowing through this?

Student: V 0 by R Sgima.

Professor: No.

Student: V 0 by R D + R Sigma.

Professor: It is R Sigma multiplied by what is the current that is what we want to know... In terms of I 0 V 0, if it is I 0 – V 0 by R D alright so you know everything now in terms of I 0 and V 0 and that way you can find out V 0 by I 0, is the point clear? No, alright let me draw this resistance here R D then this current must flow through the R Sigma, this current after this current is I 0 – V 0 by R D this current this current this one. This current splits up in the 2 parts; one is through this, one is through this, they must combine here and flow through R Sigma it was a little bit of thinking but it is not difficult so you can find out V 0 by I 0 and I leave this to you.

"Professor–student conversation starts"

Student: Sir but out of this V 0 by I 0 will also go into small r d.

Professor: Whatever it is whatever this current is, these 2 currents again combine here and flow-through R Sigma okay, any questions?

Student: Sir what happens to g m V gs?

Professor: Oh this is what we have found out, g m V gs will be – - g m R Sigma times I 0 – V 0 by R D, everything now in the circuit shall be in terms of I 0 and V 0, which current source?

Student: Sir is it not contributing current to R sigma.

Professor: Let me draw this circuit again, now I shall try in a different manner.

"Professor–student conversation ends"

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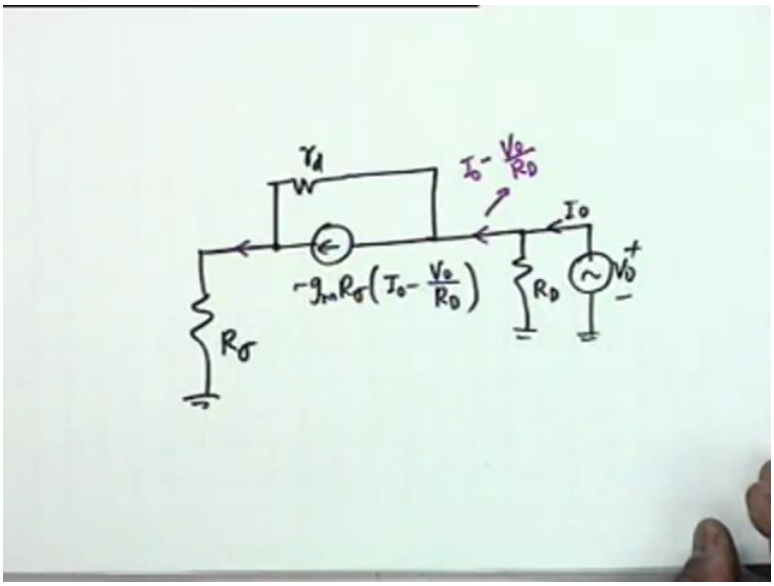

This will be – g m R Sigma I 0 – V 0 by R D, there is an R D here, this is V 0, I 0 and this goes to R Sigma alright. So whatever current comes here whatever current comes here must flow here, there is no other way. And what is this current? This is simplyI 0 - V 0 by R D this is what I have substituted for V gs, V gs is – – R Sigma multiplied by this current okay, any other doubt? I assume this is correct, I have not made any mistake yes oh sure I have all the time in the world, you must give me a signal when you are through. We shall then consider the same example that we have considered for the CS amplifier with C Sigma tends to what? The previous example tends to infinity that is R sigma short-circuited.

Student: Sir can we have the formula for R 0?

Professor: No I have not derived it therefore you have to derive it yourself.

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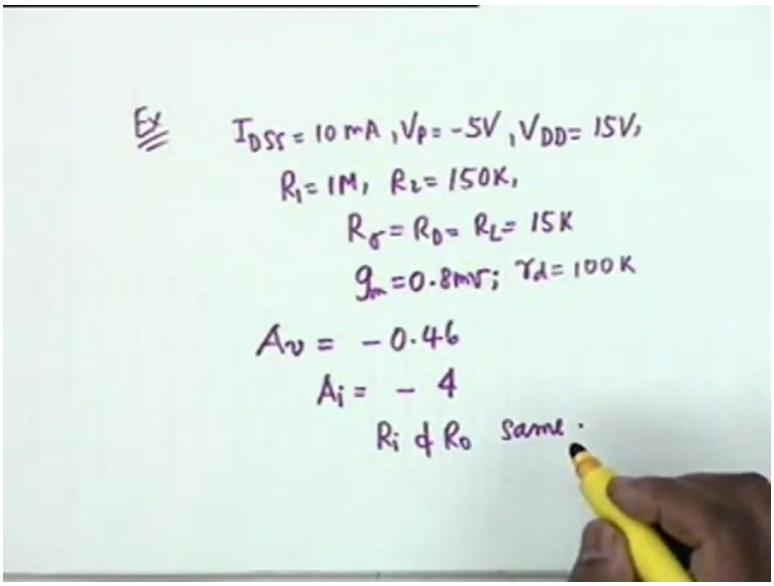

Consider the same example, what was the example? I DSS 10 milliampere, V P is - 5 volts, V DD is 15 volts, R 1 is 1 megh, R 2 150 K, R Sigma = R D = R L = 15 K. Small r d if it is 100 K then obviously all our calculation will be approximate okay. Nevertheless I give you small r d and I ask you what to find what modification is needed, we have already seen the modification, in the calculation output resistance all that you have to do is to split this current g m V gs that is about it okay so it should not be very difficult, small r d is 100K. If you calculate will the Q point change? No, because everything has remained the same, Q point does not change. If Q point does not change, gm does not change g m is the same g m is also same as 0.8 millimho

And if you utilise these formulas then you get A v do not depend on formulas unnecessarily, where you can see the formulas see it rather than committing to memory okay. If you if you calculate it is simply – g m the effective load divided by, this divided by comes because C Sigma = 0, divided by 1 + g m R Sigma and that becomes - 0.46 I will skip the arithmetic, A sub i becomes - 4 now you see A v the voltage gain now becomes less than 1 this is what the un-bypassed emitter source resistance does to the amplifier. The current gain is - 4, R i and R 0 are not changed they are the same as in the previous case okay done, let us take the common gate amplifier. You will see that the calculation is very similar there is no difference except that we have to be bit careful about the calculation of g m and the output resistance, it is the output resistance which is the complicated calculation.

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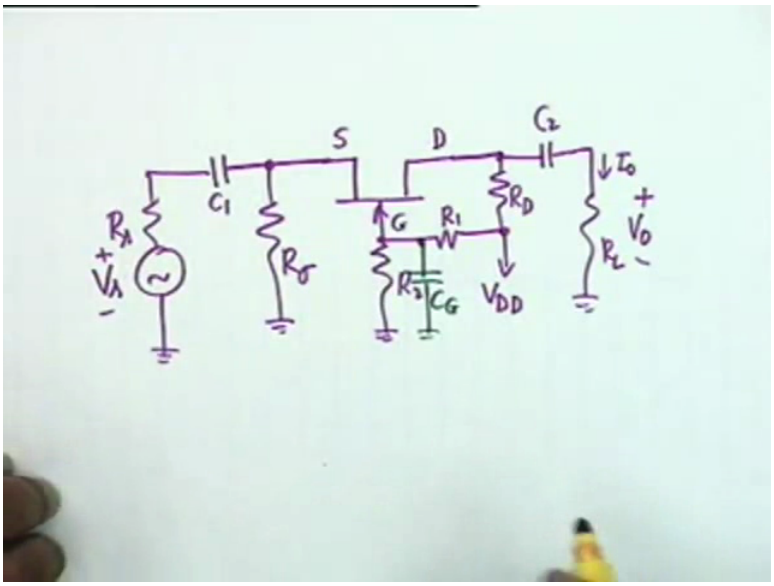

Now in a common gate amplifier CG which is equivalent to CB of BJT, you have V s, R s, capacitor C 1 started on a wrong foot so let us change the page. We have first let us draw the FET, this is the source this is the gate and this is the drain. Now in order to bias those in order to bias the source we require a resistance R Sigma and we cannot bypass it now, we cannot bypass it. In order to put a gate voltage we must have a resistance R sub 2 and we must supply it to the V DD okay, from the drain we have the resistance R D this is R 1 and should go to + V DD. From here you take the coupling capacitor and take the load R L, the voltage is V 0 the current is I 0 and for reasons that I had stated in the case of common bass amplifier R 2 must be bypass.

In other words there must be a capacitor here CG okay there must be a capacitor here which bypasses R 2 to ground but R 2 is effective in DC inserting the DC operating point. Then your input is applied through a coupling capacitor and a source resistance R s and a voltage source V s and this goes to ground alright. Now things will get little complicated because of r d why? It can be very easily ignored in a BJT, you have to be very in FET. As I said in the last analysis in the last example that we took our figures were very rough because small r d was not negligible compared to the parallel combination of R D R L and in series with R Sigma okay that makes me happy, now let us see what is the equivalent circuit is.

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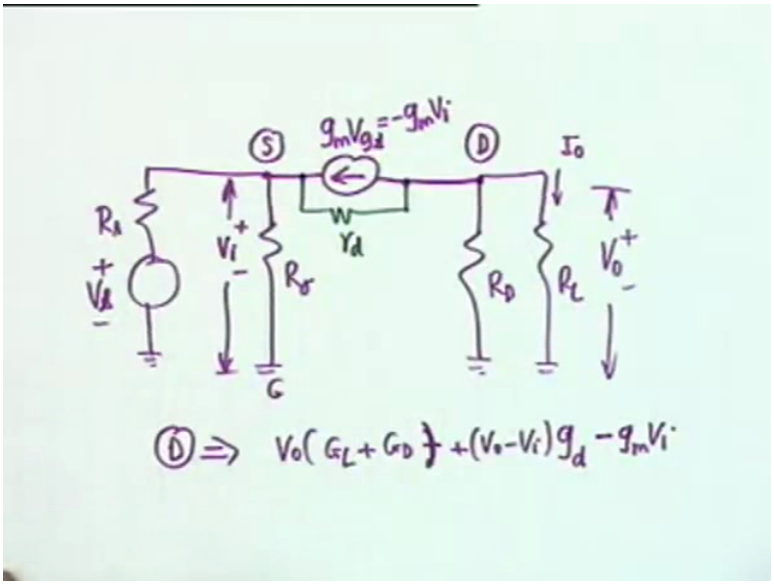

We have R s, V s AC equivalent circuit, then you have the source node from which you have an R Sigma and this voltage is V i okay, and this comes to from the drain to the source the gate is common gate is grounded, from the drain to the source you have g m V gs, what is V gs =? – V i, is that clear? This is the gate G so V gs is from this point to this point which is of opposite polarity to V i but magnitude is the same so I could write this in – g m V i this is a simplification occurring immediately. And then you have this (())(47:29) of r sub d the dynamic drain resistance. And from here you have the R D and R L and this is V 0 and this is I 0 okay, the things are not too bad as far as the equivalent circuit is concerned because there are only 2 nodes.

Not only that since we are finding out the gain, again is a relationship between V 0 and V i, you can write the note equation at D in terms of V i and V 0 nothing else. As you can see note equation of D is V 0 G L now I take conductance, it becomes simpler to do it that way, G L + G D +... then V 0 – V i divided by R D so + V 0 – V i multiplied by g d okay is that current through r d. Then I have this extra term – g m V i okay this is the node equation and the node equation contains only V 0 and V i why this? I have to add this current, this current and this current and this current, this current is g m V gs which is – g m V i okay.

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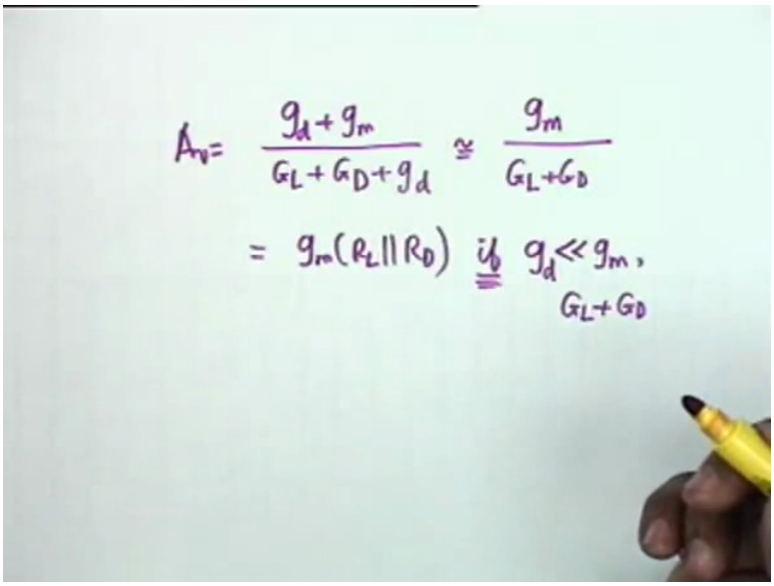

So since this equation contains only V 0 and V i, it is very easy to find out the voltage gain and the expression is g d + g m divided by G L + G D + g subscript d and if r d could be ignored if it could be ignored, wishful thinking it will should have been approximately g m divided by G L + G D, do not you see that this is same as g m R L parallel R D, is this obvious? 1 by G L + G D conductance is add so the 2 resistors are in parallel. This is also obvious for the equivalent circuit okay equivalent circuit never tells a lie, if r d is ignored if it is infinity then this current has to flow through this and that is the voltage gain, it is only because of r d that we have to write a node equation at the node D otherwise we do not have to okay.

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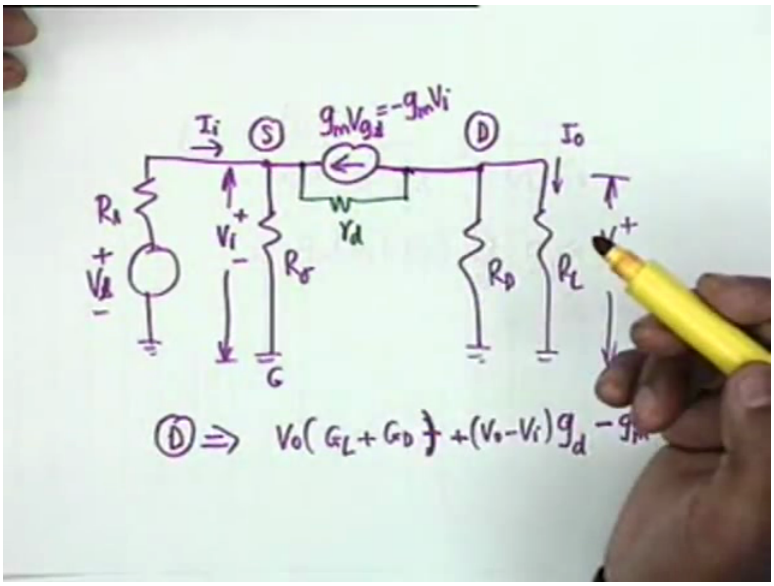

If a big if g d is much less compared to g m as well as G L + G D if this is true then this will be approximately the story. If you want to find out the input resistance, now the input resistance is also complicated by the occurrence of r d okay and the occurrence of – g m V i the input resistance is no longer R Sigma no okay. To find the input resistance all I need is the ratio of V i to I i okay, and therefore what I can do I can write node equation at the node s, if I write that at the at the node s, I i is coming, g m V gs is coming, g m V gs is – g m V i, this current will be going of V i by R Sigma and current to r d which is V 0 – V i multiplied by G D okay. Now the complication is that in this node equation you have V 0 but you know what is V 0 by V i we have already calculated V 0 by V i and therefore it is not difficult.

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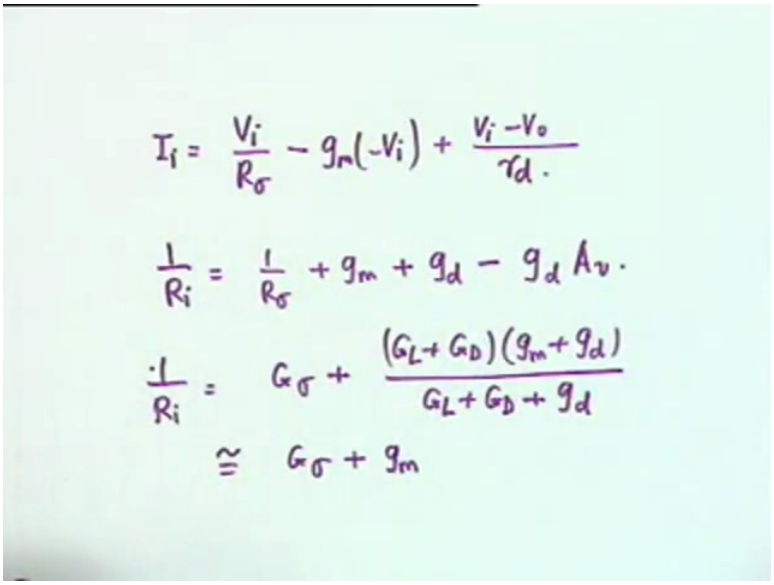

The equation that we get is if you see it is V i divided by R Sigma is the current that is going – this current leaves, the current coming is g m V gs so this is g m – V i is the current generator + V i – V 0 is the current gain divided by r d. Now what we do is we divide by V i then you get 1 by R i as = 1 by R Sigma + g m then + g d – g d times A v that is right, now you substitute for A v and simplify. The expression that I get it is a bit of algebraic simplification, not very complicated, you get 1 by R i as = G Sigma + G L + G D, this requires a bit of algebraic simplification as I have said, g m + g d divided by G L + + g d that is what I get. And once again if your wish comes true that if g d is negligible compared to g m and G L + G D, do not you see that it is simply G Sigma + g m agreed.

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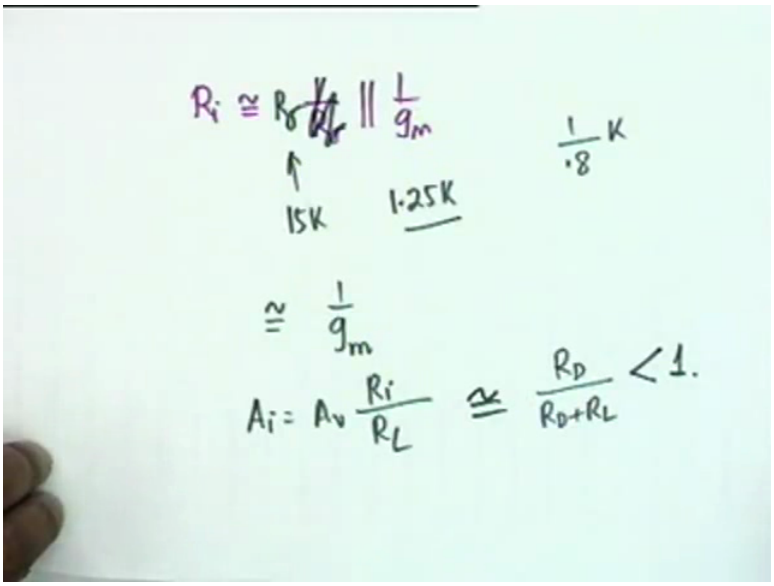

Which means that R i is the parallel combination of R Sigma and what else? 1 by g m okay, let us let us see this. R i is approximately the parallel combination of R Sigma and 1 by g m, in the example that we took what we was what was I am sorry I made a mistake because someone looked back, do not look back. R Sigma parallel 1 by g m okay, what was R Sigma in our example? 15 K, and 1 by g m is 1 by 0.8 K which is 1.25, do not you see that R Sigma is large compared to this and therefore this is approximately = 1 by g m. If you recall in the common base amplifier this was exactly the same story except that 1 by g m is now not as small as 25 ohms, in the previous case it was some 25-24 or 25 ohms, this is now 1.25K this is a generic story alright.

And finally of course A i can be calculated from A v R i divided by R L we have found out the expression but I can mention that under this condition r subscripts d very large, this is approximately R D divided by R D + R L so the gain is current gain is less than 1, it has to be in a common base case this was also true. As far as R 0 is concerned, the output resistance is approximately = R D if small r d goes to infinity, if this is not the case then I am afraid you have to calculate this from this equivalent circuit.

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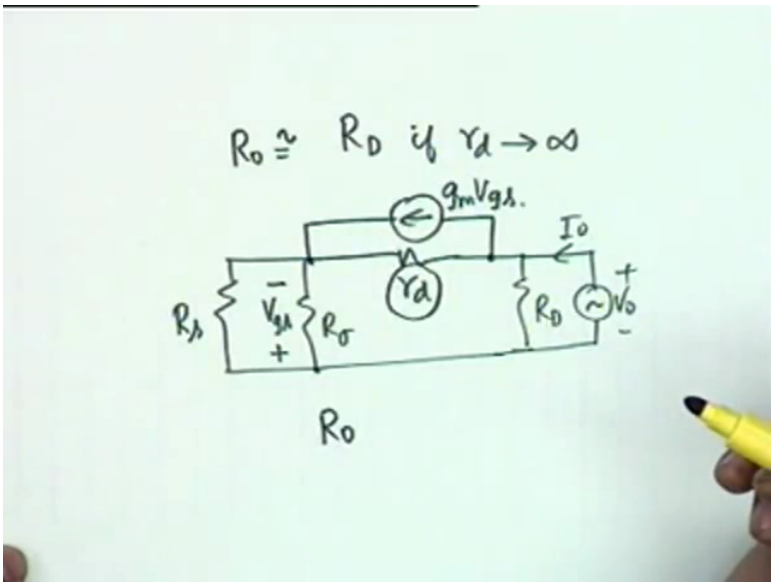

R s, R Sigma, r d, g m V gs, where is V gs now? V gs occurs across R Sigma and in what polarity? – up and + down agreed, so this is V gs, this is g m V gs, it is not difficult to calculate, then you have an R D and I 0 and V 0, please do carry out these calculations okay and find out what is R 0, how does r d effects of check on this calculation would be that if you put r d = infinity the value should be capital R D that would be the check and this is a good point to stop, next time that is Thursday we will work out some problems and we will also look very briefly at the common what is remaining... Common drain Common drain FET amplifier.