Fundamentals of Power Electronics
Prof. L. Umanand
Department of Electronics Systems Engineering
Indian Institute of Science, Bengaluru

Lecture – 75
Half bridge converter

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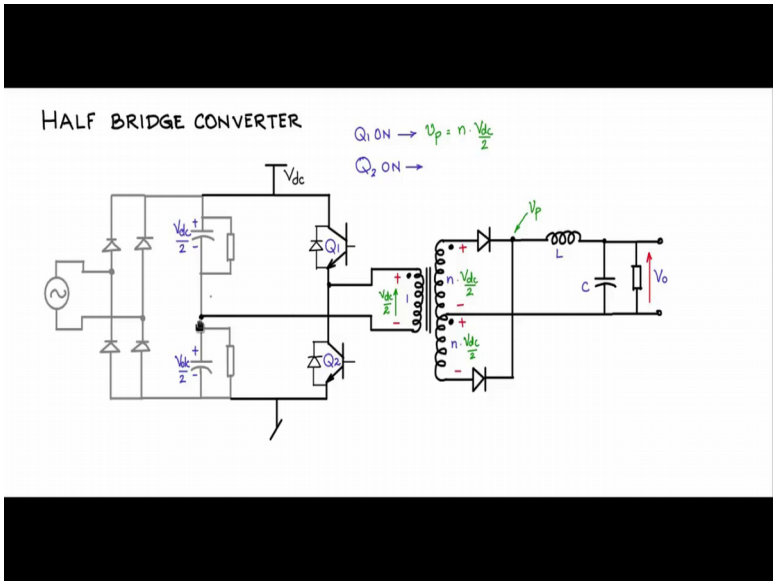

The half bridge converter like the push pull converter is also a buck derived converter, where the secondary side of the half bridge converter transformer is center tap and behaves exactly like that of the push pull secondary stage. The only difference comes in the primary side. So, let us consider where the half bridge converter differs with respect to the push pull converter. I am drawing here a sign source ac source rectifier and a capacitor filter. This is the ac to dc conversion where you have a ac source you have a rectifier and a capacitor filter. This we have studied, but I want to make use of this I am showing this ingratiate.

I will remove the capacitance and split the capacitor into two capacitors and I will have balancing resistance there so, that the voltage division is proper. Capacitances being equal you can expect Vdc by 2 to into b across the top capacitor and another Vdc by 2 across the bottom capacitor. So, if you use this as the dc link for the switch mode converter circuit, the half bridge configuration looks like this. So, I pulled this out and called this one as Vdc and I will put this half bridge on like this.

So, you have two transistors or mosfets or IGBTs in this fashion and across this center here this is Vdc by 2 point and we will put across the center winding and this winding of course, the primary of a transformer. Secondary of the transformer is center tap and you have two diodes in this fashion just like in the case the push pull and with respect to the center tap you have this inductor and the capacitor and the output load.

So, behavior of the secondary side of the circuit is exactly same as the push pull. So, I am just putting in freewheeling diodes body diodes across the switches for completeness, you have the dot polarities in this fashion and this is the pole voltage V p. So, let us say you have 1 is to n in this fashion L C V naught the output voltage.

So, let us say when Q 1 is ON. So, when Q 1 is ON Vdc is connected to the dot end. So, dot end is positive with respect to the non end non dot end is connected to Vdc by 2. So, what you have here is plus minus in this fashion dot is plus dot plus and non dot end minus and the amplitude across the primary is Vdc by 2 because this is at Vdc connected to Vdc and the non dot n connected to Vdc by 2.

So, totally you have Vdc by 2 appearing across the primary. This transferrers to the secondary n time so, you have n times Vdc by 2 on the both halfs of the center tapped secondary. Now dot the dot end is positive so, this diode here the top diode will be active and the bottom diode is reverse biased and Vp will be n times Vdc by 2.

So, likewise we can also evaluate for Q 2 ON that is Q 1 is off and Q 2 is ON, and during this time you see that the dot end is pulled to the ground and the non dot end is connected as usual to Vdc by 2.

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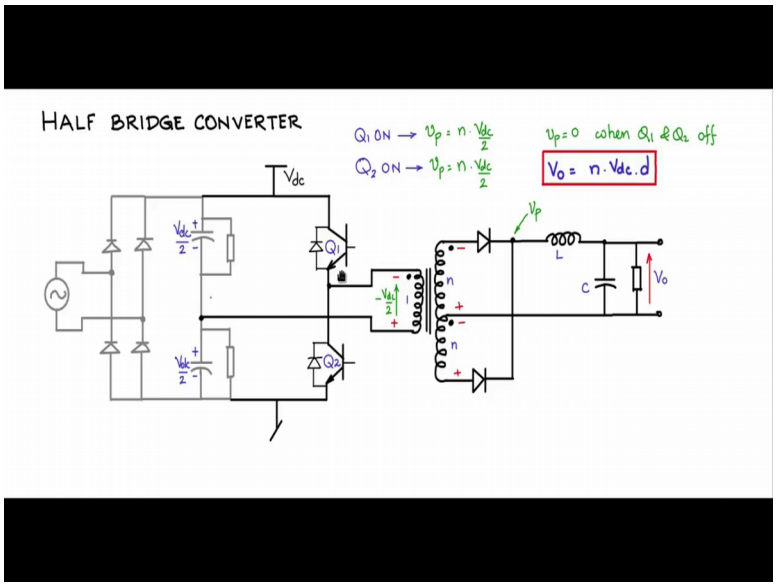

So, let us mark. So, the non dot end is positive, dot end is connected through Q 2 to ground minus so, non dot end is plus dot end minus like this. So, if we measure across the primary you have minus Vdc by 2 appearing over the primary, secondary likewise Vdc n times, V dc by 2 and n times Vdc by 2 here with the polarity are shown this diode the bottom diode is active and Vp is again seeing n times V dc by 2 just like in the push pull case.

All other operations on the secondary is same you have periods of time in both Q 1 and Q 2 both are off under that condition L is freewheeling through the secondary equally dividing between the top half of the center tap and the bottom of the center tap the mms cancel and d phi by dt is 0 and you have voltages across all coils being 0 at which point the center point is at Vdc by 2 and the voltage that is across both the halfs; across both the switches will be Vdc by 2.

So, therefore, Vp is equal to 0 when Q 1 and Q 2 are off and what is V naught? V naught is related to the Vp voltage which is equal to n times Vdc by 2 into 2 d here, again there is an oring effect here, the d is a switching the duty cycle of the switching off the switches in a period t s, but because the oring effect Vp waveform has a period of ts by 2 and therefore, the duty cycle of Vp waveform is 2 d.

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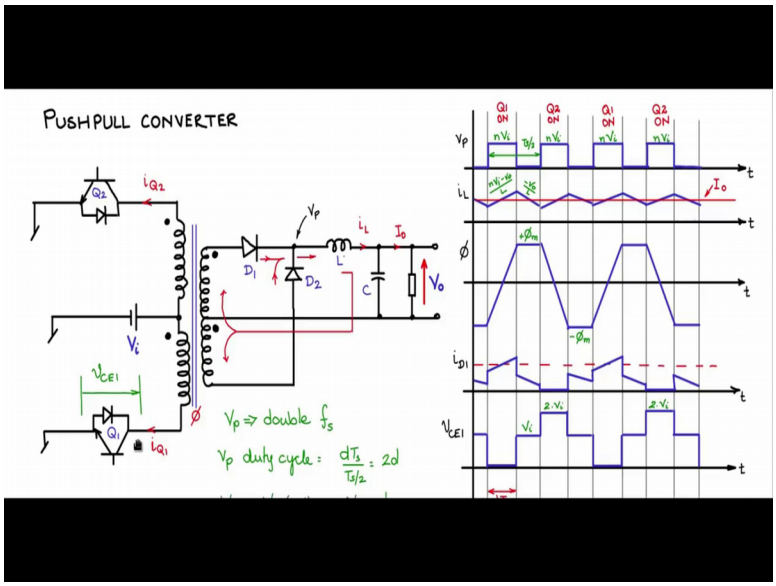

Now, I will put that 2 d here 2 and 2 will cancel of and then you have V naught is equal to n Vdc into d. So, V naught is equals to n Vdc into d is the input-output relationship for the half bridge converter. Here one important point to remember as in comparison with the push pull is that, in the case the push pull; in the case of the push pull we saw the voltage across the device, you see the voltage across the device is ON whenever the switch is ON and when the switch when the others which is ON, complementary switch is ON you see you see 2 times Vi coming across the switch.

So, whenever both the switches are off you see v i coming across it. So, the maximum voltage that each switch has to support is 2 times Vi. In the case of the half bridge converter the voltage across each of the switch max is Vdc or Vi. So, when the bottom switch Q 2 is ON, then you see that this point the dot end point is at ground and therefore, Q 1 which is off will have to with stand Vdc. In the case when Q 1 is ON you will see the bottom which is off. Then this point here dot end point is at Vdc and Q 2 will have to withstand maximum Vdc. So, that is the difference the push pull the devices have to be rated twice Vdc, in the case the half bridge the device have to be rated at just Vdc. So, you have half the voltage rating requirement for the half bridge converter that is an advantage.

Another problem in the half bridge converter like in the case of the push pull converter is that of flux walking. You will see that in the case of the half bridge converter the primary side is not center tap, but a single winding.

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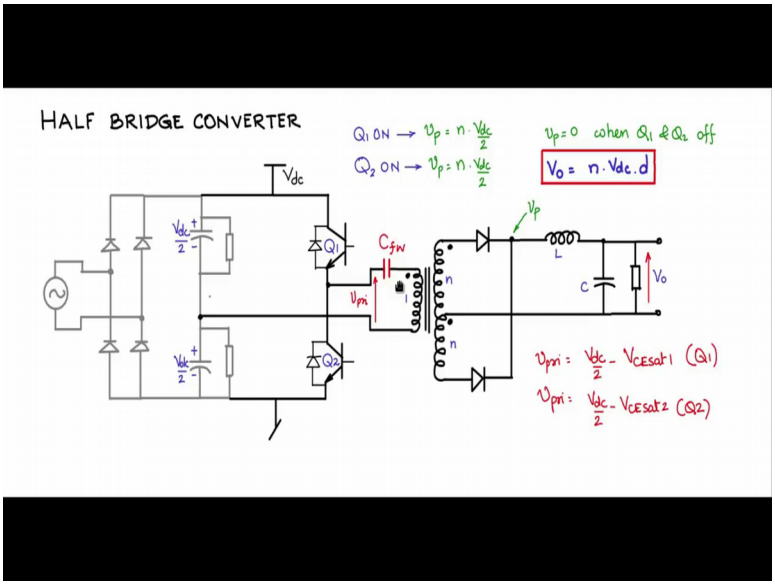

So, let us look at the flux walking problem in the half bridge converter. So, let say this V primary voltage across the single winding in the primary and let us look at that primary voltage when Q 1 is ON and Q 2 is ON.

So, V primary is equal to Vdc by 2 minus V CE sat 1 when Q 1 is ON. See normally when Q 1 is ON Vdc comes to the dot end and the non dot end is connected to Vdc by 2 here at the midpoint of the capacitance. So, the voltage across the primary V primary will be Vdc by 2, but in a practical case because of the drop across Q 1, you will see Vdc by 2 minus V CE sat 1 coming into the picture.

Now, the other condition when Q 2 is ON Q 1 is off. So, when Q 2 is ON you will see that the on state drop of Q 2 comes into the picture and therefore, V CE sat 2. And we know that V CE sat 1 and V CE sat 2 is not same is not matching it will not be equal in a practical case and therefore, there will be a difference between the primary voltage when Q 1 is ON the primary voltage when Q 2 is ON and because you are applying dts for Q 1 and dts ON time for Q 2, the difference between V CE sat 1and V CE sat 2 will reflect in an average primary voltage very small average primary voltage. And because of the

Faraday's law v average which is equal to n d phi by dt phi when you integrate the voltage, phi will be proportional to time t and it will gradually increase.

So, as a consequence you will see that the average flux will start rising and then ultimately reach the saturation flux limit and saturate the core of the half bridge converter. So, how do we solve this? Like in the push pull converter we can use the same method of adjusting the duty cycle of Q 1 and Q 2.

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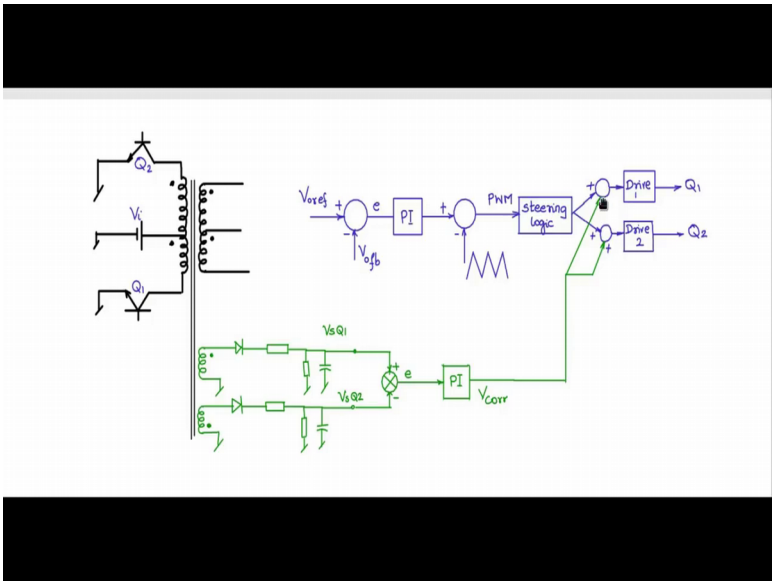

In the case of the push pull convertor we had to sense windings, one sensing the Q 1 part of the volt second, in the other sensing the Q 2 part of the volt second and these 2 are subtracted the error the difference e was passed through a PI controller; down to the PI controller developed the correction voltage and that was used for correcting the dts or the ON times of Q 1 and Q 2 respectively. In such a way that e becomes 0 and if e become 0 then the volt second of the top part that is when Q 1 was ON the old second of the bottom part when Q 2 was ON would match and thereby achieve the 0 flux average and thereby avoid flux walking.

Now, this technique can also be used for the half bridge converter and the Q 1 and Q 2 duty cycle can be adjusted. In the case the half bridge converter there is yet another way to achieve this achieve solution for the flux walking problem that is by placing another component that is placing a capacitor in series with the primary winding. The advantage

here is that the primary voltage across the center tap here if it develops an average, it can drop across the capacitance.

There are two components here the coil cannot with stand an average value, but the capacitor is capable are having an average value and therefore, the average value will drop across that and thereby save the coil from having any average. And this way the flux in the core will not walk away and the flux will not saturate.

So, this is a nice solution and this capacitor is called the flux walking capacitor Cfw. Normally, the Cfw is rated for around 10 percent of Vdc, though the voltage that comes across the flux walking capacitor will not be so high, it will be much much lesser. The one nothing that one should remember you that this Cfw the flux walking capacitor should be bipolar should be capable of having current flow in both direction and the voltage in both direction, voltage drop in both direction.

And another aspect is that the entire load current will flow through the flux walking capacitor and therefore, the arms rating of the flux walking capacitor must be high, and this will make the flux waling capacitor costlier. However, this is a nice solution especially if it is for low power circuits.