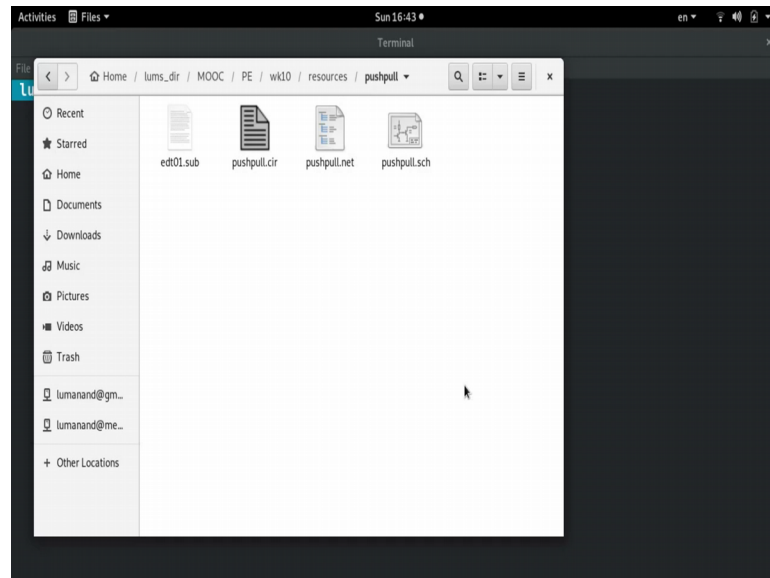


**Fundamentals of Power Electronics**  
**Prof. L. Umanand**  
**Department of Electronics Systems Engineering**  
**Indian Institute of Science, Bengaluru**

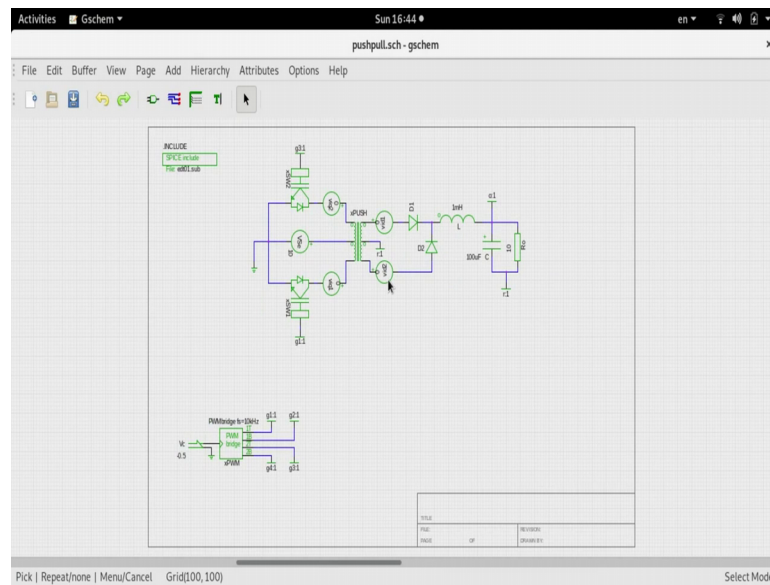
**Lecture – 74**  
**Stimulation of pushpull convertor**

(Refer Slide Time: 00:27)



Let us, now do the simulation of the push pull converter. I have here in the folder in the resources, I have a push pull folder; push pull schematic is here, push pull net list, push pull dot cir, and the edt 01 dot sub which contains the sub circuit files.

(Refer Slide Time: 00:54)



So, let me double click on this; so, you have the schematic, this is the complete schematic of the push pull converter. You see the push pull transformer here, the primary side is center tap, the secondary side is also center tap. There is this switch I have used generic switches this is q 1 and this is q 2 switch 2. I have placed here a zero voltage source to sense the switch current.

I have placed another zero voltage source here to sense the q 2 switch current. Let me expand that, so, here you see the push pull circuit, and on the secondary side which is center tap. The center tap is the reference node and to the dot from the dot end you have a diode D1 or in at this point with diode D2 which is coming from the non dot end.

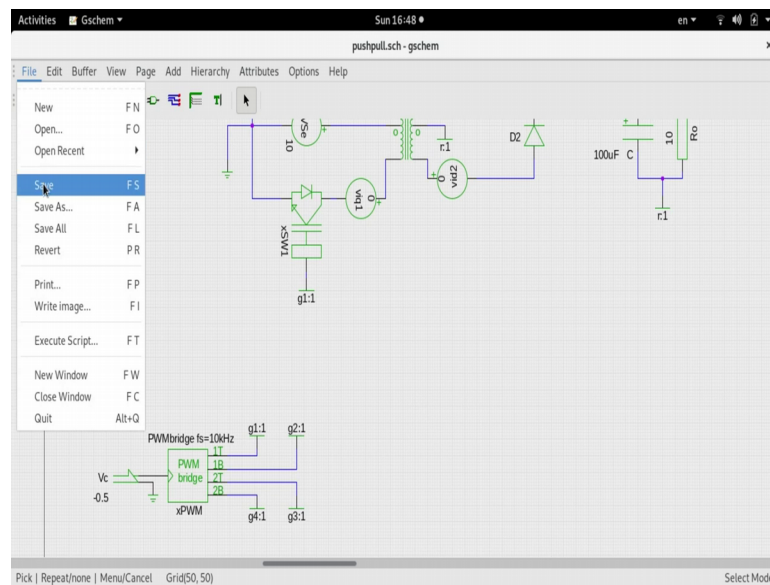
And that is passed on the inductor, capacitor and R naught load, they are all connected to the center tap reference node. I will label the node here the output node o, I have labeled the gate drive node as g 1 and g 3 here. I will tell you how I am getting that, and probably we can label a node here for the pole voltage vp, so, you have the node vp here.

Now, edt01 sub is included here; and all the sub circuits x, starting with x, x push the push pull transformer, the switches. They are all modeled in this edt01 dot sub, they have the sub circuit models which we can use. Then down here, I have a PWM bridge which will which will generate 4 outputs, this can be used even for the full bridge.

Therefore, I have made a generic PWM bridge block which will connect to arm 1 top switch, arm 1 bottom switch, 1T and 1B, arm 2 top switch, arm 2 bottom switch. This is the label that I have given and here you have the control voltage, I given it as minus 0.5 comparing with a triangular wave form which is going from minus 1 to plus 1.

So, this will correspond to 25 percent switch duty cycle. So, I am using g1 as one of the PWM signals and for q 2 I am using g3 as the other PWM cycle as the PWM signal, these two are mutually exclusive.

(Refer Slide Time: 04:21)



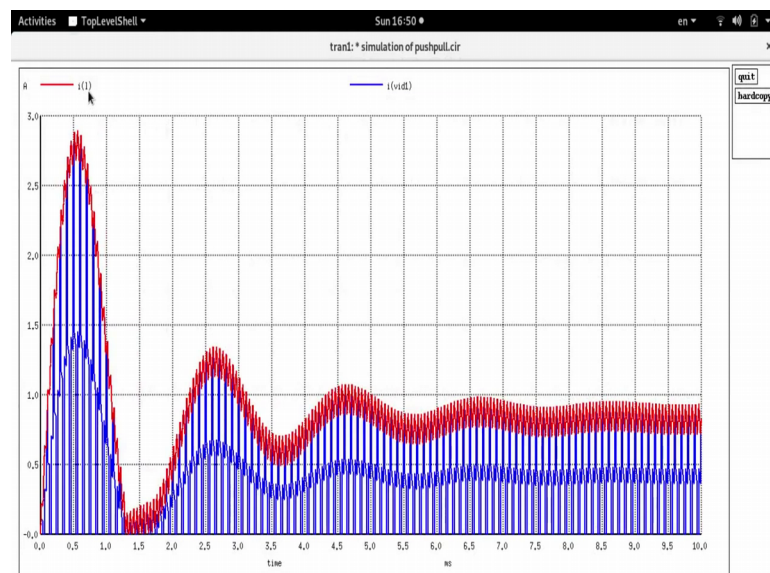
So, let me save the schematic.

(Refer Slide Time: 04:24)

```
Activities Terminal Sun 16:50
Terminal
File Edit View Search Terminal Help
Lums ... > wk10 > resources > pushpull gnetlist -g spice-sdb -o pushpull.net pushpull.sch
Loading schematic [/home/lums/lums dir/MOOC/PE/wk10/resources/pushpull/pushpull.sch]
Using SPICE backend by SDB -- Version of 4.28.2007
schematic-type = normal schematic
Found unknown component. Refdes = vid2
Found unknown component. Refdes = vid1
Found unknown component. Refdes = viq1
Found unknown component. Refdes = viq2
Found unknown component. Refdes = xSW2
Found unknown component. Refdes = xSW1
Found unknown component. Refdes = xPWM
Found unknown component. Refdes = xPUSH
Found unknown component. Refdes = L
Found unknown component. Refdes = C
Found unknown component. Refdes = Ro
Found unknown component. Refdes = .INCLUDE
Lums ... > wk10 > resources > pushpull ngspice pushpull.cir
```

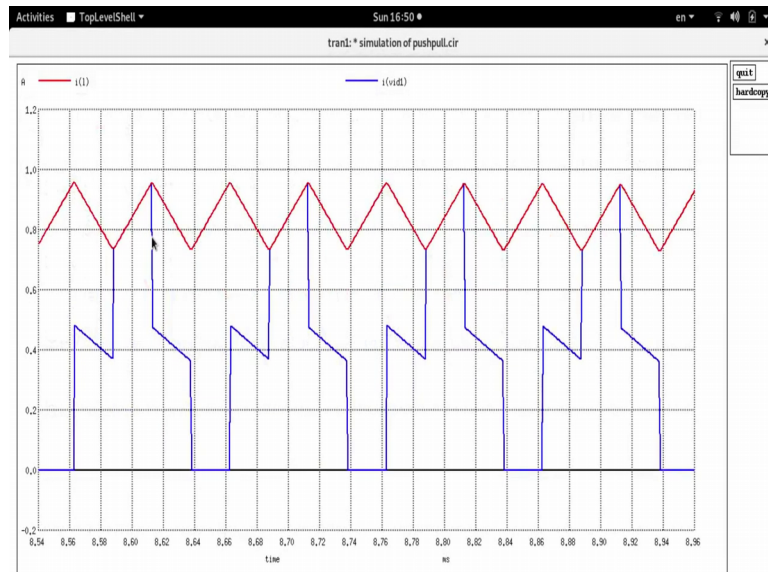
I have now opened the terminal, and let me make the net list file push pull dot net from the push pull dot schematic file. And then stimulate the push pull dot cir file in the spice.

(Refer Slide Time: 04:48)



So, on simulation you will see the waveform I have plotted the waveform inductor current waveform  $i_l$ . And the diode  $d1$  waveform, because the diode waveform are very unique. And therefore; so, it reaches steady state here around somewhere here. Let me zoom this expand this portion, let me see few cycle here you see.

(Refer Slide Time: 05:19)



So, you see that this is the inductor current waveform. So, and the diode D1 wave form, it follows the inductor current during this period when q1 is on. And during the period when both are off there is a freewheeling half of these free wheels through this diode and the other half will free wheel through diode D2.

So, the blue waveform is the diode D1 current waveform. If you look at the schematic, the output waveform is between o and r and the pole wave form is between p and r. We can see the pole voltage waveform and the output voltage waveform.

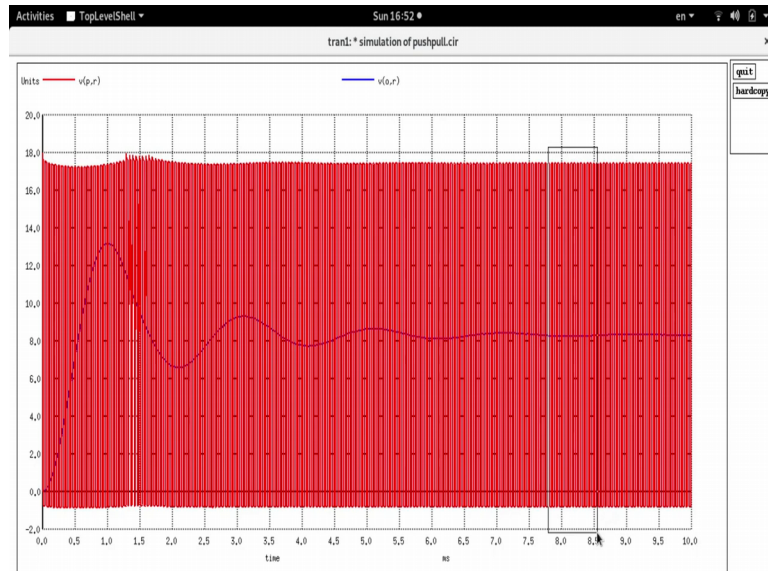
(Refer Slide Time: 06:03)

```
Activities Terminal Sun 16:52
Terminal
File Edit View Search Terminal Help
b.xpush.xgyp1.bgpl#branch 0
v.xpush.xgyp1.vsl#branch 0
l#branch 0
vse#branch 0
vc#branch 0
viq2#branch 0
viq1#branch 0
vid1#branch 0
vid2#branch 0
a.xpwm.ainv#branch_1_0 0
a.xpwm.alim4#branch_1_0 0
a.xpwm.alim3#branch_1_0 0
a.xpwm.alim2#branch_1_0 0
a.xpwm.alim1#branch_1_0 0
a.xpwm.acompare2#branch_1_0 0
a.xpwm.acompare1#branch_1_0 0
a.xpwm.atri1#branch_1_0 0

Reference value : 5.28600e-03
No. of Data Rows : 10548
ngspice 168 -> Warning: Missing charsets in String to FontSet conversion
ngspice 168 -> plot v(p,r) v(o,r)
```

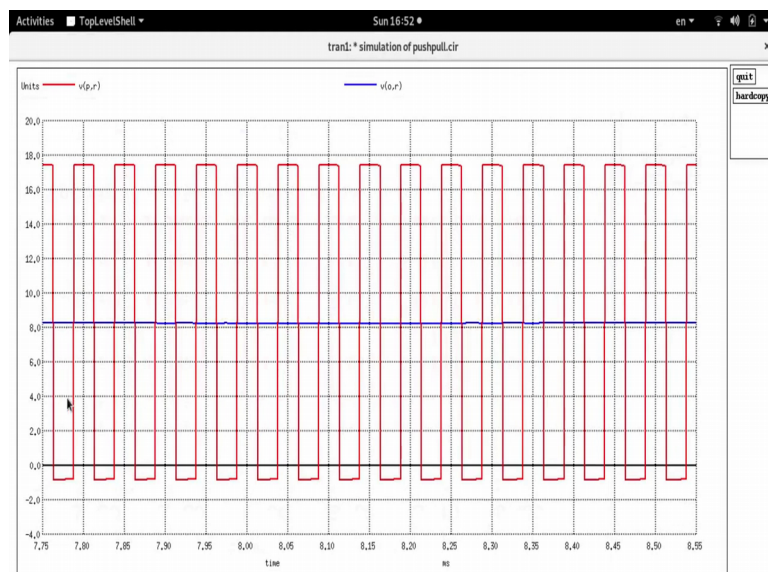
Going back to the NG spice environment, I will plot voltage; the pole voltage waveform with respect to the reference node r, output voltage waveform with respect to the reference node r. And we will see what we have, let me explain that.

(Refer Slide Time: 06:19)



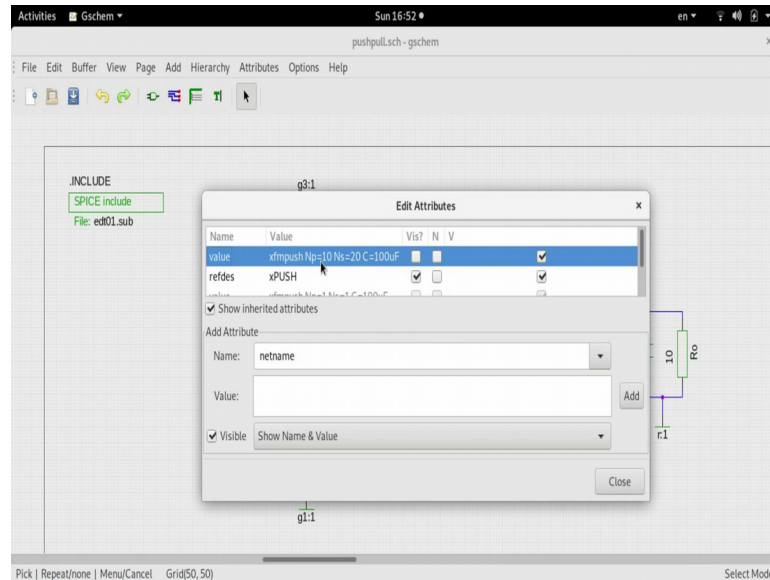
And you see that you have the output voltage waveform and the red one is the pole voltage waveform. I will show few cycles here on the; when it has reached steady state yes.

(Refer Slide Time: 06:39)



So, you see the output voltage blue wave form, and the pole voltage waveform. A negative is due to the diode freewheeling, and this is  $n$  times  $v_i$ . So,  $n v_i$  here which is  $n$  we have set it at 2, I have not shown you that one, let me show you this.

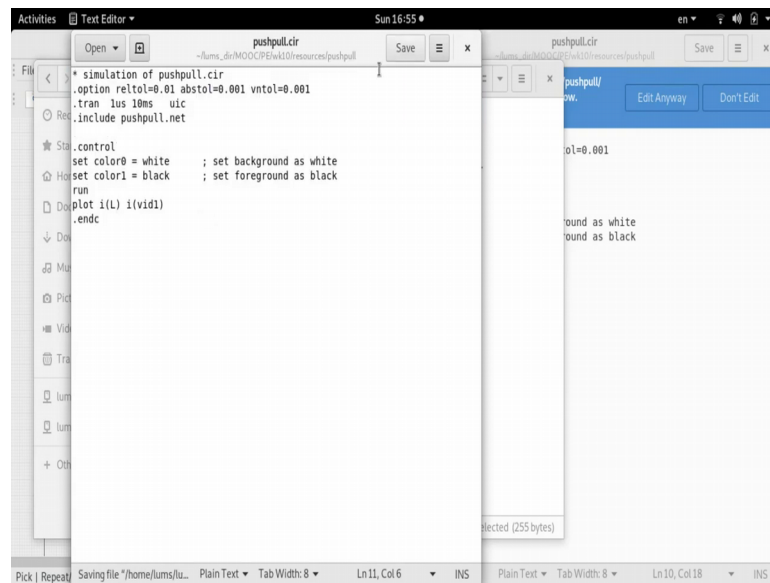
(Refer Slide Time: 07:09)



So, this push pull, when I double click I have set  $N_p$  primary turns as 10 seconds returns as 20, so, turns ratio of 2. So, you will have 10 into 2 20 will be  $v$  pole voltage ideally. But there are diode drops which comes in during the simulation, so, it was less than 20.

So, that is what you are seeing here, the pole voltage waveform is hovering at 17 point 17.5 volts or so. So, you have to 2 diode drops coming to the picture, it is actually a diode drop and  $v_c$  sat drop; so, those 2 are the once which are making up for this drop. You see also on the negative side during freewheeling the drop negative voltage is due to the diode drop. Let me show you 2 things, one is the edt01 sub and the cir files.

(Refer Slide Time: 08:19)



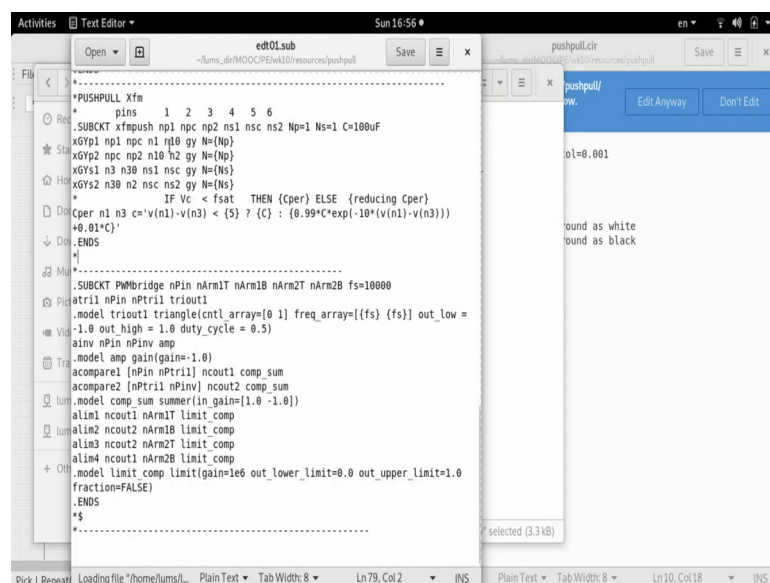
```
* simulation of pushpull.cir
.option reltol=0.01 abstol=0.001 vntol=0.001
.tran 1us 10ms uic
.include pushpull.net

.control
set color0 = white ; set background as white
set color1 = black ; set foreground as black
run
plot i(L) i(vd1)
.endc
```

So, here if I double click on the push pull dot cir, you have you have this.

So, push pull cir push pull circuit, I have a dot options relative tolerance and abs tol, I have said. So, this is the dot trans statement, it is including push pull dot net, this is the control statements where I am setting the background as white and foreground as black. And running the plot command to visualize the inductor current and the diode d1 current so, this is the say our file.

(Refer Slide Time: 08:58)

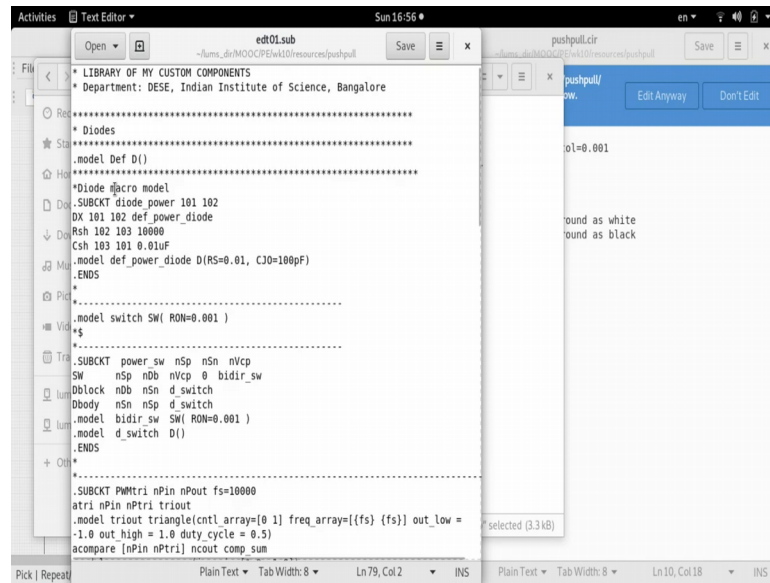


```
*-----
*PUSHPULL Xfm
* pins 1 2 3 4 5 6
.SUBCKT xfpush np1 npc np2 ns1 nsc ns2 Np=1 Ns=1 C=100uF
xGvp1 np1 npc n1 nq0 gy N=(Np)
xGvp2 npc np2 n10 h2 gy N=(Np)
xGvs1 n3 n30 ns1 nsc gy N=(Ns)
xGvs2 n30 n2 nsc ns2 gy N=(Ns)
*
IF Vc < fsat THEN {cper} ELSE {reducing Cper}
Cper n1 n3 c='v(n1)-v(n3) < {5} ? {c} : {0.99*c*exp(-10*(v(n1)-v(n3))
+0.01*c)
.ENDS
*-----
.SUBCKT PwmBridge nPin nArm1T nArm1B nArm2T nArm2B fs=10000
ptr11 nPin nPtr11 triout1
.model triout1 triangle(cntl_array=[0 1] freq_array=[{fs}] out_low =
-1.0 out_high = 1.0 duty_cycle = 0.5)
aInv nPin nPinv amp
.model amp gain(gain=-1.0)
.model amp gain(gain=-1.0)
acompare1 [nPin nPtr11] ncout1 comp sum
acompare2 [nPtr11 nPinv] ncout2 comp sum
.model comp sum summer(in_gain=[1.0 -1.0])
alim1 ncout1 nArm1T limit comp
alim2 ncout2 nArm1B limit comp
alim3 ncout2 nArm2T limit comp
alim4 ncout1 nArm2B limit comp
.model limit comp limit(gain=1e6 out_lower_limit=0.0 out_upper_limit=1.0
fraction=FALSE)
.ENDS
*E
*-----
```

Next I want to also show you the sub circuit file.



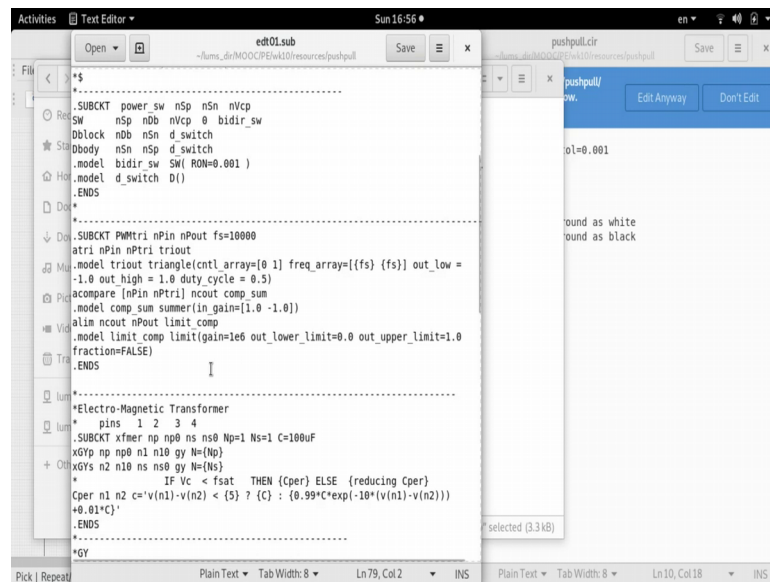
(Refer Slide Time: 09:06)



```
* LIBRARY OF MY CUSTOM COMPONENTS
* Department: DESE, Indian Institute of Science, Bangalore
* Diodes
*-----
.model Def D()
*-----
*Diode @acro model
.SUBCKT diode power 101 102
DX 101 102 def_power_diode
Rsh 102 103 10000
Csh 103 101 0.01uF
.model def_power_diode D(RS=0.01, CJO=100pF)
.ENDS
*-----
.model switch SW( RON=0.001 )
*$
*-----
.SUBCKT power_sw nSp nSn nVcp
SW nSp nDb nVcp 0 bidir_sw
Dblock nDb nSn d_switch
Dbody nSn nSp d_switch
.model bidir_sw SW( RON=0.001 )
.model d_switch D()
.ENDS
*-----
.SUBCKT PwmTri nPin nPout fs=10000
atri nPin nPtri triout
.model triout triangle(cntl_array=[0 1] freq_array=[{fs} {fs}] out_low =
-1.0 out_high = 1.0 duty_cycle = 0.5)
acompare [nPin nPtri] ncout comp_sum
.model comp_sum summer(in_gain=[1.0 -1.0])
.alim ncout nPout limit_comp
.model limit_comp limit(gain=1e6 out_lower_limit=0.0 out_upper_limit=1.0
fraction=FALSE)
.ENDS
*-----
*Electro-Magnetic Transformer
* pins 1 2 3 4
.SUBCKT xfmer np np0 ns ns0 Np=1 Ns=1 C=100uF
xGvp np np0 n1 n10 gy N=(Np)
xGvs n2 n10 ns ns0 gy N=(Ns)
* IF Vc < fsat THEN {Cper} ELSE {reducing Cper}
Cper n1 n2 ce='v(n1)-v(n2) < {fs} ? {C} : {0.99*C*exp(-10*(v(n1)-v(n2)))
+0.01*C}'
.ENDS
*GY
```

So, in this sub circuit file; so, what do I have, I have the default diodes of course, diode micro models.

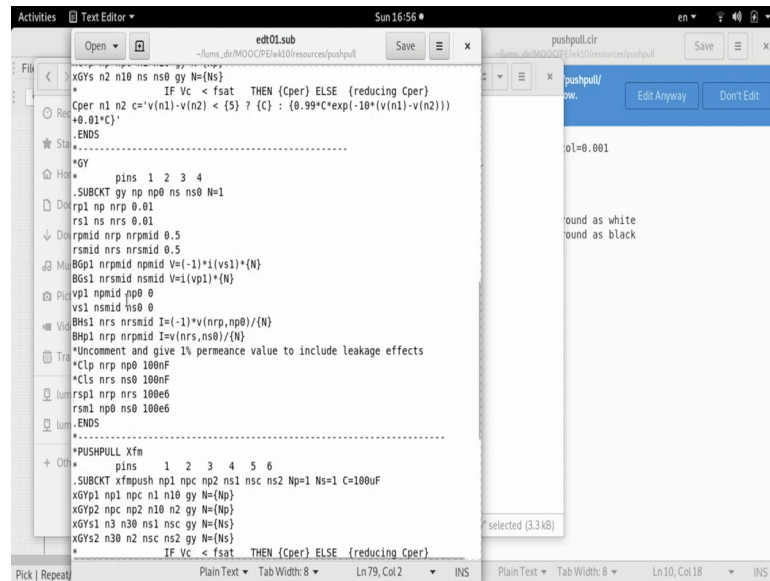
(Refer Slide Time: 09:16)



```
*-----
*Electro-Magnetic Transformer
* pins 1 2 3 4
.SUBCKT xfmer np np0 ns ns0 Np=1 Ns=1 C=100uF
xGvp np np0 n1 n10 gy N=(Np)
xGvs n2 n10 ns ns0 gy N=(Ns)
* IF Vc < fsat THEN {Cper} ELSE {reducing Cper}
Cper n1 n2 ce='v(n1)-v(n2) < {fs} ? {C} : {0.99*C*exp(-10*(v(n1)-v(n2)))
+0.01*C}'
.ENDS
*GY
```

And I have this switch model which I have used.

(Refer Slide Time: 09:21)

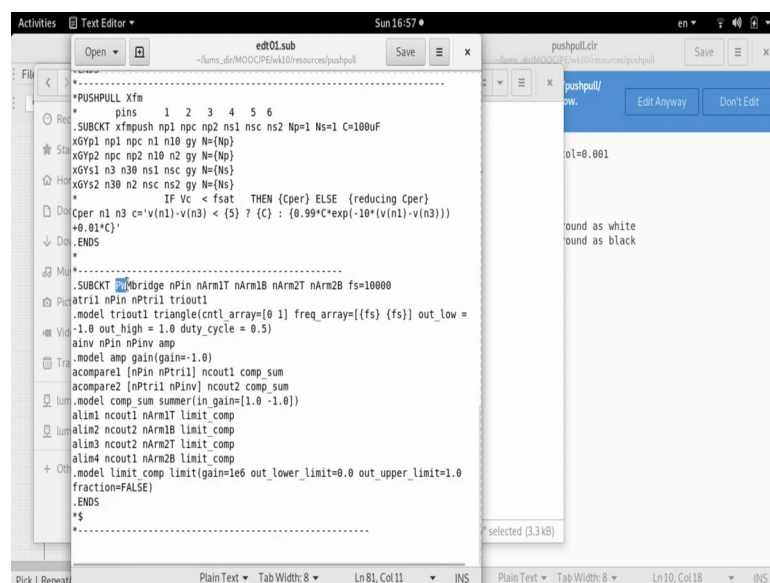


```
Activities | Text Editor | Sun 16:56 | en |
-----|-----|-----|
Open | Save | x | pushpull.cir | Save | x |
-----|-----|-----|
File | Edit | Save | x |
-----|-----|-----|
xGy's n2 n10 ns ns0 gy N=(Ns)
* IF Vc < fsat THEN {cper} ELSE {reducing Cper}
Cper n1 n2 c='v(n1)-v(n2) < {5} ? {C} : {0.99*C*exp(-10*(v(n1)-v(n2)))
+0.01*C}'
.ENDS
*-----*
*GY
* pins 1 2 3 4
.SUBCKT gy np np0 ns ns0 N=1
rpl np nrp 0.01
rs1 ns nrs 0.01
rps1 nrs nrs 0.5
rps2 nrs nrs 0.5
Bgp1 nrp nrmid npmid V=(-1)*i(vr1)*(N)
Bgs1 nrs nrmid nsmid V=(vr1)*(N)
vr1 npmid np0 0
vs1 nsmid ns0 0
Bns1 nrs nrmid I=(-1)*v(nrp,np0)/(N)
Bnp1 nrp nrmid I=(nrs,ns0)/(N)
*Uncomment and give 1% permeance value to include leakage effects
*Clp nrp np0 100nF
*Cls nrs ns0 100nF
rsp1 nrp nrs 100e6
rsm1 np0 ns0 100e6
.ENDS
*-----*
*PUSHPULL Xfm
* pins 1 2 3 4 5 6
.SUBCKT xfpush np1 npc np2 ns1 nsc ns2 Np=1 Ns=1 C=100uF
xGvp1 np1 npc n1 n10 gy N=(Np)
xGvp2 npc np2 n10 n2 gy N=(Np)
xGvs1 n3 n30 ns1 nsc gy N=(Ns)
xGvs2 n30 n2 nsc ns2 gy N=(Ns)
*
IF Vc < fsat THEN {cper} ELSE {reducing Cper}
Cper n1 n3 c='v(n1)-v(n3) < {5} ? {C} : {0.99*C*exp(-10*(v(n1)-v(n3)))
+0.01*C}'
.ENDS
*-----*
.SUBCKT Mbridge nPin nArm1T nArm1B nArm2T nArm2B fs=10000
ntrl1 nPin nPtril1 triout1
.model triout1 triangle(cntl_array={0 1} freq_array={{fs}} out_low =
-1.0 out_high = 1.0 duty_cycle = 0.5)
ainv nPin nPinv amp
.model amp gain(gain=-1.0)
acompare1 [nPin nPtril1] ncout1 comp sum
acompare2 [nPtril1 nPinv] ncout2 comp sum
.model comp sum summer(in_gain={1.0 -1.0})
alin1 ncout1 nArm1T limit comp
alin2 ncout2 nArm1B limit comp
alin3 ncout2 nArm2T limit comp
alin4 ncout1 nArm2B limit comp
.model limit comp limit(gain=1e6 out_lower_limit=0.0 out_upper_limit=1.0
fraction=FALSE)
.ENDS
*E
*-----*
pushpull.cir | Save | x |
-----|-----|-----|
pushpull/ | Save | x |
-----|-----|-----|
pushpull/ | Save | x |
-----|-----|-----|
t=0.001
found as white
found as black
selected (3.3 kB)
-----|-----|-----|
Pick | Repeat | Plain Text | Tab Width: 8 | Ln 79, Col 2 | INS | Plain Text | Tab Width: 8 | Ln 10, Col 18 | INS |
```

And there is the electromagnetic transformer, the gyrator; these are called intern by the push pull transformer. This is the push pull transformer that we are using, sub that sub circuit which is calling the gyrators.

So, these model we have done using analogue behavioral modeling; of course, it is not within the scope of this course to cover behavior analogue behavioral modeling for simulation. But, I am including this file you can study at leisure to understand that.

(Refer Slide Time: 09:55)



```
Activities | Text Editor | Sun 16:57 | en |
-----|-----|-----|
Open | Save | x | pushpull.cir | Save | x |
-----|-----|-----|
File | Edit | Save | x |
-----|-----|-----|
*PUSHPULL Xfm
* pins 1 2 3 4 5 6
.SUBCKT xfpush np1 npc np2 ns1 nsc ns2 Np=1 Ns=1 C=100uF
xGvp1 np1 npc n1 n10 gy N=(Np)
xGvp2 npc np2 n10 n2 gy N=(Np)
xGvs1 n3 n30 ns1 nsc gy N=(Ns)
xGvs2 n30 n2 nsc ns2 gy N=(Ns)
*
IF Vc < fsat THEN {cper} ELSE {reducing Cper}
Cper n1 n3 c='v(n1)-v(n3) < {5} ? {C} : {0.99*C*exp(-10*(v(n1)-v(n3)))
+0.01*C}'
.ENDS
*-----*
.SUBCKT Mbridge nPin nArm1T nArm1B nArm2T nArm2B fs=10000
ntrl1 nPin nPtril1 triout1
.model triout1 triangle(cntl_array={0 1} freq_array={{fs}} out_low =
-1.0 out_high = 1.0 duty_cycle = 0.5)
ainv nPin nPinv amp
.model amp gain(gain=-1.0)
acompare1 [nPin nPtril1] ncout1 comp sum
acompare2 [nPtril1 nPinv] ncout2 comp sum
.model comp sum summer(in_gain={1.0 -1.0})
alin1 ncout1 nArm1T limit comp
alin2 ncout2 nArm1B limit comp
alin3 ncout2 nArm2T limit comp
alin4 ncout1 nArm2B limit comp
.model limit comp limit(gain=1e6 out_lower_limit=0.0 out_upper_limit=1.0
fraction=FALSE)
.ENDS
*E
*-----*
pushpull.cir | Save | x |
-----|-----|-----|
pushpull/ | Save | x |
-----|-----|-----|
pushpull/ | Save | x |
-----|-----|-----|
t=0.001
found as white
found as black
selected (3.3 kB)
-----|-----|-----|
Pick | Repeat | Plain Text | Tab Width: 8 | Ln 81, Col 11 | INS | Plain Text | Tab Width: 8 | Ln 10, Col 18 | INS |
```

And then, down here I am including another analogue behavioral model for PWM generation which will generate the 4 PWMs for the 4 bridge switches.

So, this is stimulating push pull circuit, you are free to make changes and explore the circuit as much as possible, and change the source. You can change the output you can change the turns ratio, you can also change at the PWM the duty cycle and check how it will work, how it will behave. And the voltages and the currents at various points in the push pull circuit is it coming according to what we discussed and according to theory. And if it is not coming according to theory where is the discrepancy, where is non (Refer Time: 10:50) come into the picture, these aspects you can study.