Fundamentals of Power Electronics
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Lecture – 29
Passive power improvement circuit

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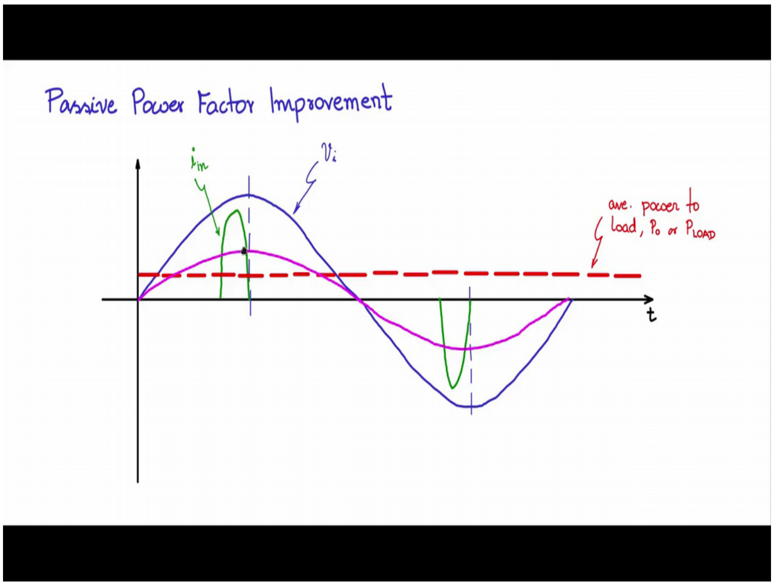

Let us look at Power Factor Improvement. Now, we will look at passive power factor improvement, later on much later after we discuss the switched mode power converters we will also discuss active power factor improvement. For now, let us improve the power factor by using passive components. Let us, to do that let us get a hang of what we should do.

We have the input voltage wave shape sinusoidal like this and the current wave shape for the rectifier capacitor filter circuit is in this fashion. This will deliver an average load power like this the red line. So, this would be the average power delivered to the load and we can call that as P naught or P load.

Now, to deliver the same average power the same P naught if we had a pure resistive load how will the current look like? Resistive load the current will be like this. Now, observe that the peak is much reduced compared to this, that is because for the same load if I had a resistive a resistance load you will see that the current is conducting for the whole cycle because the current has to be in phase with the voltage and have the same wave shape. And v m i m by 2 is the power that is delivered to the load and therefore, I m is fixed by that and you will see that the i m is much lower than what you would get for the case of the rectifier capacitor filter for this particular P naught.

The take away from here is that as I widen the base; as I widen the base of conduction the peak will start reducing. Now, that is the take away that we are going to use for improving the power factor.

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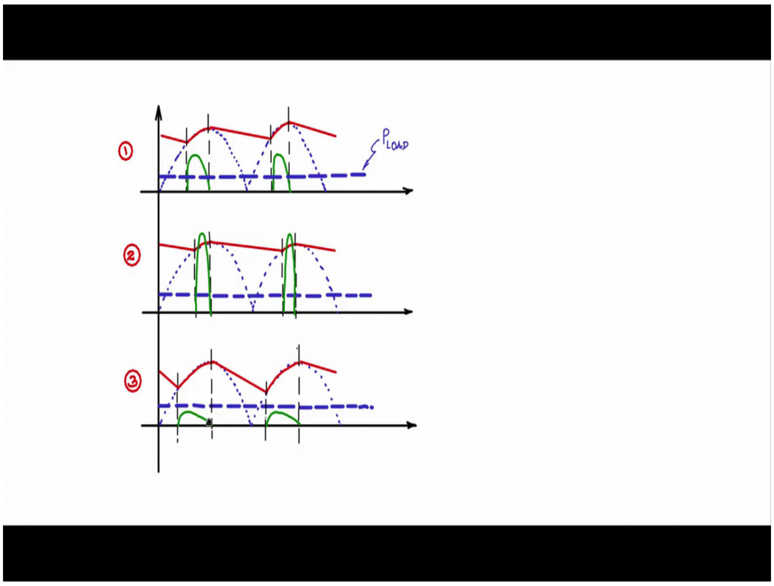

To consolidate this, I am going to show 3 possibilities on the graph. Let me draw the rectified input source and let me take the output voltage ripple in this fashion. Call this as case 1. Now, case 2, again let me have the input voltage wave shape and let me consider the output voltage ripple in this fashion. This is a slightly lesser ripple than this case and call that as case 2. And the 3d case I would like to give more ripple than previous two and let us say that the output ripple is in this fashion larger ripple.

Now, let me mark the current conduction time. This is the current conduction time for case 1, correct conduction current conduction time for case 2 and this is the current wave shape for the rectifier capacitor filter circuit. Now, if you look at the current conduction for case 2, it is now narrower because the ripple is smaller the conduction period is much narrower. Now, let us say in case 1 some amount of power is being delivered and let say this is P load, consider for the same power average power delivered to the load you will find that the current conduction as it is narrowed in order to keep the same area you will have much higher value of peak, current peak will be much larger compared to this.

Likewise, in case 3 you will see that for the same average power we have increased consciously the current conduction time and the current peaks will be much lower. So, this is actually the concept that we will be using in passive power factor improvement. We will be trying to increase the current conduction time at the expense of ripple, more ripple and thereby reduce the current peaks and improve the power factor, making it closer and closer to the full conduction as in the case of a pure resistive load.

So, that is what we would be like doing. I will take up an example passive power factor improvement circuit for rectifier capacitor filter which will give conduction for a much wider range and probably simulate that to understand its operation.

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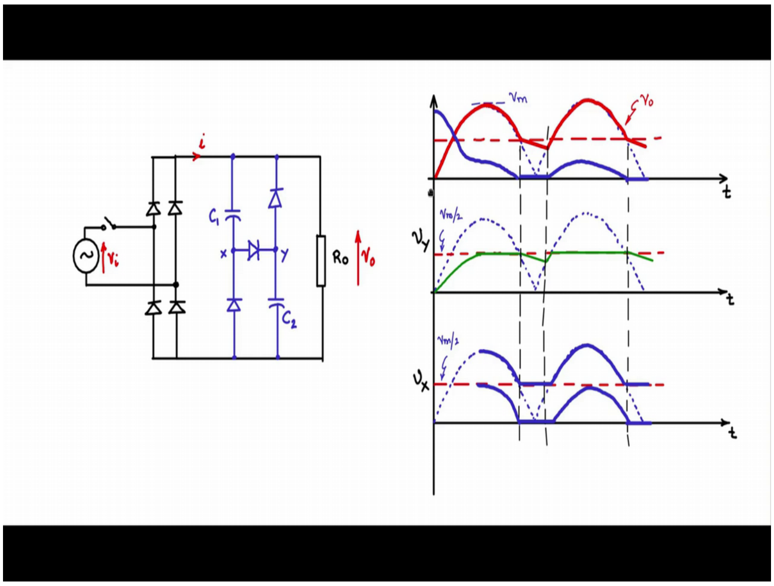

Let us now draw a passive power factor improved circuit. Let me put the source and this diode bridge we are familiar with this diode bridge then connect the source through a switch like this and across the bridge in this fashion. Now, this portion we know this P sine wave source followed by a rectifier and let me draw the load R naught first. So, this is the R naught that we connect across the rectifier capacitor.

Normally, we would have connected a capacitor like this; however, we want to modify this into a improved power factor improvement configuration. I will now split the capacitor into 2 parts into this fashion. So, you see that now I have 2 capacitors in series. So, when you connect this when the capacitors are getting charged it will charge up in this fashion.

However, there is no discharge path into the load because of the presence of this diode, there is a reason we will see that. Charging is happening in this path, half the charge will come into this capacitor, half the charge into this capacitance, so if you are having v naught each will take v naught by 2 and v naught by 2. Now, when you want to discharge it discharge each capacitor separately. So, provide the discharge path, you put a diode in this fashion. So, this diode will give you chance for this capacitor to discharge through the resistor in this fashion and if I put a diode here you will see that this capacitor can independently discharge through the load in this fashion.

So, while charging you will see that the charge path is only in this way, the charge is divided equally between the 2 capacitors if the 2 capacitors are equal and the 2 capacitors will independently discharge into the load. So, the diode steering network takes care of this issue. So, let us call this an C 1 this is C 2, x, y and you have v i and v naught. So, let us look at the wave shapes at various nodes to understand this a bit better.

Let me draw the waveforms. Let me put in the rectified waveform at this point if it was only a resistance connected. Let me draw two more time x axis, one will be v y, v y is the voltage across C 2. Note that voltage across C 2 and voltage across C 1 will be exactly same if C 1 and C 2 are same values. Then v x is the voltage across this diode, voltage across this diode will be same as voltage across this diode. So, you need to see just one of these two waveforms. Now, I will paste these images here. Now, when you switch this on the output voltage here will track, on the first cycle it will track the input wave shape like this if I say this is the v m by 2 line and this is also v m by 2 line. So, this v m this will be v m by 2, v m by 2.

V y, I told you that when you switch this on the charging path is through C 1 and C 2 and C 1 and C 2 will equally distribute the charge. So, if you look at the voltage across v y it will go to the halfway mark and stop here. Likewise, C 1 also will reach the halfway mark and stop there. Now, once it is charged fully here, then the input voltage would have gone low, these diodes would be reverse biased under the normal condition if it was a normal circuit. But now, let us say it gets reverse biased reverse condition, then this capacitor starts discharging during which time the diode conducts the capacitor is charged only half the voltage v m by 2 this also v m by 2. So, this node potential v naught will go to v m by 2.

So, if it is v m by 2 again the input will input will charge up the load the diodes will conduct because the input is still higher than v m by 2. So, till the point v m by 2 is reached the input output will track the input. So, let me draw that v m by 2 point. So, till it reaches this point the output will track the input and till that time voltage across the capacitor and voltage of across C 2 both will be fixed constant because there is no discharge path for the capacitances. The load is serviced directly by the input during this time.

Then further on at this point when the input goes below this halfway mark v m by 2, these diodes are out of the picture and the capacitance is only servicing the load. So, this is where the capacitor discharge happens to the load or not. Each of the capacitance C 1 will discharge in this fashion, C 2 will discharge in this fashion. Till it reaches this point when input means crosses this and this diodes will conduct and again the cycle will repeat. So, this will conduct here and once it starts conducting and once the C 1 and C 2 charges are replenished it will go and stay at the v m by 2 level and this continuous in this fashion.

Now, if you look at the envelope of the voltage output voltage it in the first cycle it goes in this fashion up to the point it crosses over and comes to the v m by 2 point it is tracking the input. Now, at this point these diodes switch off and the output is just the capacitor voltage which are discharging like this and then at this point again it will start tracking it will start tracking the input and comes down and then again here you will see it will track the capacitor voltages. Now, this will be the output voltage envelope look at the very large ripple. But look at the conduction time the conduction time is all this time the current conduction time.

So, this is v naught. So, let me draw these critical marker points like that. So, during this time only the current is 0 here this current i is 0 here because at that time the capacitor is discharging and during this time you will have the current this first cycle charge it is like this, the second cycle onwards you will see that it will just be in this fashion. Now, you see that the conduction period of this current has been widened so much and therefore, the peak would be significantly lower compared to the normal capacitor rectifier filter capacitor circuit.

Now, when you come to the v x waveform here, the v x will have an envelope. Now, this is a constant fixed, let us say this is a constant fixed v m by 2 this will be whatever the value v naught here, v naught minus v m by 2 will appear across this one. V naught is this waveform minus this v m by 2. So, I am just taking it from this point here let us say. So, it is this envelope that v x will have. And this point will be the 0 point because the it is during this time this diode is conducting. When the capacitor is discharging during this time the diode is conducting and then you will have a horizontal. So, this is the type of waveform that you will see for v x and also across this diodes.