Fundamentals of Power Electronics

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Lecture – 10
Thyristors

Hello and welcome back. Now, after having seen the working of a power diode its switching characteristics, its construction, so on, now let us move on to a bit more complex power devices which are more involved and actually they can do lot more then the diode which as you know is an uncontrollable switch, ok. Now, let us begin with this type 2 switch, the Thyristor.

Now, thyristor actually is a generic name for usually know the 4 layered devices which came up in 1950s. And the salient feature of these 4 layered devices is that they have an internal regenerative process which actually results in their turning on. Now, we will see that under the thyristor family there are several devices which were developed; one of them is silicon controlled rectifier which we are going to see in details. The limitation of the silicon controlled rectifier though it was possible to turn it on by using the gate terminal, it was not possible to turn it off by using the same the same terminal you cannot have any control you cannot exercise any control over the turn off of the device. So, basically, I termed it as a car which we were driving which has actually whose breaks of failed. Now, the question is how to stop this car. So, this kind of a challenge was always presented by the SCR.

Then a variant of this was actually developed which was called the gate turn-off thyristor GTO which actually could be both turn on like a SCR, but could also be turn off through its gate terminal. So, we are going to look at these mechanisms you know how this is done. So, this particular session is mainly devoted to the working the construction of the SCR and its close variant the GTO, the gate turn-off thyristor, ok.

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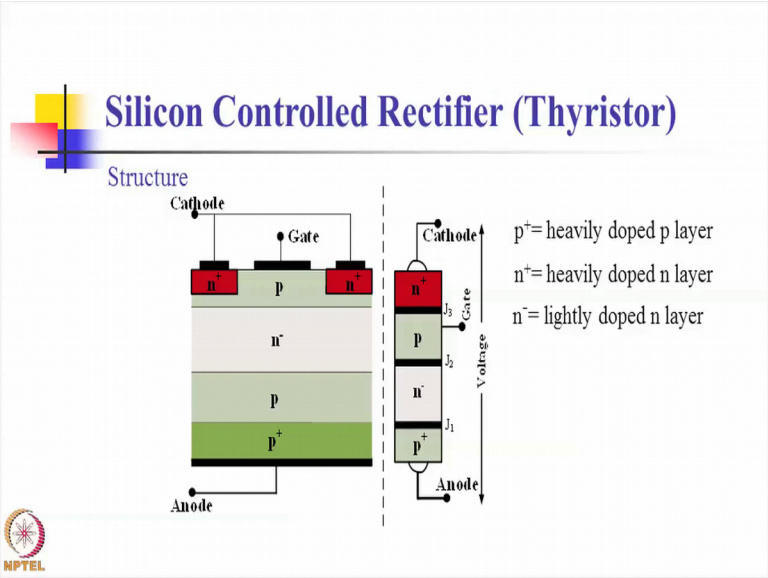

So, what do you see on the slide here, on the screen is actually the structure of a silicon controlled rectifier, ok that, we just draw this here very quickly. So, that I can use this to explain a few things to you later on, ok.

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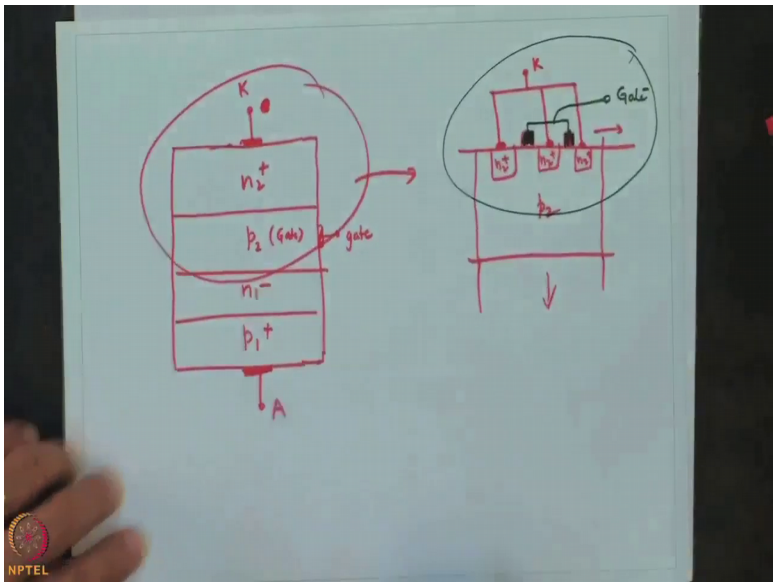

So, this is a structure and it has 4 layers as we talked sometime back, I just mentioned that. It has a p 1 layer, we call it p 1 and p 2 because there are 4 layers and two of them are p and two of them are n-type. So, p 1 plus, plus means very highly doped, n 1 with a minus sign which means it is a lightly doped layer and we have the other p which is a

moderately doped layer and this actually is going to be the gate of the device, ok. And we have this n 2 plus layer. So, the gate I can just probably show here as a gate. And this n 2 plus, so this second n layer which is very highly doped is actually through a metal contact becomes the cathode, which we just usually because of the week connection we actually prefer to noted by K. And similarly, this lower layer p 1 plus highly doped p 1 layer we just show that this is p anode denoted by A, ok.

But you know for the reasons of you know the working of this device, the basic principle that control the working of these kinds of devices, it is usually the case that the gate and the you know the cathode structure there highly interdigitated, ok. So, you actually have the gate and the you know the cathodes which are interwoven with each other.

So, if I was to just show you the top this portion here, I can show you something like this p 2 and of course, there are other layers here p 2, and into this p 2 you will see that there are several n 2 plus layers regions. So, you can see that they are all the time, they are they are actually distributed all over this p region and that is how what we what we mean by saying that they are highly interwoven. You can actually I could actually mark the cathode and other place things also here.

So, let me just say a metallic contact here, a metallic contact here, an n 2 plus and another one here and so on the many of these, they will all we connected at one place and this is called the Cathode. Likewise, you have the gate structure here, the gate structure here and they are also, so let me just use the green colour here sorry I should have used a green colour here its these are connected, and these are giving you the this has to the gate terminal. So, you can see that the cathode and the gate they are extremely interwoven with the each other and this actually plays a very prominent role, and we will see that it is a very critical role in the operation of the device.

Now, looking from the top you know this structure of the anode and the gate being interwoven with each other or interdigitated with respect to each other can be actually represented. We will just have a very simple appearance here, like this.

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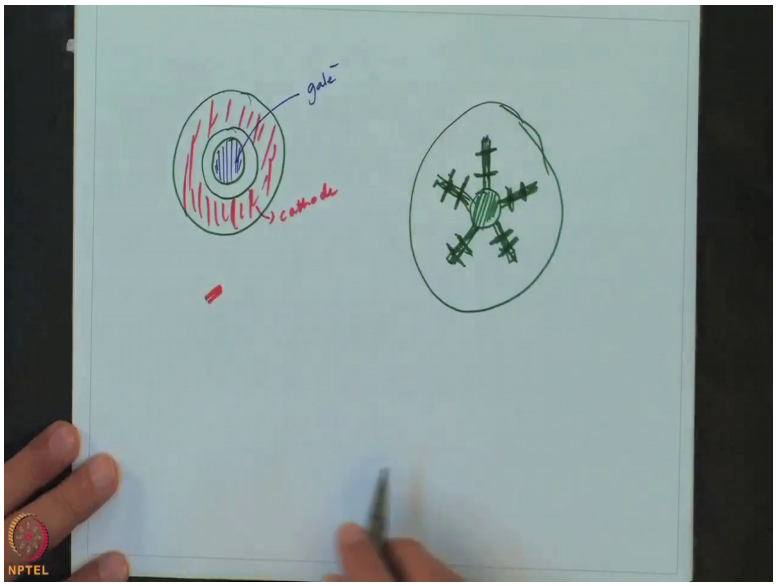

So, I will just use a red colour may be to denote the cathode part, this all cathode and I just use a blue colour to denote the gate. So, you can see that this portion is gate and here there is cathode. So, there are some silicon controlled rectifier devices which will have this kind of a appearance, a top view of the device. So, you can see how the gate and the cathode are distributed with respect to each other.

Now, there is another one which is a little bit more complex and that is specifically used for the cases where the silicon controlled rectifiers are meant to use for high frequency operations. What you see just now this one here is actually for low frequency operations, really when you are operating at a very low frequency. These high frequency ones are a little bit more involved, so let me just draw them a little bit you know more carefully. So, you can see that this is how, ok; so, you can see this is how the you know the gate would look in this case and the remaining thing is your cathode. This is a very important aspect for SCRs and the GTOs.

Now, let us try to understand you know how the SCR works. So, let me just draw this picture.

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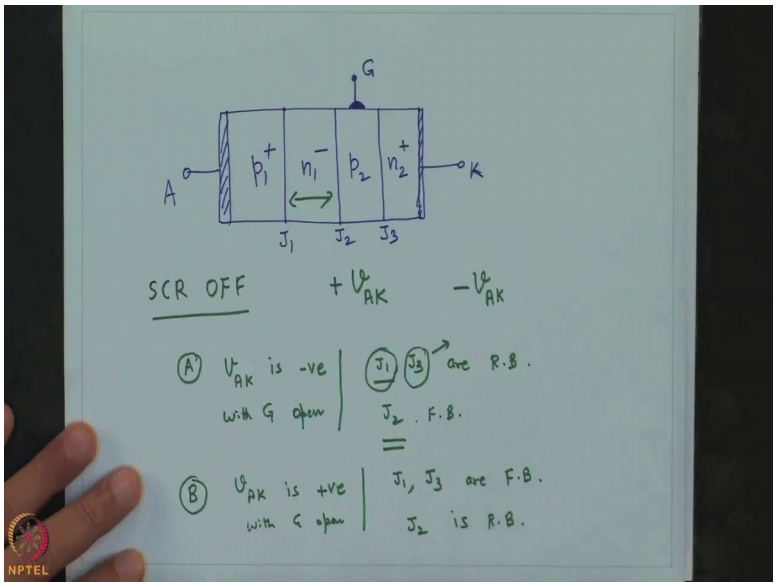

So, this is my SCR I am just trying to draw it now horizontally. So, on the left side let me say this is a metallic contact to the anode and on the right side let say we have a metallic contact with K and you have these 4 layers that we know very well there are 4 layers different types of semi-conductors. And we have already seen that this is p 1 very highly doped with a plus sign n 1 with a minus sign means it is a lightly doped n layer, p 2 here without a plus or a minus means it is a moderately doped or you know layer of p-type semiconductor and here it is n 2 plus, so highly doped n-type layer which is there. So, this is how this looks in you know horizontally SCR.

Now, let us see what are the various modes in which the SCR operates. It will actually helps us construct you know the I-V characteristics of the silicon controlled rectifier in due course, ok. Now, there are two ways or there are two conditions under which the SCR can be actually off. So, it is not just that when the device is reversed biased that your silicon controlled rectifier would be off. It can actually be off even when a forward voltage is applied to the SCR and this is called the forward voltage blocking capability or what differentiates the fully controllable devices or semi controlled devices with a device like a diode which is uncontrollable switch or device. So, there are two cases let us see what are those conditions when SCR is off, ok.

Now, this can happen as I said both when there is a plus V AK applied across the device or there is a minus V AK applied which means it is a reversed bias across the device and

plus V AK this is a forward bias across the device, ok. So, let us just put A here. Now, when V AK is negative with G open, the G is open I sorry I did not mark that G here I think I should mark that here. So, with G open we come to this case, so what happens under this particular condition? We will find that J 1 and J 3 are reverse biased, and J 2 that is forward biased where you know I can just mark here also these junctions J 1 and J 2, I can say this is J 1, this is J 2 and this is J 3.

Now, the point is that this J 3, if you see this junction J 3 it is actually surrounded by two heavily doped layers. You can see that both p 2 and n 2 are heavily doped, p 2 is of course, moderately doped, but it is still very heavily doped you know relatively very high doping still. So, J 3 is obviously, should be concept that we have learnt while we were studying the power diode, we know that the J 3 junction cannot withstand a large breakdown voltage. So, it actually we will find that it actually breaks down at very low voltages, very low negative voltages that will come across this junction it will not be able to pair them. But J 1 if you see that is surrounded by one highly doped layer p 1 plus, but the other one is n 1 minus which is a lightly doped layer. This one here when it is a reverse biased this junction J 1, the depletion layer can be accommodated in this slightly doped n 1 minus layer and that is why the capability of J 1 to stand a large negative voltages very high.

So, J 1 is where therefore, will be able to absorb this negative voltage there will be a applied across the device, ok. Usually the in practice we will see that n 1 minus this layer here that is kept to be bit long. So, that it can absorb the depletion layer, because as we said it is going to be basically, withstanding all the negative voltages because you know J 3 is not capable of doing that, ok.

Now, let us see what happens in the B case that is when V AK is positive, and, again let us say that G is open and assume V AK to be less than V BO the break over voltage in the forward direction in these two conditions. Now, we will find that J 1 and J 3 are forward biased while J 2 is reverse biased, ok, but this is not a problem that J 2 is a reverse biased because J 2 also has this n 1 minus layer on to its left. So, just like J 1 has you know the n 1 minus layer on to its right J 2 layer also the J 2 junction also has a n 1 minus layer to its left. So, basically, what we are trying to says that both J 1 and J 2 can withstand a large reverse voltage and they will have a large voltage break down

capability. By the way if the break down occurs in these devices it is mostly through avalanche break down.

Now, we want to understand little bit more about this device, ok. And it is observed that in this context it really helps if we can actually split this 4 layer device into two transistors which are connected in a very specific manner that is what we are going to see now. And it is very easy with the help of this what is called two transistor model to understand the working of the you know the several aspects of the silicon controlled rectifier.

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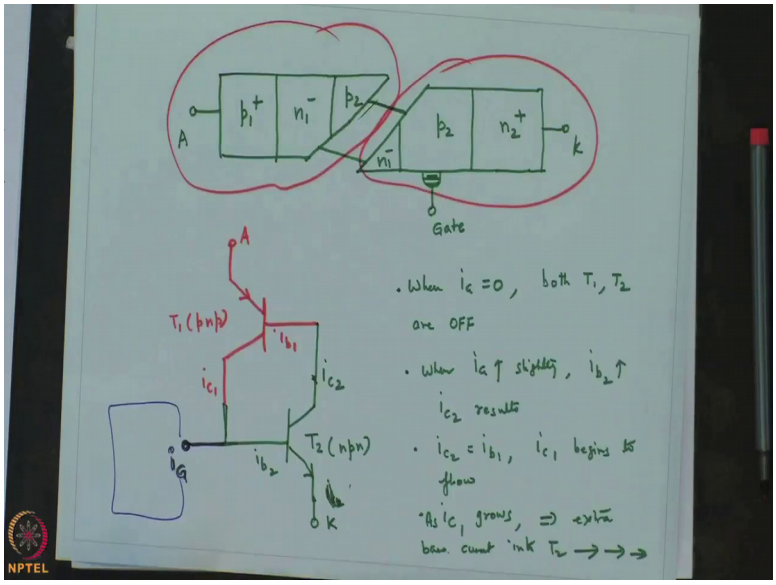

So, let me just first prepare the ground for creating this two transistor model. So, please see that this is just you know the one of the half the you know the anode side half that I have drawn, and I have just kind of sliced you know through this device and the other side, will be also will be just analogous to this we cathode side that is k and I can just say that this is my n 1 minus layer and this is p 2 and this is n 2 plus these are the two layers and here is the gate, ok. But I will also have to obviously show the connection between these two. So, we know that this p 2 is actually connected with this and this n minus n 1 minus is connected through this connection, ok.

Now, what we see here on the left side if I just look at this structure and also look at this right side structure these are nothing but two transistors one of them is a p n p transistors the other is an n p n transistor. So, if I give them their symbols you know that are used to

represent them and I redraw this I can probably make it much simpler you know to look at. So, let me just draw that. So, this let me just draw the p n p type transistor first. So, let us say this is the anode of the main device of the SCR and this is the first transistor which is the p n p type, let us call this as T 1 and in the bracket I will just say p n p type and it actually is having a current i c 1 the collector current there will be associated with it and of base current i b 1 there will be associated within. Of course, we also have the emitted current which is associated with it.

We can similarly draw the transistor corresponding to the second half of the SCR shown above, ok. So, this is that n p n transistor and it is not very difficult for you to see that you know this base of the second transistor which I am calling as T 2. Now, this is n p n-type first of all transistor and this one the base of this is connected to the collector of the first transistor. And we can also say that this is getting a base current i b 2 and let us say I should probably use another colour may be a blue colour here just to say that this is the i G which is probably coming from some circuit which is designed to provide the gate current for control of the device SCR. So, this here is going to k.

Now, let us quickly understand a few things. Let us supply a forward voltage across the device that is the anode is more positive compared to the cathode. Assume that the applied voltage is less than the forward break over voltage V BO which we will discuss when we come to the I-V characteristics of the device. When i G is 0 both p 1 and p 2 transistors are off; when i G is increased slightly let us see what happens. We find that this actually means i b 2 increases which means i c 2 results, but that is connected to the base of p 1 to this means because i c 2 is equal to i b 1, i c 1 begins to flow and the last important point here is that as this i c 1 grows.

It actually pumps in extra base current into T 2 which in turn increases its collective current and which in turn increases the base current of the first device and so on. So, you can see that this is a cyclic process this is a chain reaction which is starts and it continues till both the transistors they actually get into this saturation mode and completely that turned on.

The turn on of the SCR can also be explained using the Aber Balls model according to the Aber Balls model I A. So, let me just write this equation.

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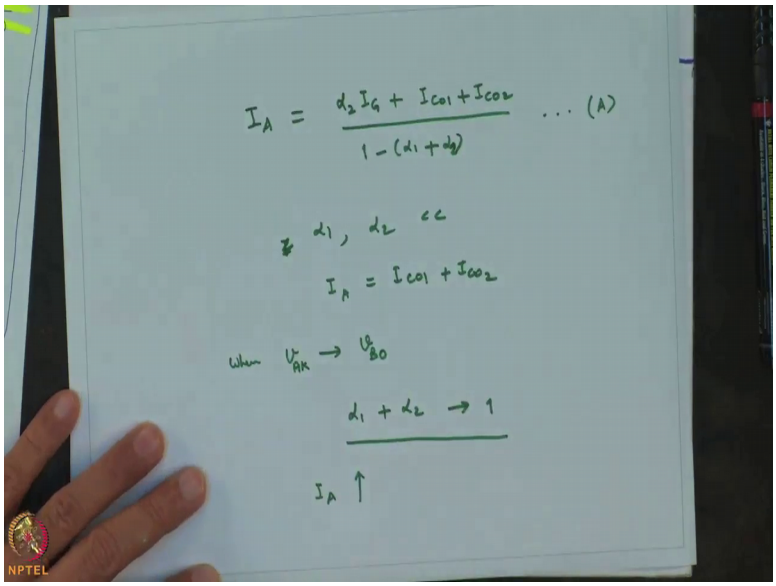

The current flowing through the device I A is equal to alpha 2 into i G, where i G is nothing, but the gate current plus I CO 1 plus I CO 2 divided by 1 minus alpha 1 plus alpha 2, where I CO 1 and I CO 2 represent the leakage currents of the device and alpha 1 and alpha 2 are the base transport factors associated with the two transistors.

Now, in the absence of the gate current and assuming that V AK we applied forward voltages less than the break over voltage V BO, alpha 1 and alpha 2 are small and therefore, I A is equal to I CO 1 plus I CO 2; just two leakage currents add up and it is a very small current. When the forward voltage applied across the device V AK tends towards V BO the reverse bias layer J 2 it expands into the n 1 and the p 2 layers. As this depletion layer due to the reverse bias it expands into n 1 n p 2 layers the base areas of the two transistors they reduce. This results in a higher gain value and the value of the alphas also go up.

Now, as alpha 1 and alpha 2 values go up alpha 1 plus alpha 2 it tends to 1, and if I just number this equation as A and I use this fact that alpha 1 plus alpha 2 is equal to 1 in equation A, we can see that I A the current through the device it raises which means that the device turns on. Now, as the that the two transistors the p n p and the n p n transistors they go into saturation and the anode current of the device it builds up, you know there is a time when this current re is actually exceeds a certain value which is called the latching current. And I can just say if I just denote the device current by I A, I say the moment my

I A is greater than or equal to I L, where I L is nothing but the latching current, ok. Now, the device becomes uncontrollable through G.

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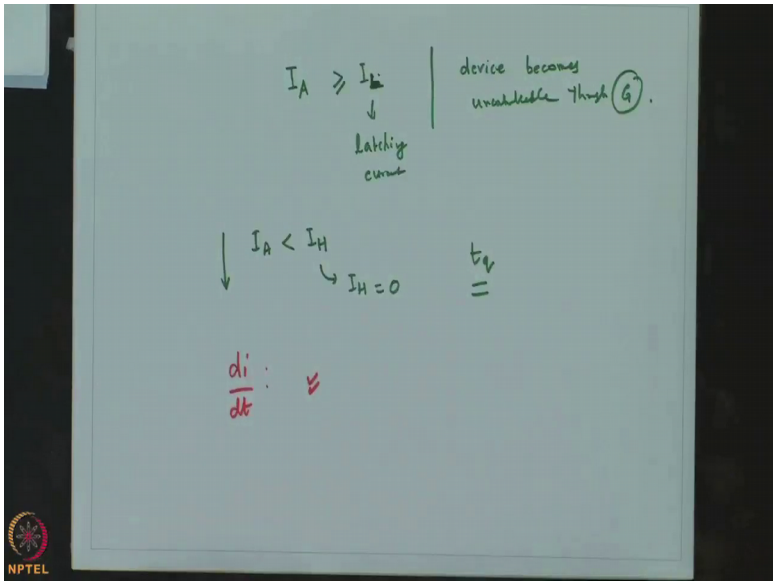

So, now even if we remove the G source or even we apply anything to the G source to somehow stop the device from conduction it will not help that control is lost. Interestingly, to understand the concept of the latching current we need to go back to the original 4 layer structure of the SCR.

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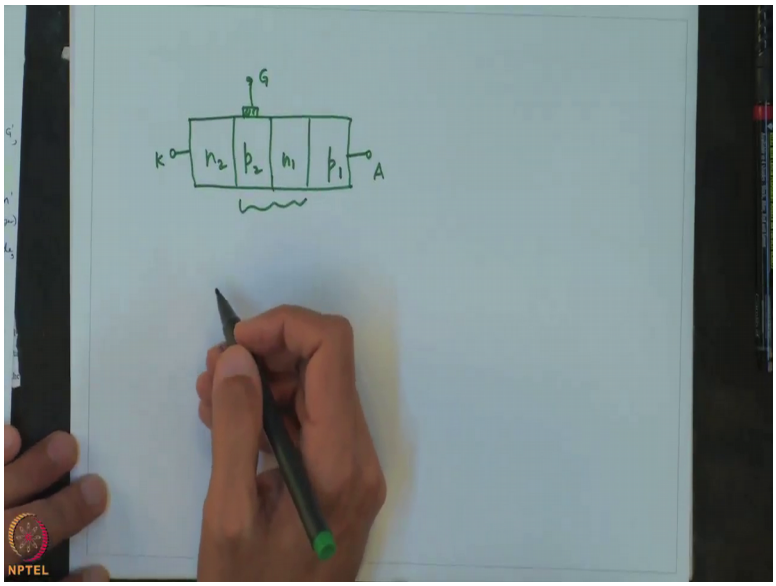

Now, I will just quickly draw this 4 layer structure. So, these are the 4 layers and if we have the anode on this side and the cathode on this side I can just mark these various layers as n 2 p 2, n 1 p 1.

Now, as the device turns on the p 2 layer it gets frudded with electrons coming from G the gate and together with the n 1 layer you know these two they actually constitute what is called an intrinsic low doping density n layer of the device. Thus, the SCR it actually reduces to a power diode structure which we have studied before. Now, we know that a diode is uncontrollable. Now, that is why the gate of the SCR it loses control over the device ones it has crossed a certain value of current called the latching current. In fact, after the SCR has turned on the two transistor model is not really valid.

Now, one very important thing is about the switching off, as we said the gate control is lost ones the device current has exceeded the latching current. Now, let us say that by some mechanism this current is brought down. Now, while this current is being brought down the device actually is not turned off is not considered to be off, as long as it has not gone beyond another very important parameter current parameter which is call the holding current. So, while we are trying to switch off the SCR my I A must go below this current which is called the holding current and the holding current is less than the latching current, and for the ideal case it is you know very common to take I H to be equal to 0.

So, you actually want your device get in to fall to 0 and now you must maintain reverse bias voltage across the device for a certain stipulated time t q, which is called the circuit commutated turn off time t q for the device to completely switch off. Otherwise, if you again apply the forward voltage to the device may again get turned on it may remain in the turn, it may not never switch off it may turn on. Again, actually the turn off characteristics of an SCR are similar to a power diode that we have seen before. Hence, during the turn off the excess charge carriers must be removed in the case of an SCR also this takes time. There is a trade-off between the value of the t q and the forward voltage drop of the device.

If t q is more typically more than 100 microseconds as the case with the rectifier grade SCRs then the forward voltage drop is relatively low, typically 1.5 volts on an average. However, if the value of t q is less typically 20 to 30 microseconds as is found in the case

of inverter grid SCRs, then the forward voltage drop goes up and is found to be typically 2.5 volts or even higher in such cases, ok. So, that is an important thing.

Now, the other very important thing about is SCRs is that they have you know because there are the surface areas are large usually use for high power applications, and though the gate and the cathode structures are we have actually make them highly interdigitated we have tried to make them distributed. So, that you know the gate has excess to all the regions of the cathode as is required. Because you know if you are trying to put a control pulse through gate it must be able to reach all the regions of the cathode to be able to you know then only it will be able to exercise control over the device.

So, in spite of doing this in SCR we will find that this does not really happen and whenever the gate trigger is given the current through the device actually it starts from a very small slice, in a region which is very close to the gate, and then slowly it spreads to the other areas. Now, since the external circuit in which or the circuit in which the SCR is connected that has nothing to do with what is that region or what is that slice a portion of the device which is actually conducting. It has a large current let us say to conduct, it wants a large current to flow.

Now, that current tends to come out from this very small slice very close to the gate region. And this can cause that very high current to pass through that slice very thin slice or break of the device which may actually causes look likes heating, hotspots and may ruin the device. Therefore, there is a limit which is called the di by dt limit which must be followed and it is actually part of this specification (Refer Time: 29:52) of any SCR that you should not exceed a di by dt beyond a certain value. Now, typically the di by dt is controlled by using an inductive snubber in series with the SCR. That is how you limit the di by d t, so that you do not have hotspots and you do not ruin the device. So, it is a very parameter.

Now, just like we saw there is a limit on the di by dt if you recall you know one of the things is that when the devices are applied a forward voltage it was actually the J 2 which was reverse biased. So, J 2 junction which was a reverse biased.

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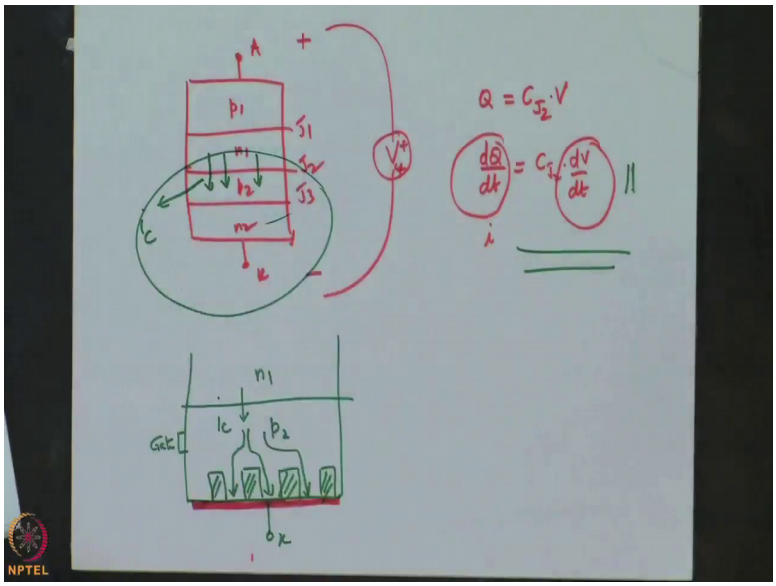

Now, if we just see the device here, you know in this way and we just say that you know there is a J 3 here, J 2 here and J 1 here my anode is on this side, my cathode is on this side, this is p 1 n 1, p 2 n 2 you know that I have now J 2 is reverse bias when I have applied a positive politely externally through an external source through this, ok.

Now, it is basically, as you know a reverse biased junction; J 2 is a reverse biased junction it actually acts as a capacitor. And we know that we can write this relation q is equal to C J 2 let us say the junction two capacitance when it is a reverse biased C J 2 into V, ok. Now, dQ by dt from here will give me C J 2 into dV by dt. Now, what happens that if this dV by dt it actually is more than a certain value you will actually have this dQ by dt which is nothing but the current and which I can actually show with the green colour here you know that this is the current which is actually passing from n 1 to p 2 you know this is the current that is because of this junction J 2 capacitance. So, this I this current and I can actually call this as i c, that is it.

So, what we will see that this current that flows its value will depend on how large is dV by dt from this expression and if this value is very large my i c will be large. And if you see this diagram carefully and look at the previous constructions carefully you can see that this i c is working just like giving a gate current to the device which will actually it triggers this device into conduction. So, basically, you will have to limit dV by dt otherwise the device may get into conduction, you know arbitrarily at any time. Not true

a proper control at the time that you desire through a proper gate signal. So, that is why there is a limit on the dV by dt rating as well.

Now, one very nice way of actually handling this is actually a obtained by is actually realised through schotted emitter connections which I will just show here. I will just show the relevant part. So, this is my you know the cathode and my gate is here, let us say and n 1 layer is here so this is p 2 basically. And now what is happened is that my emitter is schotted at many places. So, what I will actually see is something like this is the emitter or the cathode, ok.

So, what will happen is that when this i c will come as I have shown in the previous diagram, it will actually find a path directly to the cathode, it will directly find a path because you know if I just draw here this is all connected, this is all connected here, this cathode through this plate it is its they are all conduct. So, basically, you will have this current i c which comes and goes just its bypasses the you know the layer which is n 2 it bypasses the n 2 layer and it actually straight away goes to the cathode.

And in this process, you know it reduces the effect and you can actually have more dV by dt. So, if you want to increase the rating dV by dt you can actually have a structure of your emitter which is made like this and therefore, this current that is being generated through the reverse biased junction J 2 this will actually get distributed all over the place. It will bypass the n 2 layer and in the process it will allow you to have more current which means more capacitance which means that it will allow you to get a or to work with a higher dV by dt. So, we will just quickly see the characteristics.

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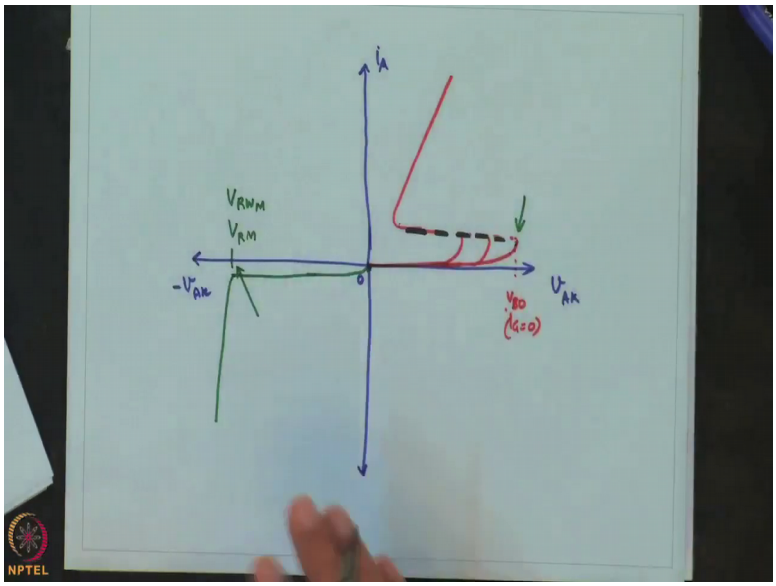

So, let us say we are plotting V AK on to the right side, minus V AK on this side and we have this the device current I A which is discrete here. Let us say that this is 0 the origin. Now, the various device characteristics are going to look like I verses V for the SCR. I will just I am going to use another colour here. So, let us just use a red colour. Let us see we apply a forward voltage.

When we apply the forward voltage let say it goes like this, the leakage current increases little bit and it comes to a certain value V BO when i G is 0 I should say and now I am not applied any gate current signal. And the moment it crosses V BO you know the saturation current to actually initiate the region that you process of the device that I just describe to you with the help of the two transistor model. So, actually you come here and then from here you have this very unstable mode which I am just showing with a, let me just use black colour like this and then the device actually just takes off, like this.

Now, instead of giving no gate signal or gate current if we had given some gate current. What we will find? That this point, where the conductions release starts will actually come a bit earlier. So, you will actually have for slightly more i G you will have the characteristic like this, for still more i G you will have the characteristic like this and so on. So, this is the forward side or this is a forward direction characteristics of the SCR, ok.

Now, what you see on the left side if you apply a negative voltage to the device then what you find that it will have let me just use another colour now, a green colour that it will have a characteristic which will be something like this. Of course, this current here magnitude will not be so much, I have just magnified it for the understanding part and then beyond a certain value which is the maximum reverse voltage or some people also call it as reverse working maximum voltage negative sign negative voltage, it will actually go there and then you actually the device goes avalanche breakdown. So, this is how the characteristic of the of an SCR would look like.

Now, the characteristic of a GTO is also similar as far as a forward side is concern. Now, only thing is that in GTO we happen to do a compromise with the left side characteristics. So, the capability of a GTO to withstand large negative voltage, that is much less compared to an SCR. For an SCR in general the rating of the V BO you know this rating and this rating here both they would be symmetrical they will be same, ok. With GTO this side rating would be less.

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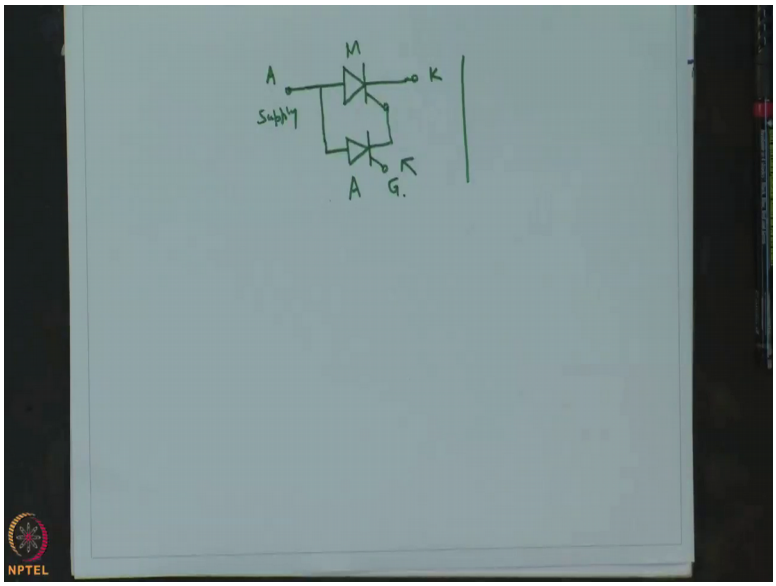

Now, to conclude about SCR here are some interesting facts. Fact number 1, the SCRs are often used is (Refer Time: 39:07) pairs to reduce the gate current requirements. And once such pair you can see that I have already drawn here where you can see that there is a main SCR, and there is an auxiliary SCR and the auxiliary SCR is actually used to

draw a the main SCR. It suddenly reduces the gate requirement required at this terminal G for the overall device, but it actually has a disadvantage of high forward voltage drops.

Fact number 2, there is variant of SCR which is called the a symmetrical SCR where the reverse voltage capability of the device is not same as the forward break over voltage capacity of the device or the forward break over voltage rating of the device because usually that is the case with the SCRs. Now, the reverse voltage blocking capacity is actually compromised you know through special design in the structure. So, as to achieve a lower turn of time t q and to achieve a higher dV by dt rating for the device.

Point number 3, there are special variants of SCR which are actually called the light activity SCRs, which actually get triggered by flashing light on the gate region. Now, this is the very important and useful device for high voltage applications where several of these are actually stacked in series and providing triggering signals becomes a challenge. Now, after having done this let us now see the most important and popular variant of SCR that is the GTO, ok.

Now, coming to the GTOs which I said that they take away the inconvenience of the SCRs. They as I said the SCRs they cannot turn off, in spite of the fact that their basic construction do have some sort of interviewing between the gate and the cathode region, but it is not so significant.

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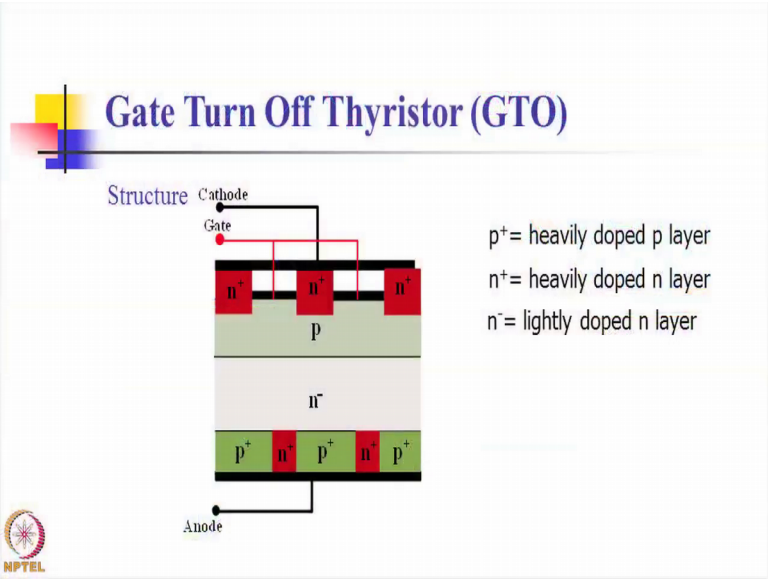

The GTOs were designed with even more prominent interdigitization of the gate and the cathode region. And what you see on your screen right now is the example of the gate turn off thyristor GTO, which is nothing but a variant of thyristor.

So, we will see that its structure is almost the same as an SCR with some minor modifications done here and there, to be able to be switched off, ok. So, what you see here, for example in this slide you can see that this is a very highly interdigitated structure. I will just mark and show you um. So, if you see here this is a very highly interdigitated structure what you see on the screen here, ok. So, this is your cathode, and you can see that the p layer, which is the gate of the device, that is you can see that is highly interdigitated. In fact, the cathodes are actually made like islands. They jut out you know from the surface, in between the gate area and they are all connected through a common metallic plate and this is what you see on your screen right now, ok.

So, how we are able to switch off a GTO, but not an SCR. So, one of the important things that really is contributing to this is the fact that we have a very highly interdigitated structure. So, this is something that is very important for us to understand.

Now, to understand this mechanism of switching off the GTO, let me just draw this structure and you know let us just try to see how this can be done. So, let me just draw one more time this two transistor model, remember the structure of the GTO is same as that of the SCR. So, it can also be represented by a two transistor model just the same way as we have seen in case of the SCR.

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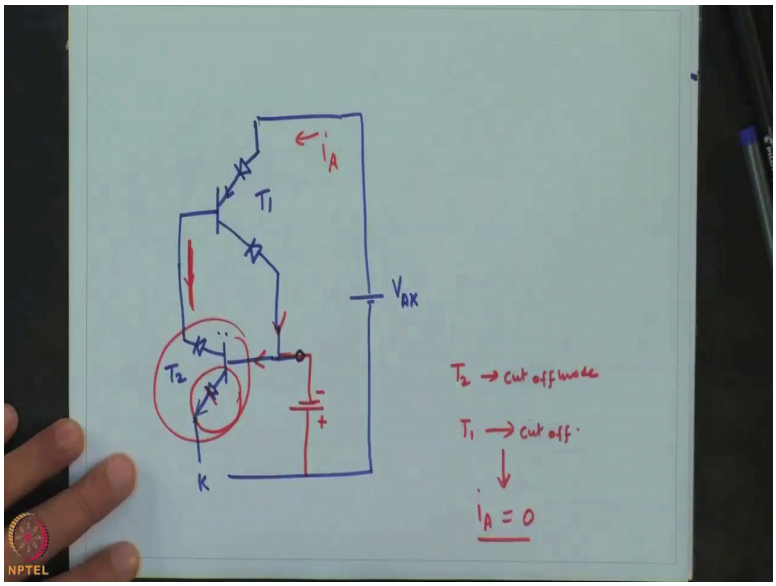

So, you know here there is a, so, that is your T 1 as before and this is a diode and there is another diode here. We just representing the various junctions or the transistor by diodes this is T 2, and this is connected here this is nothing but K and here this thing let us say its connected to an external supply, V AK.

Now, we are trying to turn it off. So, we assuming that you know we are applying to the gate terminal a negative voltage, we are applying a negative source. So, let me just denote that using a red colour this is the G of the device and I just connect this voltage here voltage source here whether negative here and a positive here. Now, the moment this source is applied as you can see in this diagram that this particular junction it becomes reverse biased, ok. It gets reverse biased and when that happens this transistor T 2, it actually goes to from saturation, it goes to cut off more.

So, of course, you know our assumption is that in the beginning before just before we apply this negative pulse to the gate the device is conducted, and when it is conducting we have seen before I told you that both T 1 and T 2 are in saturation. So, when a negative voltages are applied across this you know this junction represented by diode then you find that this particular transistor T 2 it goes into cut off. Now, when that happens, then this current that is flowing here in this branch which is you know the collector current as far as the T 2 is concerned, but the base current as far as T 1 is concerned we find that reduces.

And when that reduces T 1 also goes to cut off. And it again it is see that it actually causes a cyclic process, it is a chain reaction. So, this will cause a reduction in the current that will be flowing through T 1, further reduction in the current that will go into the gate terminal T 2 and then again further reduction in the current of T 2 in the collective region and so on. So, this chain reaction continues till the 5 l G current I A, if I just mark this as I A it goes to 0. So, this is how GTO turns off.

Now, a lot of help for this actually comes from the very peculiar structure that it has. Now, one of the things that is done as you will see in the slide again, if you see the anode region actually is interdigitated between p plus and n plus layers, ok. The idea of doing this is to basically, increase the speed of the GTO, this give works as follows.

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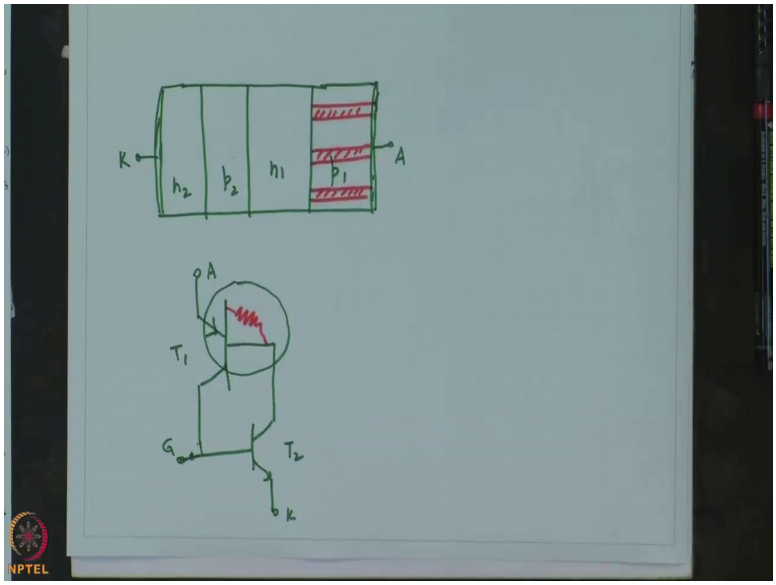

As n 1 is extended into p 1 layer in the form of fingers as you can see in this diagram. So, you can see this diagram which I have drawn this red colour is actually the extension of the n 1 layer into the p 1 layer. So, basically, this effectively reduces the 4 layer device into a 3 layer n p n bipolar transistor therefore, the (Refer Time: 47:32) deep process is not required it is just like switching off normal (Refer Time: 47:36); therefore, the switching off time or the turn off time of the GTO comes down.

However, there is also a disadvantage as I have tried to show with the help of this two transistor equivalent circuit that I have drawn below here, so this one. Now, these fingers the extension of n 1 into the p 1 layer it actually amounts to shorting the emitter and the

base of the top transistor T 1 in this two transistor model, ok. Now, it has the following repercussions. It actually causes a higher voltage drop when the device is conducting. There is also disadvantage with respect to the reverse bias voltage capability of the device. Since, the device behaves like a diode without a likely doped n layer its reverse voltage blocking capability gets compromised.

Another important point when, basically understand here is that a GTO would usually have a higher forward voltage drop when it is conducting compared to an SCR, ok. And it will have the same sort of limits on di by dt and dV by dt as we have seen in the case of SCR, and the one important point however is that I like to mention that there is a maximum limit on the anode current which the GTO can actually turn off. So, which we can actually turn off through the gate control of the GTO. Now, this is a you know an important thing.

Now, typically you know when there is a current I A which is flowing. So, let me just, I have not shown you the symbol yet of the GTO. So, I will just draw this.

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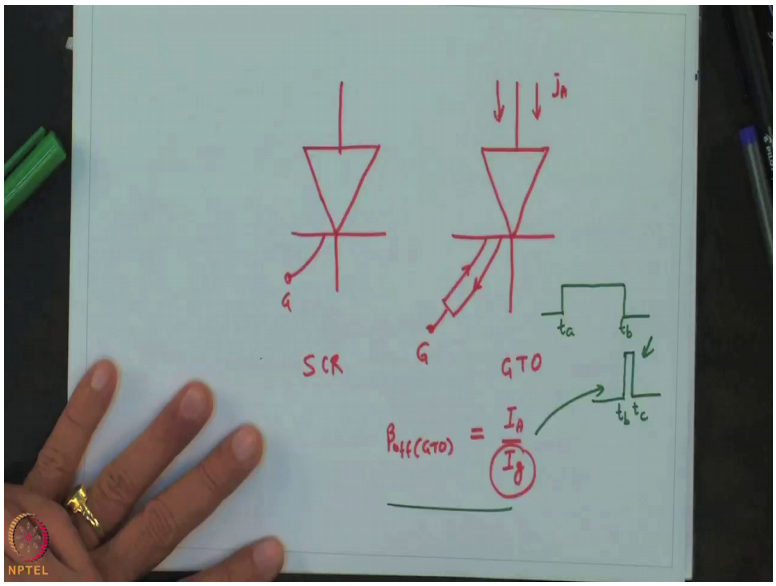

This is the symbol of the SCR. If I put a gate terminal and if I just use this. So, these are both gates. So, this is SCR and this is GTO, ok. These are the symbols, ok. Now, let us say it is conducting the GTO is conducting a current I A. Now, what is that current that we need to pump through the gate terminal to turn the GTO off? It actually is determined by you know this what is called the turn off current gain, which will denote by beta off of

the GTO, ok. So, that turn off current gain or the beta of GTO it is defined as the I A that is flowing what I am showing here, divided by i g; the current that we need to pump through the gate control to turn the GTO off.

So, you can see from here that if the typical values of beta off are something like 3 to 4 then you can see that we will need you know a very high current up to 25percent all the I A will be required to actually switch off the device. So, there is always a limit on this what current you can pump through the gate, ok. So, that is why there is a very critical value that you can actually turn off you know your GTO. So, I A if it is beyond a certain value you will not be able to turn off through the gate control you know as is usually taught, ok.

So, these are some of the things I wanted to tell you. Of course, one of the very important thing is that for the GTOs we have to if we are trying to you know turn on and turn off, turning on is same as what we do in SCR. So, typically the waveforms would appear something like this. So, this is for turn on of the GTO and let us say this is nothing, but t a and t b. And when you are trying turn off then you need to give pulse, a high current pulse which will be determined by you know our beta off; what I just explained to you. And this is how it is going to look like. So, this will be t b and t c. This will be the duration when you are trying to turn off.

So, basically, you will have to give a continuous current waveform to the GTO unlike the SCR to turn it on. While as far as the turning off is concerned you can give a high current pulse which will be determined you know as per the wave if you will look like this, and will be determined by the limitations imposed by the beta off value, which is nothing but the turn off current gain of the GTO.

So, I think we will just conclude this session here. With this I thank you very much for your attention and we will continue to work on the power devices in the coming lectures.

Thank you very much.