Basic Electronics
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Lecture – 71
Digital-to-analog conversion (continued)

Welcome back to Basic Electronics. In this lecture, we will look at the R-2 R ladder network and how it can be used to make up ADAC. We will then discuss analog to digital conversion we will start with the flash ADC and then discuss other types of ADC. So, let us start.

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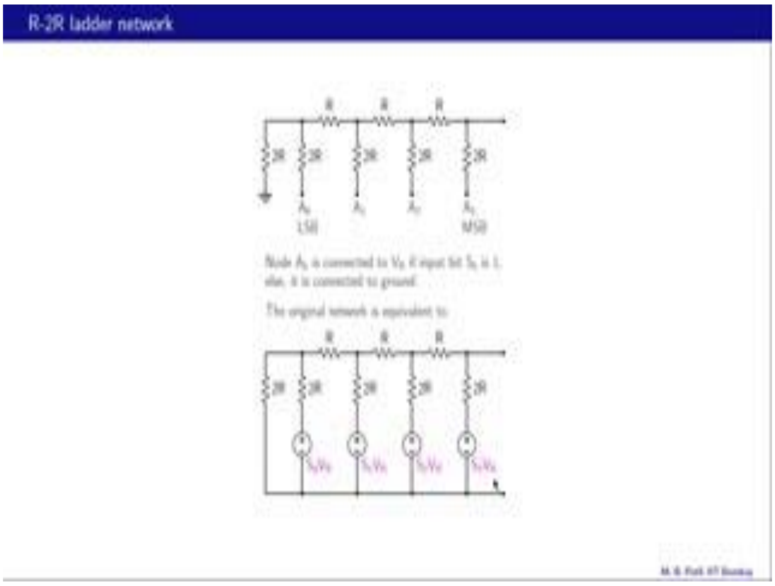

R-2R ladder network

Node A_k is connected to V_R if input bit S_k is 1, else, it is connected to ground.

The original network is equivalent to:

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Let us start here is an example of the R-2 R ladder network and this example corresponds to a 4 bit DAC. This node A 0 corresponds to the LSB; and this node A 3 corresponds to the MSB. And note that we have only R, R - 2R in this network; you do not have any other resistance value that is why it is called R-2 R ladder network. How does it work node A k is connected to V R the reference voltage if input bit is k is 1, else it is connected to ground.

For example, if our LSB is 0, is 1 then the voltage at this node will be V R; otherwise, it will be 0. We can replace this original network for convenience in analysis with this equivalent network, and let us see why the two are the same. This node the ground node here is the same as this common node. Now, let us consider this node here which is A 0 that one. The voltage at this A 0 with respect to this node is S 0 times V R. Now if S 0 is one then the voltage at A 0 is V R; otherwise it is 0 and that is exactly the functionality the hand over here.

And similarly, we connect a voltage supply S 1 V R here, S 2 V R here, S 3 V R over here.

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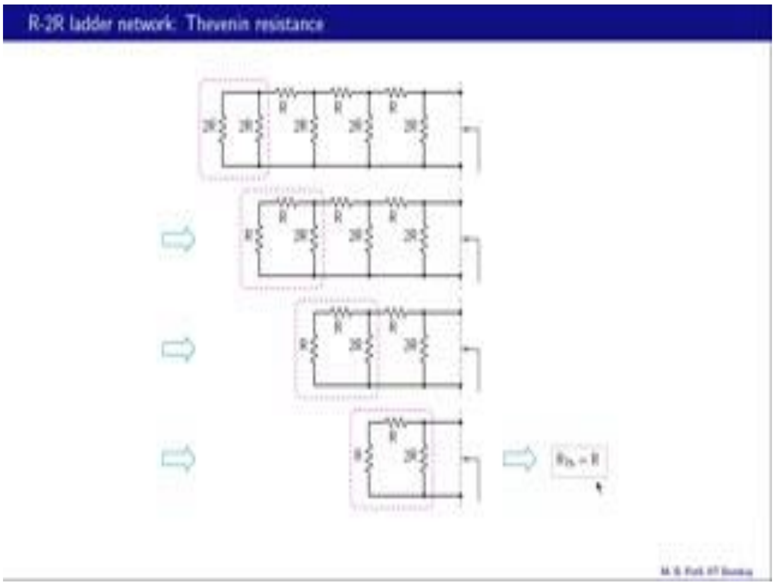

R-2R ladder network: Thevenin resistance

So, let us now find the Thevenin resistance of the R-2 R ladder network. And step number one; we deactivate the independent sources which we saw in the last slide. And after doing that we get this network here. What we can do to begin with is to combine these two registers 2 R parallel 2 R gives us R, so we get this circuit now. The rest of the circuit of course, remains the same, where R and R in series and that in parallel with 2 R; so that once again gives us R. And we can continue this process these three can again be combined to give us R like that and finally, these three can be combined to give us R. So, the Thevenin resistance as seen from here turns out to be R.

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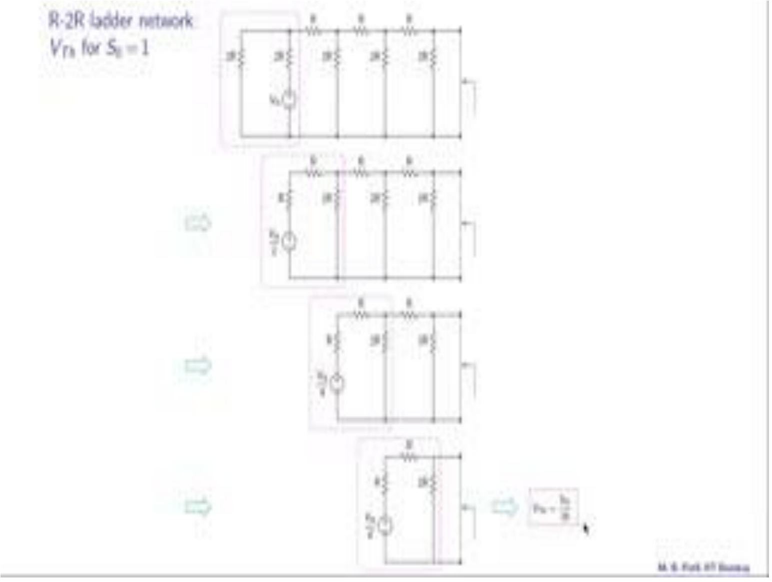

R-2R ladder network

V_{Th} for $S_0 = 1$

So, we have found the Thevenin resistance of the R-2 R ladder network. Next, let us find the Thevenin voltage corresponding to one specific bit equal to one with all others 0. If S 0 is 1, then this voltage source is V R; and the voltage sources that we had over here are all 0 so that means, there is a short circuit here. And now what we want to do is to find V Th as seen from this port. First we can replace this part with its Thevenin equivalent.

What is the Thevenin resistance as seen from here, it is just 2 R parallel 2R that is R. And what is the Thevenin voltage, the Thevenin voltage is the open circuit voltage here. So, we remove all of that and find this voltage between this node and this node. And then we see that there is a voltage division happening between these two resistances. So, this voltage will then be V R by 2. So, that is what we get. The Thevenin resistance is R of this part and the terminal voltage is V R by 2.

Now, we continue with this process. Note that this R and this R, R is series. So, this part looks exactly like this one with only one difference that is we have V R, V now here, V R by 2 over here. So, then we will get this Thevenin equivalent R and V R by 4. Next, we can replace this network, which is Thevenin equivalent. And we can anticipate that we are going to get R Th equal to R and V Th equal to half of this that is V R by 8 like that. Once again this network is exactly the same as any of these except the voltage supply is not V R by 8. So, we are going to get Thevenin resistance R Th equal to R for this entire network and a Thevenin voltage of half of this that is V R by 16.

So, that is our final answer. So, I have seen from here the Thevenin voltage is V R by 16.

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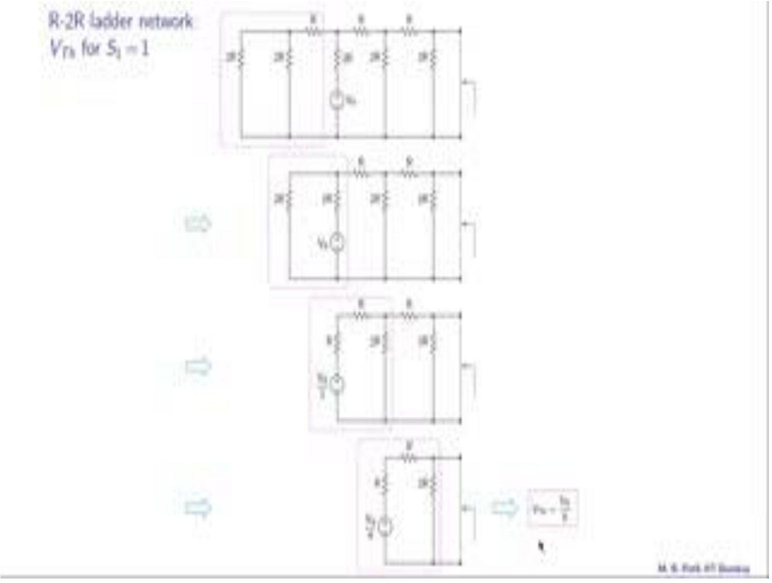

R-2R ladder network

V_{Th} for $S_1 = 1$

$V_{Th} = \frac{V_R}{8}$

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Next, let us consider S 1 to be 1, and all other bits equal to 0. So, we have V R here in the branch corresponding to S 1 and 0 volts here, here and here; that means short circuit. Once again, we want to find the Thevenin voltage as seen from here. Let us start with this network what is the Thevenin resistance it is 2 R parallel 2 R, which is R that in series with R, so that is 2 R. So, that is what we get and now we can replace this network with its Thevenin equivalent and they have done that in the last slide. So, we are going to get R Th equal to R, and V Th equal to half of this voltage like that.

Let us continue we can now combine these components and get R Th equal to R again and V Th equal to half of this that is V R by 4 like that. And then finally, we combine these to get R Th equal to R and V Th equal to V R by 8, so that is our final answer as seen from this port V Th is V R by 8.

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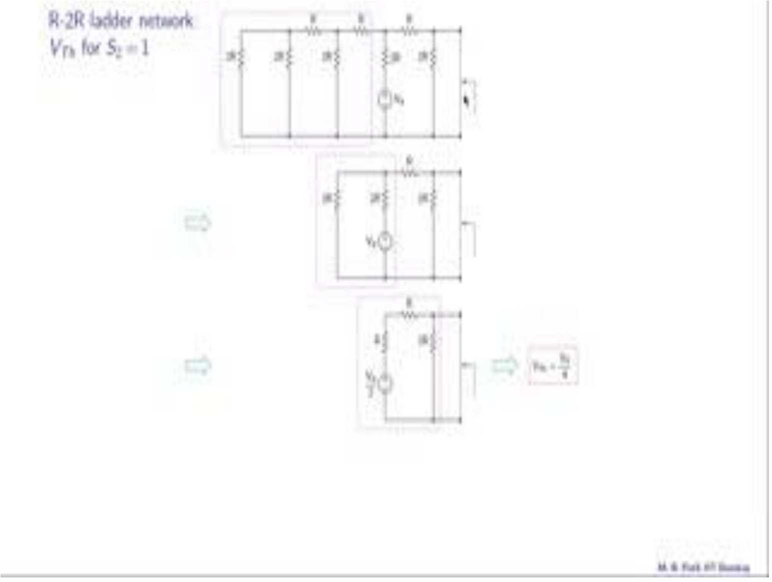

R-2R ladder network

V_{Th} for $S_2 = 1$

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Next, let us consider S 2 equal to 1 and all other bits equal to 0. So, the voltage supply is here now. To begin with we can combine all these registers 2 R parallel 2 R is R r plus R is 2 R then 2 R parallel 2 R again is R and R plus R is 2R. So, this entire network is equivalent to a single resistance 2 R like that. And now we can replace this network with R Th equal to R and V Th equal to V R by 2 like that.

And finally, we can replace this network by R Th equal to R, and V Th equal to half of this that is V R by 4, so that is our V Th as seen from there. And finally, let us consider S 3 equal to 1 and all other bits equal to 0. So, we have the voltage source here.

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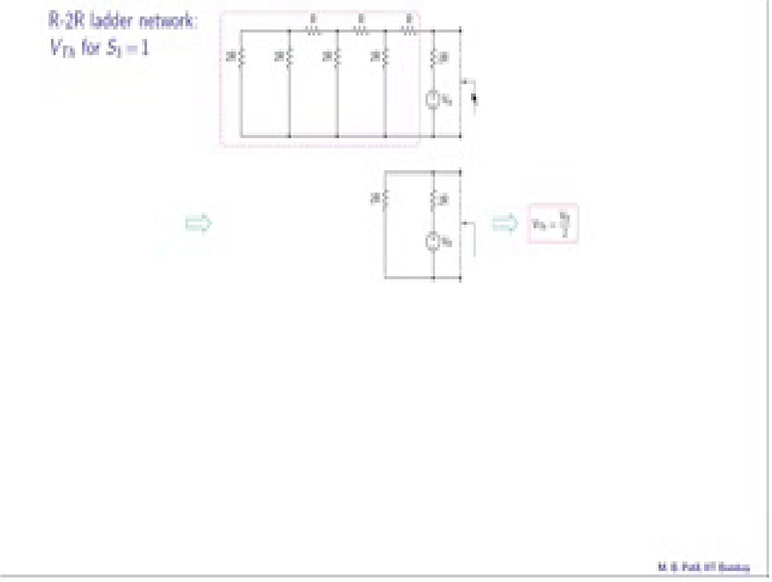

R-2R ladder network: V_{Th} for $S_3 = 1$

$V_{Th} = \frac{V_R}{2}$

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Now, V R and these voltage sources are 0, so short circuits. Now this entire network can be replaced with a single resistance 2 R, and you are encouraged to show that. So, this is what we get and now this network can be replaced with R Th equal to R and V Th equal to V R by 2 like that. So, as seen from here we have V Th equal to V R by 2.

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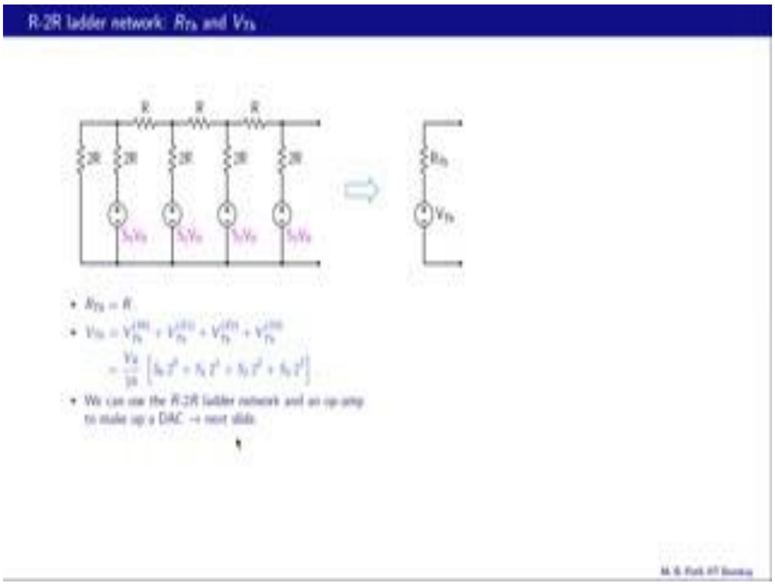

R-2R ladder network: R_{Th} and V_{Th}

- $R_{Th} = R$.
- $V_{Th} = V_{Th}^{(1000)} + V_{Th}^{(0100)} + V_{Th}^{(0010)} + V_{Th}^{(0001)}$

  $= \frac{V_R}{16}\left[S_0 2^0 + S_1 2^1 + S_2 2^2 + S_3 2^3\right]$
- We can use the R-2R ladder network and an op-amp to make up a DAC → next slide

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To summarize our original network this one can be replaced with this Thevenin equivalent R Th and V Th, where R Th is R, and V Th by superposition is the V Th arising from this source and V Th arising from this source and so on. So, then we get V

Th due to S 0 plus V Th due to S 1 etcetera. And when we add all of these, we get V R by 16 times S 0 2 raised to 0 plus S 1 2 raised to 1 plus S 2 2 raised to 2 plus S 3 2 raised to 3. And we can now use this R-2 R ladder network and an op-amp circuit to make up a DAC and we will see that in the next slide.

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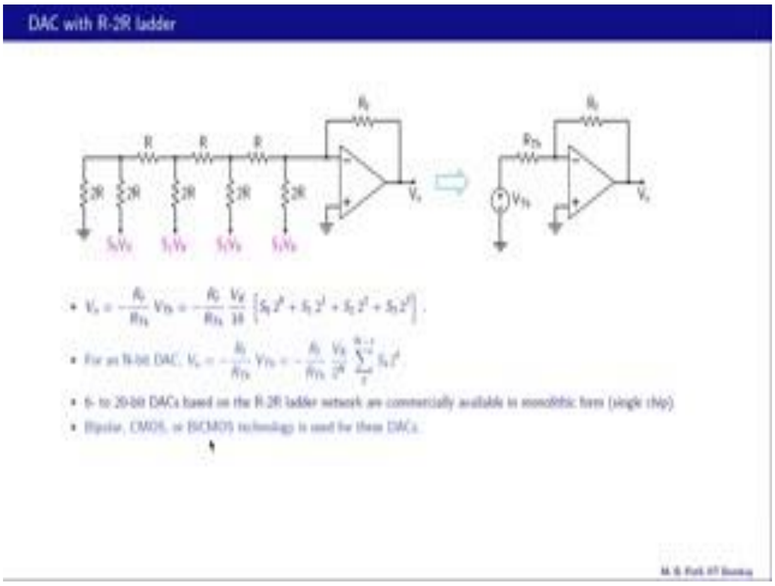

DAC with R-2R ladder

- $V_o = -\dfrac{R_f}{R_{Th}}V_{Th} = -\dfrac{R_f}{R_{Th}}\dfrac{V_R}{16}\left[S_0 2^0 + S_1 2^1 + S_2 2^2 + S_3 2^3\right]$.
- For an N-bit DAC, $V_o = -\dfrac{R_f}{R_{Th}}V_{Th} = -\dfrac{R_f}{R_{Th}}\dfrac{V_R}{2^N}\sum_{0}^{N-1} S_k 2^k$
- 6- to 20-bit DACs based on the R-2R ladder network are commercially available in monolithic form (single chip).
- Bipolar, CMOS, or BiCMOS technology is used for these DACs.

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So, here is a DAC circuit made with an op-amp. This is our R-2 R ladder network. And as we have already seen this entire network can be represented by its Thevenin equivalent R Th and V Th. So, now, the circuit looks like this. And this is nothing but an inverting amplifier. So, we have V o equal to minus R f by R Th times V Th as simple as that. So, we have V o equal to minus R f by R t s times V Th, and when we substitute for V Th in the last slide, we get this expression. And this can be extended to n bits, and we can then write for an n bit DAC V o is minus R f by R Th times V Th, which is minus R f by R Th V R by 2 raise to n summation 0 to n minus 1 S k 2 raise to k. Like we said earlier electronics is full of clever things and the R-2 R ladder network is definitely one of them.

Now, these DACs based on the R-2 R ladder network are commercially available ranging from 6 bit DACs to 20-bit DAC s and they are available as a single package that is in monolithic form single chip. And they can be made using the bipolar technology or the CMOS technology or a combination of the two, which is BiCMOS technology and negligee to say higher the number of bits more expensive is the IC.

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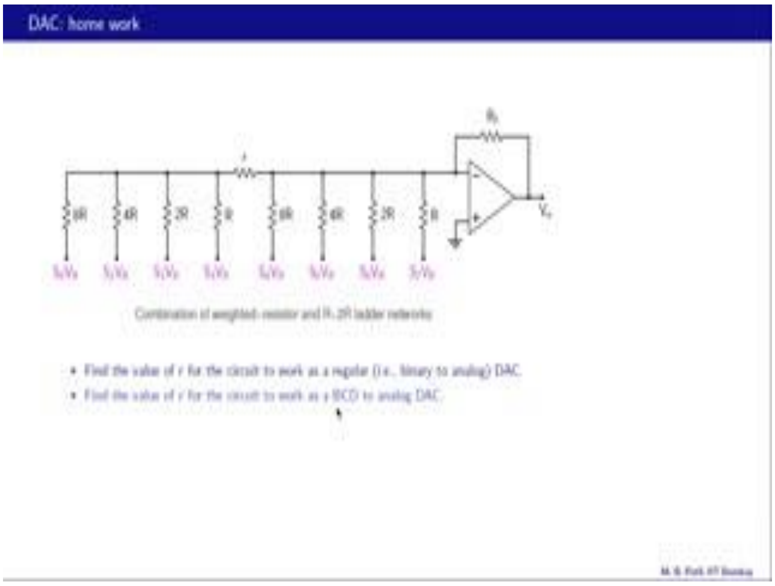

DAC: home work

Combination of weighted-resistor and R-2R ladder networks

- Find the value of r for the circuit to work as a regular (i.e., binary to analog) DAC.
- Find the value of r for the circuit to work as a BCD to analog DAC.

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Here is some homework for you. In this circuit, we have a combination of w8ed resistor and R-2 R ladder networks. So, here is our weighted registered array R-2 R 4R, 8R also here R-2 R, 4R, 8R. And you need to find the value of R this small R here for the circuit to work as a regular DAC that is binary to analog that would be an 8-bit DAC. This is the LSB S 0 and that is the MSB that is part 1. Part two find the value of small R for the circuit to work as a BCD to analog DAC.

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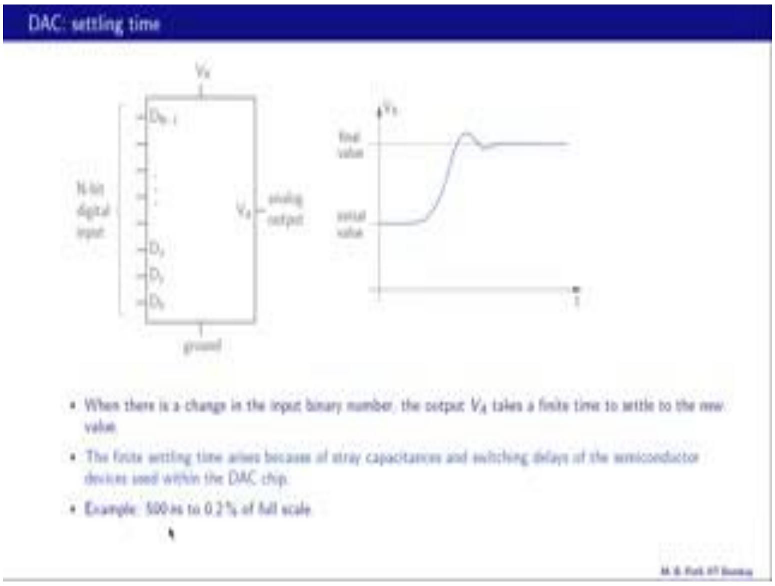

DAC: settling time

- When there is a change in the input binary number, the output V_A takes a finite time to settle to the new value.
- The finite settling time arises because of stray capacitances and switching delays of the semiconductor devices used within the DAC chip.
- Example: 500 ns to 0.2 % of full scale.

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There is a very important specification of a practical back and that is the settling time. Let us take a four bit DAC as an example. And let us say we are changing our binary input number from say 0 0 1 1 to 1 1 0 0. As a result of that our analog output is going to change this is our initial value and that is our final value. And it is going to take some time for this initial value to change to the final value. So, when there is a change in the input binary number, the output V A takes a finite time to settle to a new value. This finite settling time arises because of stray capacitances and switching delays of the semiconductor devices used within the DAC chip. And manufacturers will of course, strive to make this settling time as small as possible, but it cannot be made 0.

Now, this is how the settling time is specified in a datasheet. For example, 500 nanoseconds to 0.2 percentage of full scale. Let us see what this means let us say our initial value corresponding to our initial binary number is 1 volt, and the final value corresponding to the new binary number is 2 volts. So, our V A has to change from 1 volt to 2 volts. Suppose, our full scale is 10 volts and 0.2 percent of 10 volts is 20 millivolts so that means, to go from 1 volt to within 20 millivolts of 2 volts it is going to take 500 nanoseconds, so that is what this specification means.

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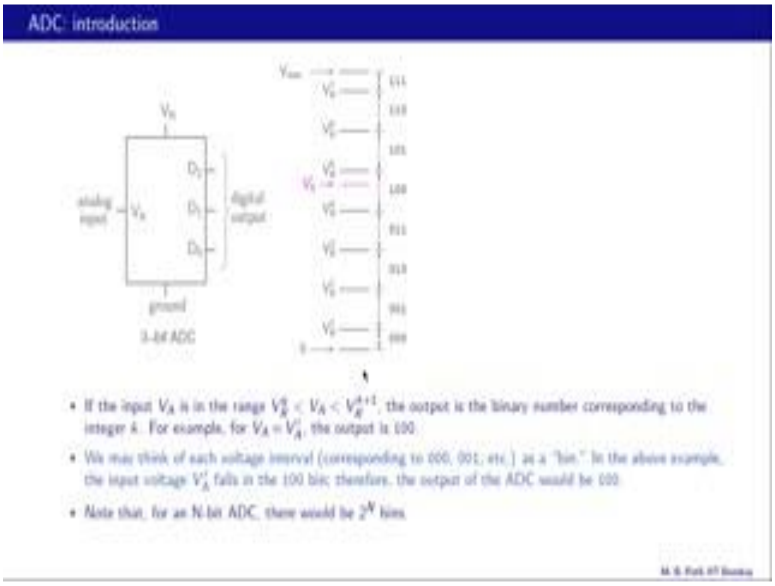

ADC: introduction

- If the input V_A is in the range $V_R^k < V_A < V_R^{k+1}$, the output is the binary number corresponding to the integer k. For example, for $V_A = V_A'$, the output is 100.
- We may think of each voltage interval (corresponding to 000, 001, etc.) as a "bin." In the above example, the input voltage V_A' falls in the 100 bin; therefore, the output of the ADC would be 100.
- Note that, for an N-bit ADC, there would be 2^N bins.

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We will now discuss analog-to-digital conversion. And let us take this example of a 3-bit ADC analog-to-digital converter. Here is the analog input which we will denote by V A and this is the digital output since its three bit ADC we have 3-bits here - D 2, D 1, D 0.

This is the MSB and that is the LSB. Apart from that, this ADC has two additional things ground and a reference voltage.

Here is a schematic diagram showing what an ADC should do. In this case we have a 3-bit ADC, so this interval between 0 and V max which is the same as V R is divided into 8 intervals that is 2 raised to 3; and these intervals are labeled 0 0 0, 0 0 1, 0 1 0 etcetera all the way up to 1 1 1. Now, the given input voltage V A prime is compared with each of these levels 0, V R 1, V R 2, V R 3 etcetera; and if it falls between these two levels for example, then the output of 1 0 0 is aside. So, this is the MSB. So, D 2 would be 1, D 1 would be 0, and D 0 would be 0.

Here is the summary. If the input V A is in the range V R k to V R k plus 1, the output is the binary number corresponding to that integer k - this one. For example, for V A equal to V A prime this V A prime, it fell between V R 4 and V R 5 and therefore the binary number corresponding to four which is 1 0 0 is assigned to the digital output. We may think of each voltage interval corresponding to 000, 001 etcetera, these intervals as a bin or a box. In the above example, the input voltage V A prime falls into 100 bin this bin here and therefore, the output of the ADC would be 100. And finally, note that for an N-bit ADC there would be two raised to N means; in this case there are 2 raised to 3 or 8 bins.

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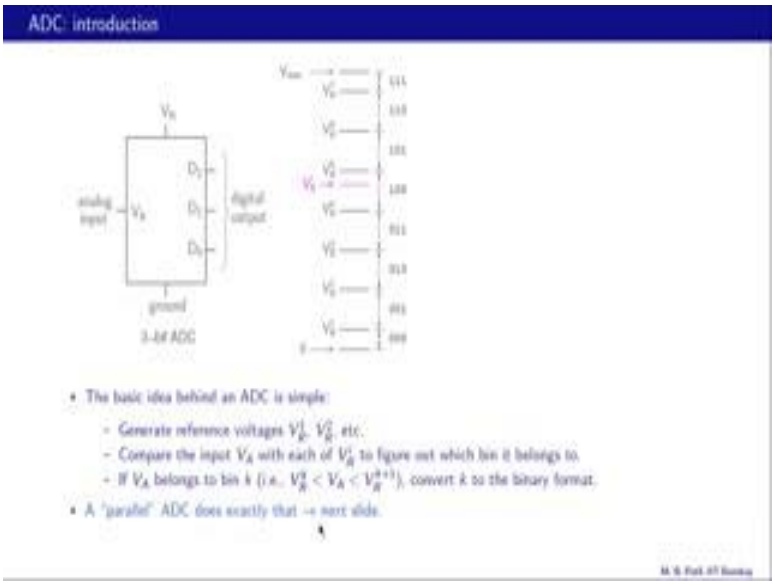

ADC: introduction

- The basic idea behind an ADC is simple:
  - Generate reference voltages V_R^1, V_R^2, etc.
  - Compare the input V_A with each of V_R^i to figure out which bin it belongs to.
  - If V_A belongs to bin k (i.e., $V_R^k < V_A < V_R^{k+1}$), convert k to the binary format.
- A "parallel" ADC does exactly that → next slide.

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So, the basic idea behind an ADC is quite simple. First, we generate reference voltages V R 1, V R 2 etcetera, and these levels. Then we compare the input V A with each of these reference voltages. To figure out which bin it belongs to. And if V A belongs to bin k then we converted k to the binary format and that is our ADC output. And parallel ADC does exactly that and let us see that in the next slide.

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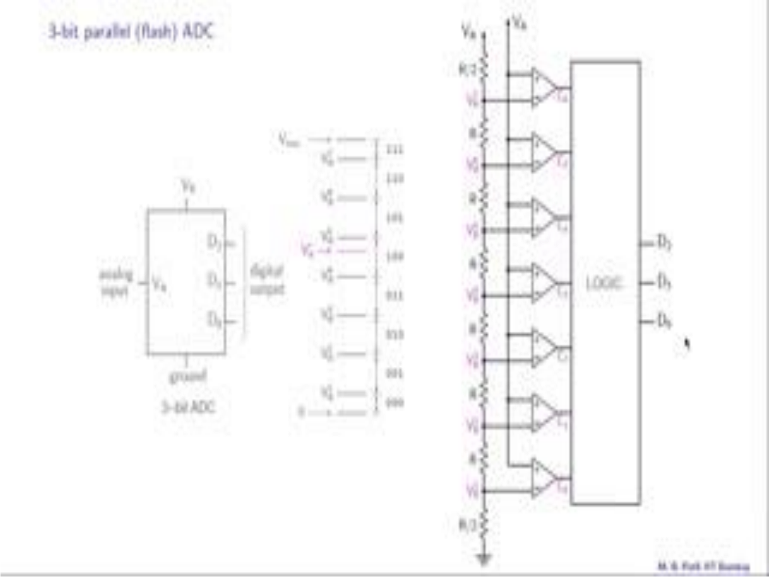

3-bit parallel (flash) ADC

Here is a schematic diagram of a 3-bit parallel of flash ADC and let us see how it works. Let us look at these figure, we need to generate V R 1, V R 2 up to V R 7 that is 7 reference voltages, and that is done by this register network over here. For example, V R 1 would be R by 2 divided by this total resistance multiplied by V R. What is the total resistance? We have R by 2 here. Then we have six of these Rs so that means 6 R and another R by 2, so that is seven R in all. So, V R 1 would be R by 2 divided by 7 R times V R. V R 2 would be 3 R by 2 divided by 7 R times V R and so on. Next, we have these comparators; one input for all comparators is common that is the plus input and that is connected to the applied analog voltage V A; the second input the minus input is V R 1 for this comparator; it is V R 2 for this comparator and so on.

Now, let us take an example let us say that V A is this V A prime which falls between V R 4 and V R 5. So, the output of this comparator which is denoted by C 3 is going to be 1. In this case because V A is greater than V R 4 C 2 also is going to be 1, because V A is also greater than V R 3; and C 1, C 0 are also going to be 1. On the other hand, C 4 is going to be 0, because V A is less than V R 5; and also C 5 and C 6 are going to be 0. So, we have 000 1111. And now we have this logic which can figure out what combination this situation should correspond to and output of this logic is D 2, D 1, D 0 that is our ADC output, so that is how this parallel or flash ADC works.

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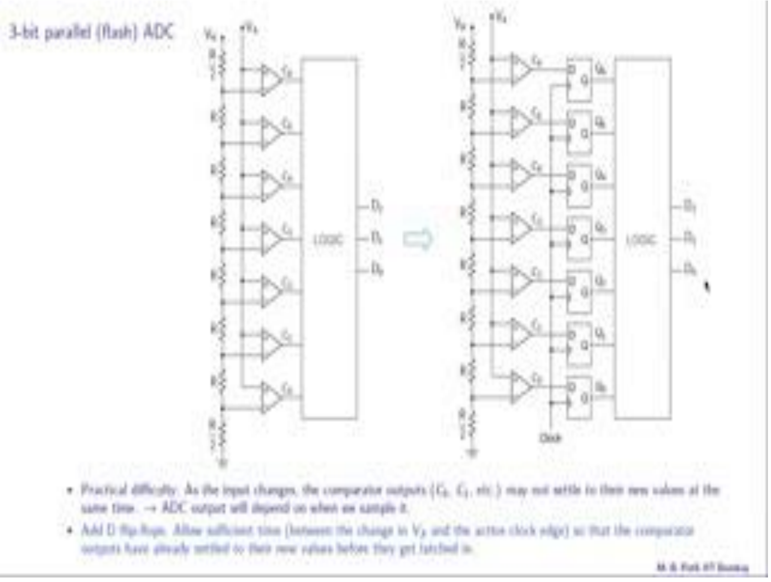

3-bit parallel (flash) ADC

- Practical difficulty: As the input changes, the comparator outputs (C_6, C_5, etc.) may not settle to their new values at the same time. → ADC output will depend on when we sample it.
- Add D flip-flops. Allow sufficient time (between the change in V_A and the active clock edge) so that the comparator outputs have already settled to their new values before they get latched in.

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So, this circuit which we saw in the last slide represents a 3-bit parallel ADC, but there is a practical difficulty with this circuit and that is as the input changes, the comparator outputs C 0, C 1 etcetera. These outputs may not settle to their new values at the same time this might settle earlier, this might settle later and so on. And therefore, the ADC output will depend on when we actually sample D 2, D 1, D 0 and that is not desirable. And to circumvent that difficulty, what we do is add D flip-flops as shown over here, allow sufficient time between the change in V A and the active clock edge. So, that the comparator outputs have already settled to their new values before they get latched in. So, what does it mean?

Let us take an example. Let us say this comparator takes 50 nanoseconds to settle down that means, when we change V A from V A 1 to V A 2, from that time it takes 50 nanoseconds or less for all of these outputs to settle down. In that case, we can make sure that our active clock edge here is 50 nanoseconds after the analog voltage has changed. And then we are sure that these values Q 0, Q 1, Q 2 etcetera are consistent with the new analog voltage V A 2, and then we get the correct D 2, D 1, D 0 at the output.

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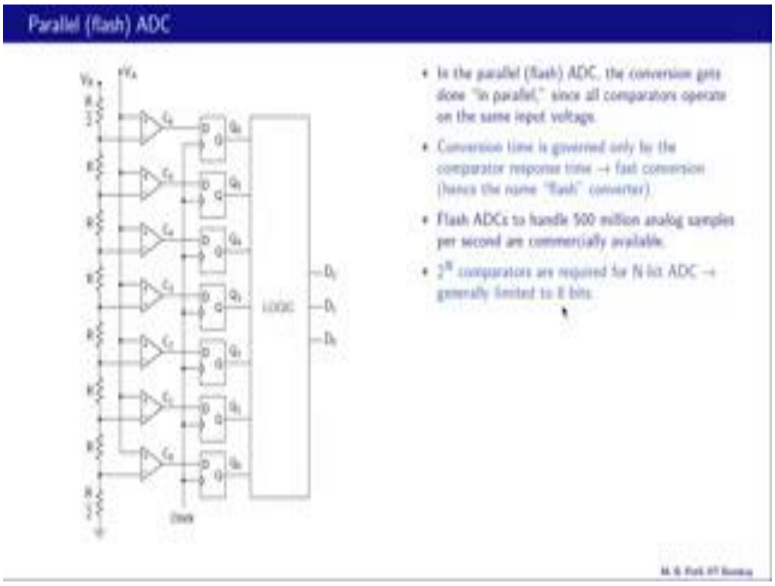

Parallel (flash) ADC

- In the parallel (flash) ADC, the conversion gets done "in parallel," since all comparators operate on the same input voltage.
- Conversion time is governed only by the comparator response time → fast conversion (hence the name "flash" converter).
- Flash ADCs to handle 500 million analog samples per second are commercially available.
- 2^N comparators are required for N-bit ADC → generally limited to 8 bits.

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Let us make a few remarks about the parallel or flash ADC. In the parallel ADC, the conversion gets done in parallel since all comparators operate on the same input voltage that we have already seen, all of these comparators get the same input voltage as V plus. Conversion time is governed only by the comparator response time and that makes the conversion very fast here is the name flash converter. The conversion happens in a flash that is why the name flash converter. Flash ADCs to handle 500 million analog samples per second are commercially available, so that is how fast these flash ADCs can get.

What is the disadvantage? We need 2 raise to N comparators strictly speaking 2 raise to N minus 1 for an N bit ADC. Here we have N equal to 3, and we require seven comparators which is 2 raised to C minus 1. So, as N grows this number becomes very large in practically large, and therefore, these parallel or flash ADC are generally limited to 8-bits.

To summarize we have looked at the R-2 R ladder network and its advantage over the weighted binary registered array. We have seen how a DAC can be constructed using the R-2 R ladder network. We then started our discussion of analog-to-digital conversion. After looking at the basic idea of A to D conversion, we looked at one implementation namely the flash ADC. We found that the flash ADC is fast, but it requires a large number of comparators. In the next lecture, we will look at other ADC types, which offered a larger number of bits that is a higher resolution at the expense of speed. So, see you next time.