Basic Electronics
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Lecture - 70
Digital-to-Analog conversion

Welcome back to Basic Electronics. We now start with a new topic namely interface between the analog and digital domains we will look at the basic functionality of a digital to analog converter or DAC we will then look at a DAC implemented using binary weighted registers and work out various quantities of interest for an example let us begin.

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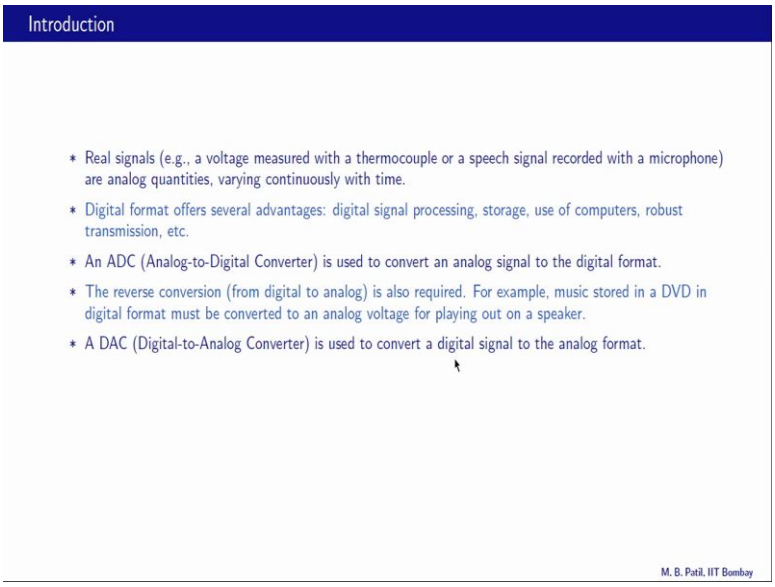

We will now discuss analog-to-digital conversion and digital-to-analog conversion and let us begin with the motivation behind this kind of conversion why do we need this conversion in the first place. So, here are some points real signals for example, a voltage measured with the thermocouple or a speech signal recorded with a microphone or analog quantities varying continuously with time. On the other hand the digital format as we have seen earlier offers several advantages such as digital signal processing, storage, use of computers, robust transmission etcetera.

Therefore, it makes sense to convert these real signals, that is the analog signals to the digital format and then take advantage of all of these features that the digital format offers. An ADC is just that an ADC which stands for Analog-to-Digital converter is used

to convert an analog signal to the digital format, all right. Now the reverse conversion from digital to analog is also required for example, music stored in a DVD in the digital format must be converted to an analog voltage for playing out on a speaker that is how we hear that music and that conversion is done by a DAC, a DAC which stands for digital to analog converter is used to convert a digital signal to the analog format.

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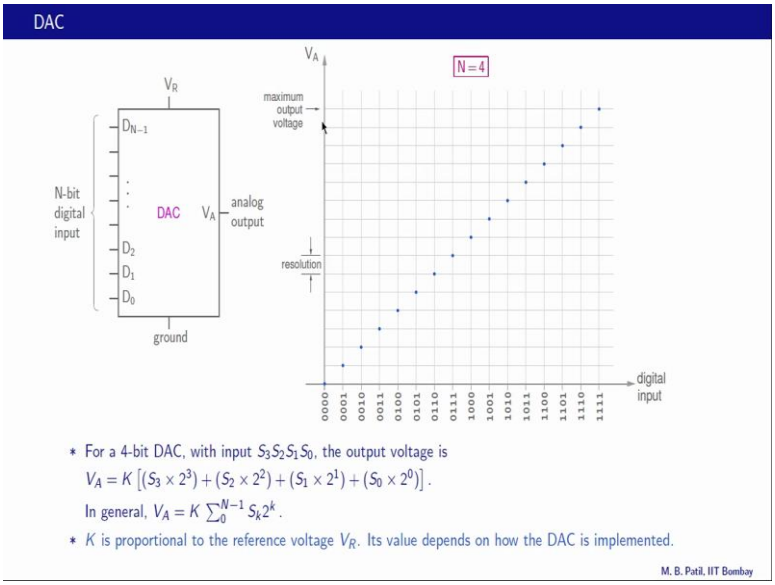

Here is the schematic picture of a DAC that is Digital-to-Analog converter, this is the digital input that is the analog output then we have ground and a reference voltage from the chip. The digital input as N bits D 0, D 1, D 2 up to D N minus 1. Now depending on the values of this binary number and this reference voltage the DAC will produce an analog voltage output. Here is an example for a 4 bit DAC; that means, N is 4 here with input S 3, S 2, S 1, S 0 that corresponds to D 3, D 2, D 1, D 0. The output voltage is V A equal to K some constant times S 3 which can be 1 or 0 times 2 raise to 3 plus S 2 which again can be 1 or 0 times 2 raise to 2 plus S 1 times 2 raised to 1 plus S 0 times 2 raised to 0.

And in general we can write this equation as V A equal to K summation from 0 to N minus 1 S k times 2 raised to K. So, the important thing to notice here is each bit gets a different weight the higher bits get a higher weight and lower bits get a lower weight and this scaling factor K here is proportional to the reference voltage V R this one, its value depends on how the DAC is implemented.

Now, let us look at how V A varies the output voltage here as a function of the digital input that we apply to the DAC or diagram and we will take the same example again where N is 4. So, it is a 4 bit DAC. So, here is our digital input the first number is 0 0 0 0 then 0 0 0 1, 0 0 1 0 etcetera all the way up to 1 1 1 1. So, this is decimal 0, this is decimal 1, 2, 3, 4 etcetera up to 15 and as a result of this applied input the output voltage V A varies from 0 to some maximum output voltage. And note particularly that we do not have a straight line here or a curve we have only discrete points and that is because our input is discrete there are only these 16 values and that in between 2 values for example, there is no digital input between this number and that number.

So, that is why we see points here and not lines or curves all right. Now this difference between 2 successive output values is called the resolution of the (Refer Time: 06:17). Now the number of bits of the DAC and the maximum output voltage we can easily figure out the resolution because we know that there are 2 raise to N minus 1 divisions over here in this case for example, we have 2 raise to 4 minus 1 that is 16 minus 1 or 15 divisions between the lowest and the highest values. So, then we can calculate the resolution as the maximum output voltage divided by 15 in this case.

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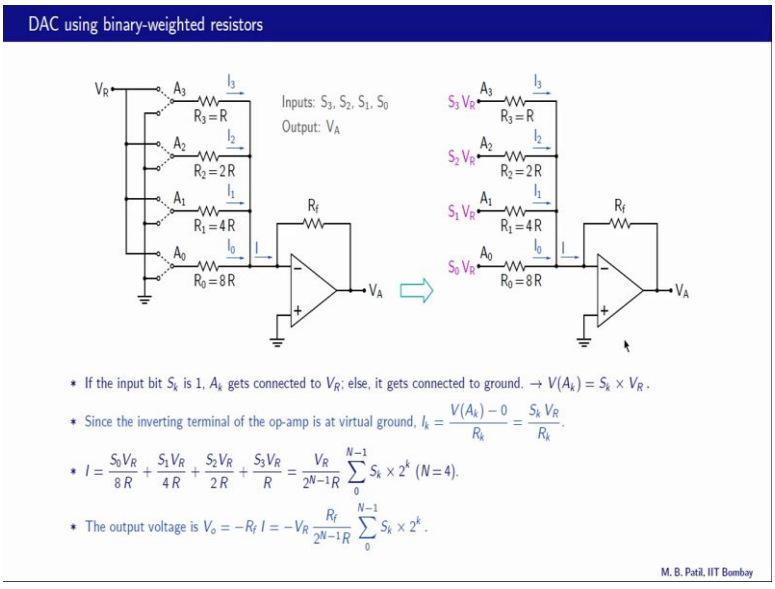

Let us now talk about implementation of our DAC and our first approach is to use binary weighted registers what is the meaning of this term? If 1 resistance is, then the next 1 is 2 times that that is 2 R the next 1 is 2 times 2 R that is 4 R and then 8 R and so on all right.

Now this specific example is a 4 bit DAC the inputs are S 3, S 2, S 1, S 0. So, S 3 can be 0 or 1, S 2 can be 0 or 1 and so on. The output is V A the output of this op amp here, we have 4 switches here which are controlled by the input bits S 3, S 2, S 1 is 0 this switch for example, is controlled by S 3, if S 3 is 0 then this node a 3 gets connected to ground like that and if S 3 is ground then A 3 gets connected to this reference voltage V R.

In other words the voltage at this node is S 3 times V R if S 3 is 0 then that voltage is 0 and if S 3 is 1 then that voltage is V R and that is what we have shown over here and similarly this switch is controlled by S 2 and therefore, this voltage is S 2 times V R. This one is controlled by S 1 therefore, this is S 1 times V R and this one is S 0 times V R. So, that is our simplified circuit and we see that it is our op amp summer and let us now see how that works.

Since V minus and V plus are equal we have V minus equal to 0 and therefore, this current can be calculated and this current is nothing, but I 0 plus I 1 plus I 2 plus I 3, I 0 is S 0 V R minus 0 divided by 8, R 1 is S 1 V R minus 0 divided by 4 R and so on. So, that gives us this expression here. So, the current I is S 0 V R by 8 R plus S 1 B R by 4 R etcetera and now what we can do is to take this V R by 8 R common and then get this expression here now here we have written a general expression for N bits in our case N is equal to 4.

So, this 2 raise to N minus 1 is in our case, 2 raise to 3 which is the same as 8. So, this is what we get and as we expect each bit gets a different weight for example, the LSB S 0 gets a weight of 2 raise to 0 or 1 and the MSB S 3 in our case gets a weight of 2 raise to 3 or 8 and that is what we would expect from a DAC.

Finally, let us find the output voltage V A here we have done that earlier when we talked about op amp circuits - this V minus is 0 volts and there is no current going into the op amp therefore, this current I also goes through R f and therefore, V A which is our output voltage V o is 0 minus I times R f and that is what we have over here minus R f times I and I comes from this expression and therefore, this is what we get for the output voltage.

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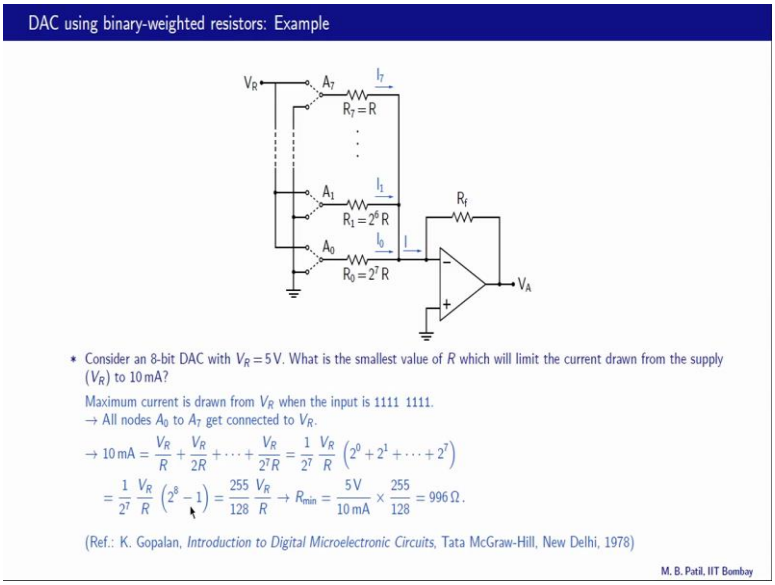

Let us take a specific example, consider an 8 bit DAC with V R equal to 5 volts, what is the smallest value of R? that resistance which will limit the current drawn from the supply to 10 milliamps, this is our supply V R and that is supplying all these currents and the total current that we draw from the supply it should be limited to 10 milliamps. Now since this is an 8 bit DAC our resistance values go from R, 2 R, 4 R etcetera then 2 raise to 6 R and the last value is 2 raise to 7 R.

Otherwise the circuit is the same as what we saw earlier we have a total of edge which is now in the circuit this switch is controlled by the LSB that is S 0 this switch is controlled by S 1 and so on and finally, this switch is controlled by S 7 which is the MSB. Now let us look at these currents I 0, I 1 etcetera up to I 7. Now this node is that virtual ground V minus and V plus, is nearly equal. So therefore, we have 0 volts here this current R 0 is given by the potential at this node a 0 minus 0 divided by R 0 it is 2 raise to 7 R and similarly we can get these other currents.

When S 0 is 0 this switch is in this position node a 0 is at ground and therefore, I 0 would be 0 on the other hand if S 0 is 1 then the switch is in that position the potential here is V R and then we do have a current V R divided by R 0. In other words this register is drawing a current from the power supply only if S 0 is 1, similarly this resistor will draw a current from the power supply if S 1 is 1 and for the power supply to supply the maximum current clearly we require S 0 equal to 1, S 1 equal to 1 etcetera all the way up

to S 7 equal to 1. So, that is what we have written over here. Maximum current is drawn from V R when the input is 1 1 1 1, 1 1 1 1 that is all loads a 0 to a 7 get connected to V R.

And that maximum current is restricted to 10 milliamps so therefore, we equate 10 milliamps to V R by R that is the current through this resistance plus V R by 2 R the current through the next resistance and so on all the way up to V R by 2 raise to 7 R that is this correct and we can take V R by 2 raise to 7, R common and get 2 raise to 0 plus 2 raise to 1 plus 2 raise to 2 etcetera up to 2 raise to 7 and this bracket turns out to be 2 raise to 8 minus 1 that is 256 minus 1, 2 raise to 7 is 128 so therefore, we end up with 255 by 128 times V R by R and that should not exceed 10 milliamps and that gives us the value of R the minimum value of R. So, that is V R which is 5 volts divided by 10 milliamps times 255 by 128 and that turns out to be about 1 kilo ohms.

Now, this example has been taken from this book by Gopalan and it has many other interesting details about DACs and ADCs and it is a good book to look at.

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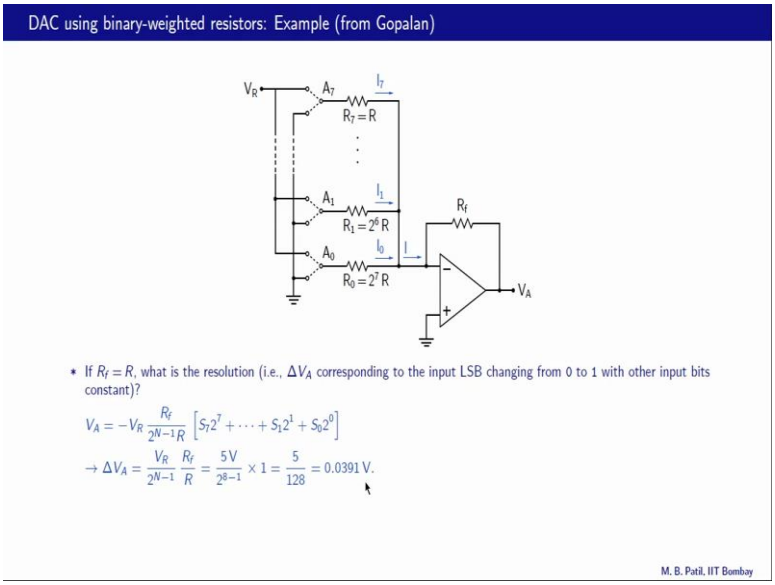

Next question, if R f is equal to R what is the resolution that is delta V A change in V A here corresponding to the input LSB changing from 0 to 1 with all other input bits kept constant all right. So, this is our expression for V A and this bracket corresponds to the input binary number, what is the lowest value of this bracket? That happens when S 0 is 0, S 1 is 0 etcetera all the way up to 7 equal to 0. So, that lowest value is 0 what is the

highest value? Highest value is when S 0 is 1, S 1 is 1 etcetera all the way up to S 7 is 1 and that highest value is 255 or 2 raise to 8 minus 1.

And when we talk about resolution what it means is we are allowing the change in this bracket by 1 and that is the same as saying that it is delta V A corresponding to the input LSB this S 0 here changing from 0 to 1 with other input bits constant. You can now calculate the resolution. So, the resolution which is delta V A when this bracket changes by 1 is given by this factor here which is reproduced here and that is 5 volts that is V R 2 raise to 8 minus 1 this number here times R f by R and R f and R are going to be equal so therefore, this turns out to be 0.0391 volts or 39.1 millivolts.

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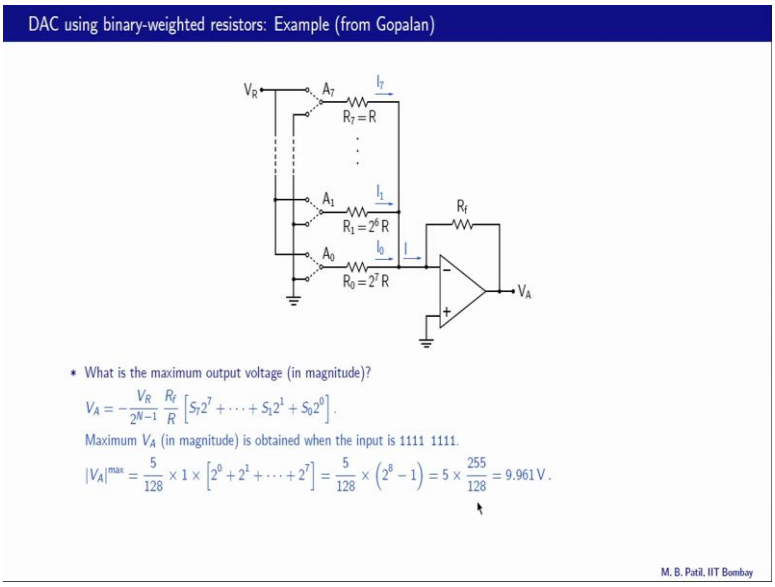

Next question what is the maximum output voltage in magnitude here is our V A and note that it is negative and that is why we have put magnitude in brackets over here and when does the magnitude become maximum? That happens when the bracket becomes maximum that means, all these bits are equal to 1. So, the maximum V A in magnitude is obtained when the input binary number is 1 1 1 1, 1 1 1 1. So, all we need to do now is to replace all these S's by 1 and evaluate this bracket and that is what we get - V R is 5 volts 2 raise to N minus 1 is 128 R f and R are equal.

So, that is one and this bracket is then 2 raise to 0 plus 2 raised to 1 all the way up to 2 raise to 7 and when we evaluate that we get 9.961 volts.

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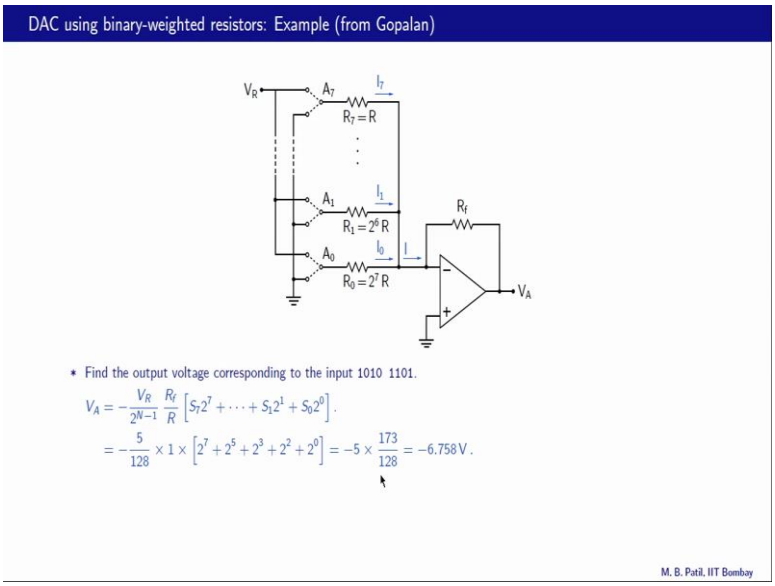

Next find the output voltage corresponding to the input binary number 1 0 1 0 1 1 0 1 fairly straight forward to do we have V A here, all we need to do now is to put S 7 equal to 1, S 6 equal to 0, S 5 equal to 1, S 4 equal to 0 and so on and that is what we get. So, V A turns out to be minus 6.758 volts.

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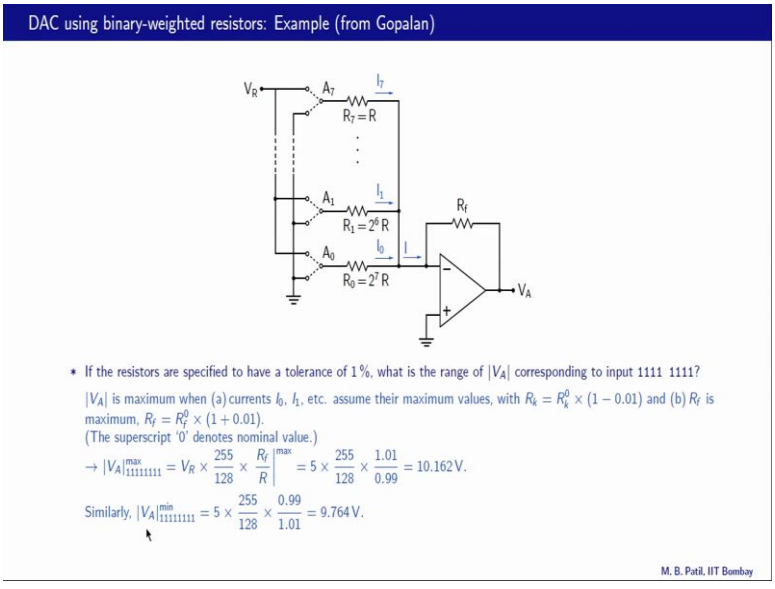

Next question, if the resistors are specified to have a tolerance of 1 percent what is the range of mod V A corresponding to the input 1 1 1 1, 1 1 1 1. Now first let us figure out what this means a tolerance of 1 percent take this resistance for example, let us say it is

nominal value is 1 k then what this means is that the actual value can be anything between 0.99 times 1 k to 1.01 times 1 k. What about this resistance? We will assume that R and R f are the same, therefore, the nominal value of R 7 is also 1 k and therefore, the actual value will vary from 0.99 k to 1.01 k.

What about this resistance? Is nominal value is 2 raise to 6 times r; that means, 64 times 1 k or 64 k and its actual value can vary from 64 k times 0.99 to 64 k times 1.01. Let us now get back to our original question and with this input all our switches are in the upper position; that means, A 7 is connected to V R, A 1 is connected to V R etcetera and all of these currents now are nonzero. Now for V A to be maximum in magnitude all of these currents must take on their maximum values and that happens when these resistances take on their minimum values that is condition number 1, second condition is that this current which is addition of all of these currents.

Now, passes through this R f and this R f times I should also take on its maximum value; that means, R f should take its maximum value. Once we realize that then it is straightforward to calculate V A max. So, mod V A is maximum when a current is I 0, I 1 etcetera assume their maximum values with R k equal to R k 0 that is the nominal value times 1 minus 0.01 that is 0.99. So, the resistance is these resistances take on their minimum values that are how these currents become maximum.

And second R f is maximum that is R f is equal to which nominal value times 1.01. So, the maximum value of mod V A for this condition is then V R times 255 by 128 this gets in earlier times the maximum value of this ratio R f by R; that means, 1.01 divided by 0.99 because their nominal values are equal they cancel out and that gives us 10.162 volts. What about the minimum value of mod V A? That is just the opposite we want to make these numbers now as small as possible. So, R f should take on its lowest value and all these resistances should take all their maximum values. So, that gives us this same factor times 0.99 divided by 1.01 that is 9.764 volts.

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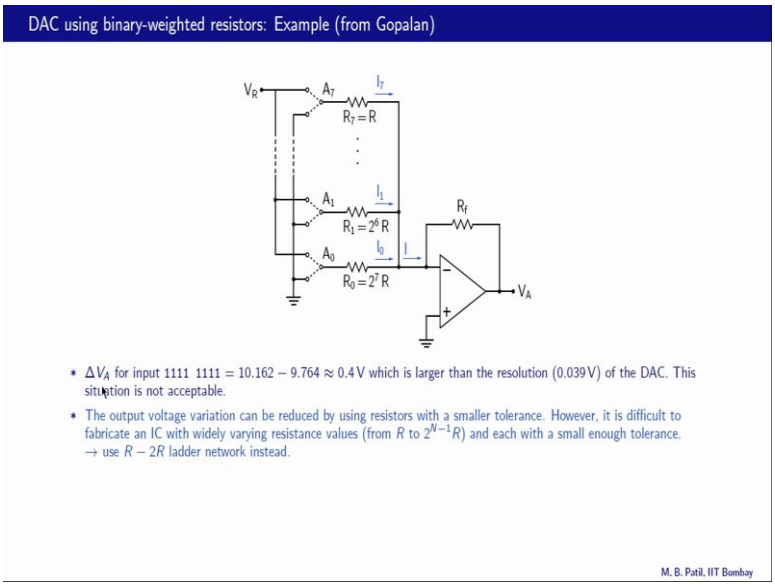

So, as we found in the last slide for a fixed input combination such as 1 1 1 1, 1 1 1 1 the output voltage can vary substantially because our resistances are not perfect they are nonzero tolerance and in the last example we found that the maximum V A in magnitude was 10.162 and the minimum was 9.764 and the difference between these 2 is about 0.4 volts which is quite significant because it is much larger than the resolution of the DAC which was 39 millivolts.

So, this situation is clearly not acceptable because it will lead to inaccuracies and what can we do to improve this situation? We can use resistances with a more tight tolerance. So, the output voltage variation can be reduced by using registers with a smaller tolerance; however, it is difficult to fabricate and IC with widely varying resistance values such as R 2 128 times R and each with a small enough tolerance.

So, there is a technological difficulty there and therefore, this entire design needs to be improved upon. The solution is to this the so called R 2 R ladder network, in this network we have only 2 resistance values R and 2 R. So, all registers in this network will be either R or 2 R and in this manner this problem of delta V A arising out of variation in resistance values gets effectively addressed.

To summarize we have started looking at digital to analog converters we looked at an implementation using the binary weighted resistor approach we considered an 8 bit DAC example and worked out various quantities of interest. We found that statistical

variations in the resistance values make this type of DAC unsuitable when the number of bits is large. In the next class we will look at the R 2 R ladder approach which circumvents this difficulty. See you next time.