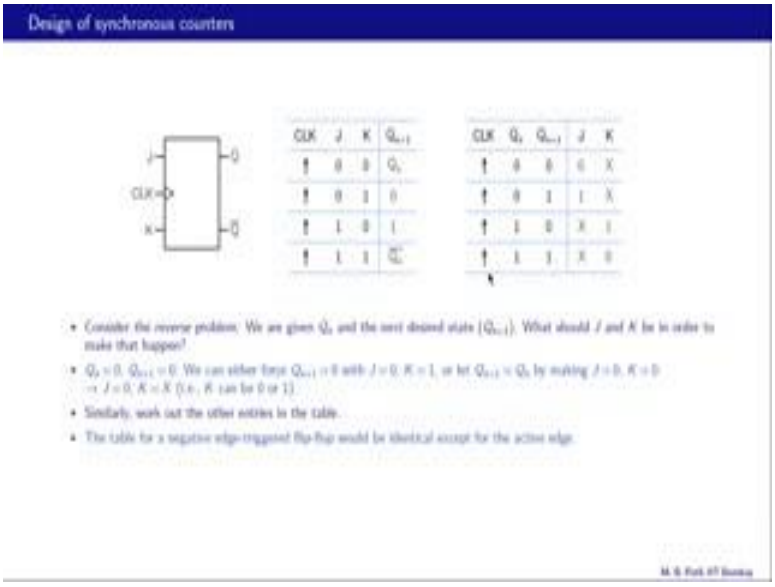
Basic Electronics
Prof. Mahesh Patil
Department of Electrical Engineering
Indian Institute of Technology, Bombay

Lecture - 67
Counters (continued)

Welcome back to Basic Electronics. We have looked at a synchronous counter in the last lecture, and worked out it is state transition table. We will now look at the reverse problem, that is given the state transition table how do we design a synchronous counter, which follows the table. We will then look at how 2 counters can be combined. Let us begin.

(Refer Slide Time: 00:46)



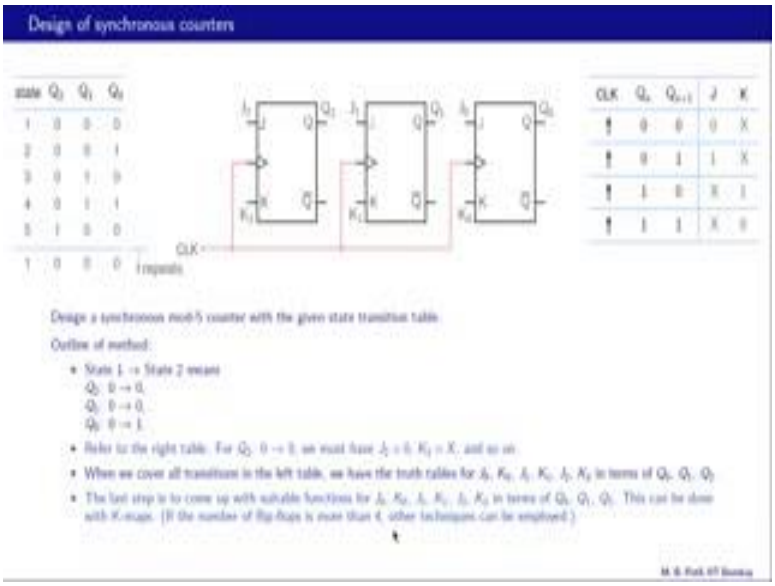
Let us now discuss how to design synchronous counters. We start with this transition table for a JK flip-flops, and here we have taken a positive edge triggered flip-flops so therefore, these active clock edges are shown to be positive edges. So what is this table about it says that if we have J equal to 0 and K equal to 0 then our Q N plus 1 is going to be the same as Q n. If we have J equal to 0 K equal to 1 then our Q N plus 1 is going to be 0 and so on. Now when we talk about design we need to consider the reverse problem. That is we are given Q N and we are given the next desired state that is Q N plus 1, and then what should J and K be in order to make this happen that is the question we ask.

Let us take a specific example. Let us say our Q N is 0 and we want our Q N plus 1 also to be 0 all right. How can we achieve that? We can do 2 things: one, we can have J equal to 0 K equal to 1 that way we ensure that Q N plus 1 is 0 that is the output just after the active edge. Or we can have J equal to 0 and K equal to 0 that will make Q N plus 1 equal to Q N and since Q N is already 0 Q N plus 1 will also be 0. What it means is we must have J equal to 0 and our K can be either 0 or 1, that is K is a do not care condition. And that is how we indicate the choice of J and K. So J is 0 K is X for Q N to be 0 and Q N plus 1 also to be 0. Now let us consider this next case, if Q N is 0 and Q N plus 1 is required to be 1 then what can be do. One thing we can do is have J equal to 1 K equal to 0 that will first Q N plus 1 to be 1. The second option is we see that this Q N is toggling here and therefore, we can have this last J and K values. Let me say equal to 1 and K equal to 1. So these are the 2 options we have; that means, J must be equal to 1 and K is a do not care condition like that.

For Q N equal to 1 and Q N plus 1 equal to 0, we can either use this row of the table or we can use this row in which Q toggles. And that suggests that K must be equal to 1 and J is a do not care condition like that. And finally, for Q N equal to 1 and Q N plus 1 also equal to 1, we can either use this row or we can use this row in which Q does not change that gives us K equal to 0 and J is a do not care condition like that.

So, this is the complete table. And it tells us what J and K should be if Q N and Q N plus 1 are given. And this table can be used for designing a counter with a specific sequence and we will take a look at an example soon all right. What if this flip-flops is a negative edge triggered flip-flops rather than a positive edge triggered flip-flops? The table would be identical except for the active edge. So here we will have a negative clock edge rather than a positive clock edge apart from that these entries will remain identical.

(Refer Slide Time: 05:04)

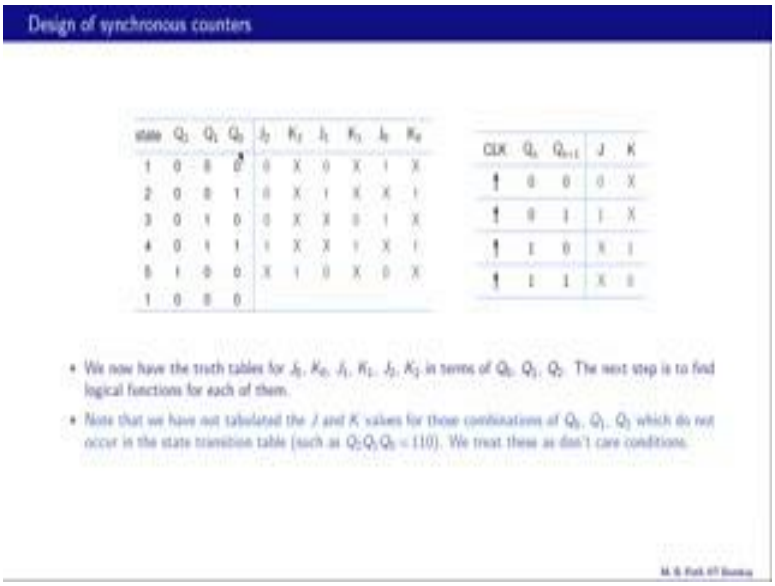


Let us take up this design problem now. Design a synchronous mod 5 counter with the given state transition table. What is the meaning of synchronous; that means, the same clock is going to all flip-flops we have 3 flip-flops here, their outputs are Q 2 Q 1 Q 0 and the corresponding inputs are J 2 K 2 J 1 K 1 and J 0 K 0. And here is the straight transition table that our counter must satisfy. We start in state 1, which is Q 2 equal to 0 Q 1 equal to 0 Q 0 equal to 0, then state 2 0 0 1 followed by 0 1 0 0 1 1 1 0 0 and then back to 0 0 0.

Here is an outline of the method that we will use. First let us see the meaning of state 1 changing to state 2 what does that mean; that means, we are going from this state to this state, that is Q 2 is changing from 0 to 0 Q 1 from 0 to 0 Q 0 from 0 to 1, that is the meaning of state 1 going to state 2 all right. Now what we do is refer to this table on the right hand side this 1, let me saw on the last slide. Now for Q 2 to go from 0 to 0 we look at this entry Q N is equal to 0 Q N plus 1 equal to 0. Then we require J 2 equal to 0 and K 2 equal to X and so on. When we cover all transitions in the left table, here we have the truth tables for J 0 K 0 J 1 K 1 and J 2 K 2 in terms of Q 0 Q 1 Q 2, and the last step is to come up with suitable functions for J 0 K 0 J 1 K 1 J 2 K 2 in terms of Q 0 Q 1 Q 2.

And this can be done with K-maps as we have seen earlier if the number of flip-flops is more than 4, then we cannot use K-maps and then other techniques can be employed.

(Refer Slide Time: 07:30)



Let us get started. Here is our table for J and K from given Q N and Q N plus 1. Let us start with the first change that is from state 1 to state 2. And let us consider Q 2 first Q 2 is changing from 0 to 0, will look at this row Q N is 0 Q N plus 1 is also 0. Therefore, J is 0 K is X. J is J 2 here and K is K 2. So therefore, we write 0 and X over here. What about Q 1, the same transition so 0 X again for J 1 K 1. What about Q 0? Q 0 goes from 0 to 1 so will look at this row our table and find that J 0 must be 1 and K 0 must be X like that. Let us consider the next transition now from state 2 to state 3. Q 2 goes from 0 to 0, so we have 0 X for J 2 K 2, Q 1 goes from 0 to 1, so we have one X for J 1 K 1 and Q 0 goes from 1 to 0 so we have X 1 for J 0 K 0 and so on.

And proceeding in that manner, we now have the truth tables for J 0, K 0, J 1, K 1 and J 2, K 2 in terms of Q 0 Q 1 Q 2 this table here. The next step is to find logical functions for each of them. And note that we are not tabulated the J and K values for those combinations of Q 0 Q 1 Q 2 which do not occur in the state transition table for example, this combination Q 2 Q 1 Q 0 equal to 1 1 0 is not present over here. So therefore, these combinations can be treated as do not care conditions. Now in this table we have 5 distinct states out of the 8 binary numbers that we can make up with 3 variables and therefore, there would be 3 do not care conditions.

(Refer Slide Time: 10:05)

Here are the K-maps for J 2 K 2 J 1 K 1 and J 0 K 0 which are derived from this table that we saw in the last slide. And let us take one of these as an example and see how the K map is constructed. Say we take J 2, now for state 1 we have Q 2 Q 1 equal to 0 0 Q 0 equal to zero; that means, we have this column and this row and J 2 is 0. So we write 0 over here. Next we have column equal to 0 0 and row equal to 1 and J 2 is 0, so we are talking about this column this row and again J 2 is 0. State 3 the column is 0 1 row is 0 and J 2 is 0, so column 0 1 row 0 again J 2 is 0 state 4 column 0 1 row 1 and J 2 is 1. So column 0 1 row 1 and J 2 is 1. And finally, for state 5 column is 1 0 row is 0, and J 2 is X. So column is 1 0 row is 0 and J 2 is X like that.

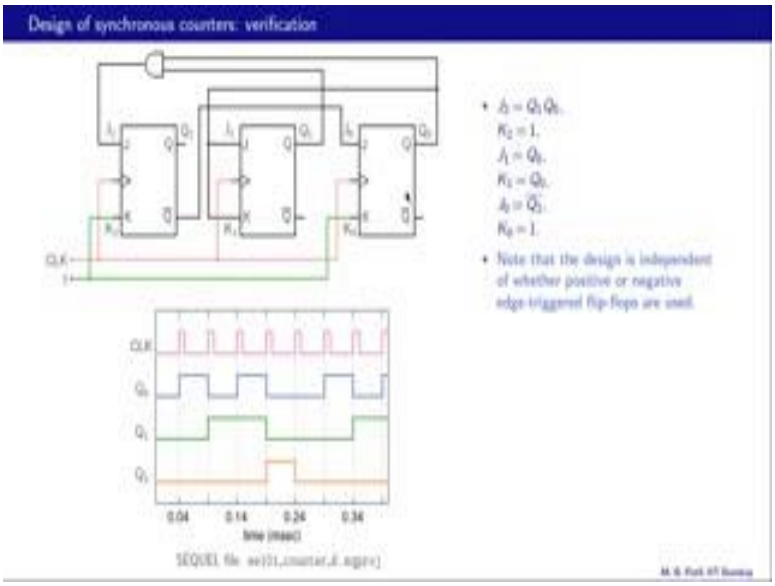
Now, these other combinations; these 3 do not occur in the state transition table, and therefore, J 2 each X over there. We do not care about J 2 is and similarly all other variables and so on. Now these 3 Xs have been marked in a different color, just to distinguish them from this other Xs which come from this table all right. Now once we have these K-maps we can go ahead and minimize these functions J 2 K 2 J 1 K 1 and J 0 K 0 and then come up with expressions for each of them.

And here are the minimized expressions for J 2 K 2 etcetera. J 2 turns out to be Q 1 Q 0 and you can verify K 2 is 1, in the maps for K 2 there is only 1 1 and all others are Xs. And we can assign 1 to each one of these Xs, so that this entire function is simply 1. J 1 is Q 0 this term here K 1 is also Q 0, that one J 0 is Q 2 bar this term, and K 0 is 1. So if

we implement these functions then we should get a counter which follows this state transition table.

And one more final point we will assume that a suitable initialization facility is provided to ensure that the counter starts up in one of the 5 allowed states for example, Q 2 Q 1 Q 0 equal to 0 0 0 and if that happens then the counter will simply keep following the counter sequence given in this table.

(Refer Slide Time: 13:32)



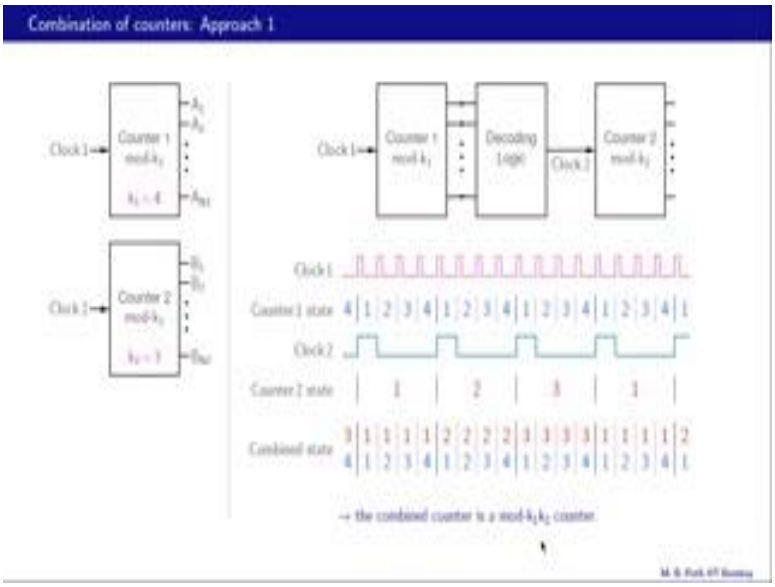
So here is our final implementation these are the flip-flops. We saw in the last slide and now in addition we have main connections for J 2 K 2 J 1 K 1 J 0 K 0 such that they satisfy these equations, which we have seen in the last slide also. Let us check whether the implementation is correct. J 2 is expected to be Q 1 Q 0, here is J 2 and there is an and gate here one input is Q 1 the other input is Q 0. So J 2 is indeed Q 1 Q 0 K 2 should be 1, here is our K 2, and that is tied to 1, J 1 should be Q 0 that is J 1, and that is connected to Q 0, K 1 is also Q 0, J 1 and K 1 are tied together. J 0 should be Q 2 bar J 0, should be Q 2 bar. So we have Q 2 bar here and K 0 should be 1. So K 0 is tied to 1 here.

Here are the simulation results and the circuit file is available to you so you can check it out. Even better you can go to your digital electronics lab and hope up this circuit and see if you get the same counter sequence all right. Now let us verify whether our counter operation is correct. We start with Q 2 Q 1 Q 0 equal to 0 0 0 and after the first active clock edge which is the rising edge here, since these are positive edge triggered flip-flops

we get 0 0 1 then we have 0 1 0 then we have 0 1 1 followed by 1 0 0 and then finally, back to 0 0 0. So we can go back to the previous slide, and make sure that this is indeed the sequence that we set out to achieve.

One more final remark, note that the design is independent of whether positive or negative edge triggered flip-flops are used. So the same connections are also valid if we replace these flip-flops with negative edge triggered flip-flops. The only difference that will happen in the results is that the transitions will now happen at the negative clock edge.

(Refer Slide Time: 16:23)



Let us now see how we can combine 2 different counters and what does it buy for us. So here is counter 1 with it is own clock called clock 1. And it is a mod K 1 counter and we will take this example where K 1 is 4 so this counter would have 4 different states. These are the outputs, and it is not really important what N1 is right now. Here is the second counter, counter 2. It has it is own clock called clock 2, and it is a mod K 2 counter. And we will take this example where K 2 is 3. So this second counter has 3 distinct states. And now let us see how we can combine these 2 counters.

So here is our counter 1. It is a mod 4 counter so it has 4 different states called 1 2 3 4 here. This is the clock for the counter which is called clock 1, in the first clock period the counter is in state 1, then it is a state 2 3 4 and then back to state 1, and then that repeats. What we do now is to use some decoding logic, to derive the clock for the second

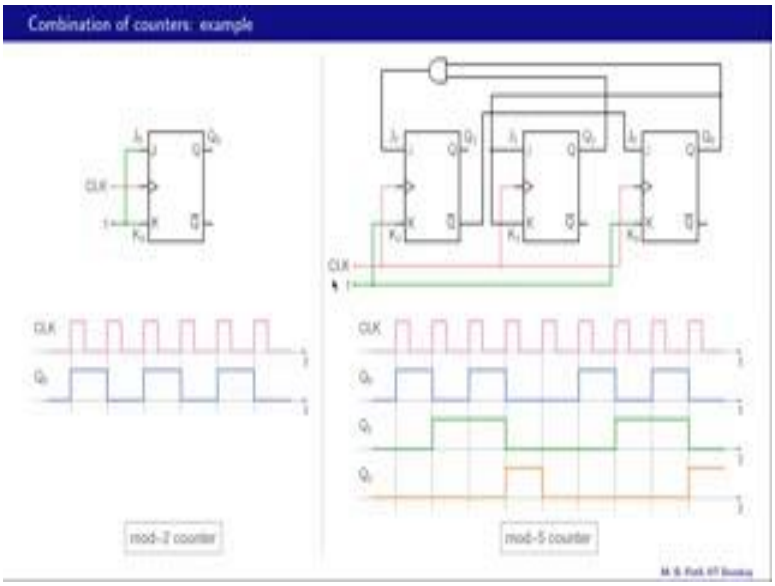
counter, which is called clock 2 here from the outputs of the first counter. And here is an example so this is what clock 2 may look like, it is 1 when the first counter is in state 1 otherwise it is 0, so it is 0 when the state of the first counter is 2 or 3 or 4. And it is 1 again when the first counter is state 1 and so on.

Now, this clock 2 serves as the clock for the second counter, which has 3 states, so with every clock pulse the state of the second counter changes. So here it is 1 then it is 2 then it is 3 and then back to 1. So we have 2 different states here state for counter 1 which is indicated by blue numbers here, and the state for counter 2 which is indicated with red numbers here.

Let us now look at the combined state of the entire circuit. It has got 2 components the state of counter 1, indicated by the blue numbers here and the state of counter 2 indicated by the red numbers. Where in this interval counter 1 is in state 1 counter 2 is and state 1, so we have this combination here. In this interval counter 1 is in state 2 counter 2 is in state 1 so we have this combination here and so on. And let us now try to figure out the modulus of the combined counter circuit.

What is the meaning of modulus? That means the number of clock pulses after which the combined state repeats. So let us start with 1 1, then 1 2, 1 3, 1 4, 2 1, 2 2, 2 3, 2 4, 3 1, 3 2, 3 3, 3 4 and now we are back to 1 1. So after 12 clock pulses the combined state is repeating. So therefore, this is a mod 12 counter. And this 12 of course, came about because K 1 is 4 and K 2 is 3 so 12 is simply K 1 times K 2. So the combined counter is a mod K 1 K 2 counter. So that is the conclusion from this figure.

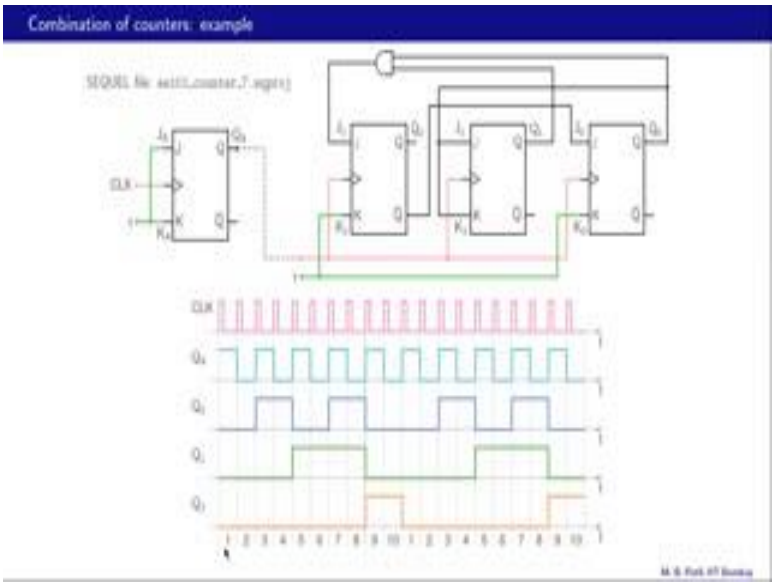
(Refer Slide Time: 20:37)



Let us look at an example of combining 2 counters using the approach that we saw in the last slide. Here is the mod 2 counter, here is a mod 5 counter, and using these 2 counters we are going to make up a mod 10 counter 2 times 5 all right. The first counter is simply a JK flip-flops with J and K tied to whether connected to 1, so therefore, this Q 0 is simply going to g1 toggling as shown over here.

This second counter is a mod 5 counter and in fact, we have seen this circuit earlier. And the associated waveforms are shown over here. It has this sequence 0 0 0 for Q 2 Q 1 Q 0 0 0 1 0 1 0 0 1 1 1 0 0 and then back to 0 0 0. So this is it is own clock. And now what we want to do is to derive the clock for the second counter, this 1 here from the output of the first counter and in this case we do not really require any decoding logic, because this Q 0 itself can serve as the clock for the second counter. So let us see what happens when we do that.

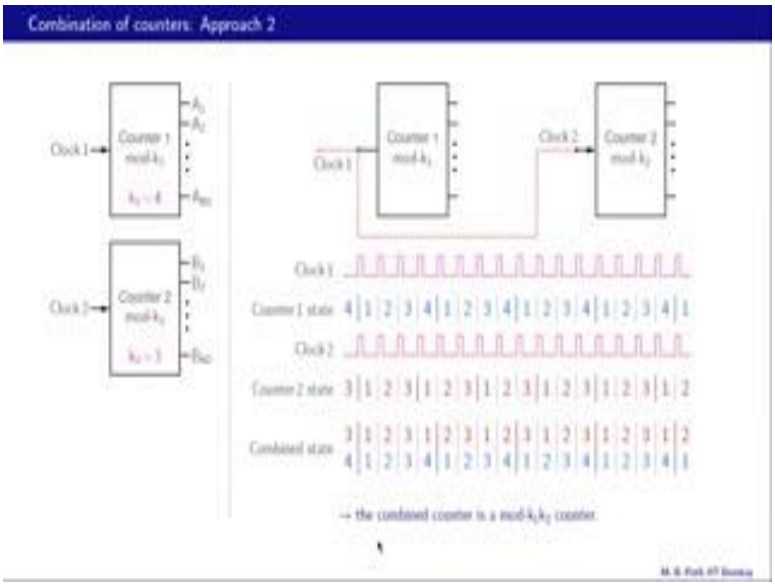
(Refer Slide Time: 22:00)



So, here is the combined counter. This is the mod 5 counter. And it is clock is now coming from the output of the first counter, which is a mod 2 counter and now let us verify that the modulus of the combined counter is indeed 2 times 5 that is 10. Here are the waveforms. This output the output of the first counter as we renamed as Q A now. And that is what it looks like with every clock pulse it toggles. And these are the outputs coming from the second counter Q 0 Q 1 and Q 2.

This is the first clock period; this is the second clock period third and so on. And we see that this state that is 0 0 0 1 appears again at this point 0 0 0 1, and therefore the modulus of this counter is 10, because after 10 clock periods we get the same state again.

(Refer Slide Time: 23:22)

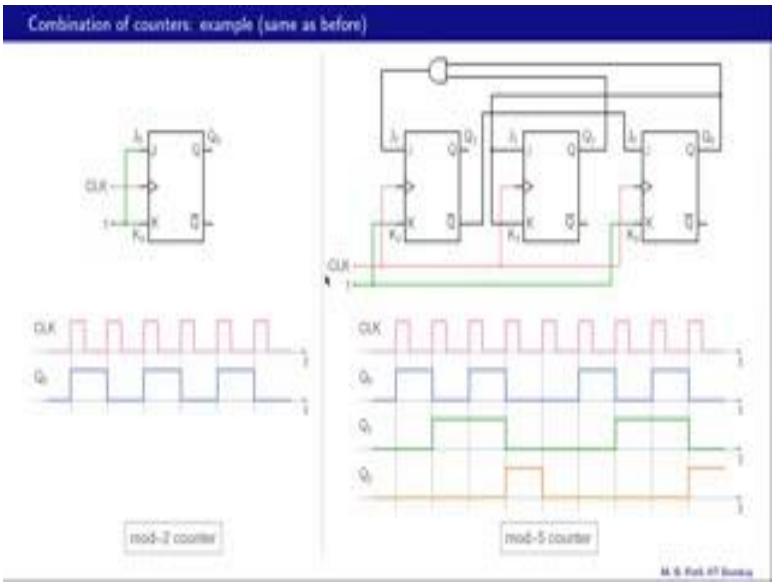


Let us now consider another approach to combine 2 counters, a mod K 1 counter and a mod K 2 counter, to obtain a mod K 1 K 2 counter. Here is the same example again over counter 1 is a mod 4 counter and counter 2 is a mod 3 counter. This is our counter 1 and that is clock 1, it has 4 different states marked with this blue numbers and after 4 clock periods state 1 appears again and so on. Here is our second counter, counter 2 and that gets the same clock edge clock 1; so clock 1 and clock 2 are the same signal now.

And let us see what happens so this clock 2 the same as clock 1. And these are the states of the second counter it is a mod 3 counter so we have 3 different states and after 3 clock periods this state 1 appears again and so on,. Here is the combined state in this interval over a counter 2 is in state 1 counter 1, is in state 1, in this interval or counter 2 is in state 2 counter 1 is in state 2, and so on. And now let us take a specific state say 1 1, and see when it appears again. So we start with 1 1, then 2 2, 3 3, 1 4, 2 1, 3 2, 1 3, 2 4, 3 1, 1 2, 2 3, 3 4, 1 1.

So now, 1 1 has appeared again and that has happened after 12 clock periods. So therefore, the combined counter is a mod K 1, K 2 counter. K 1 is 4; K 2 is 3 so therefore the combined counter in this case is a mod 12 counter.

(Refer Slide Time: 25:44)



Let us now look at an example and these counters our counter 1 and counter 2 are the same as before. This is the mod 2 counter, and this is about 5 counters. And now what we want to do is to apply the same clock to both of these counters, and see what happens.

So, here is the combination. The same clock now goes to counter 1 as well as counter 2, at here are the waveforms. This output is called Q A and the outputs of the second quarter are called Q 0 Q 1 Q 2. So this wave form is for Q A then we have Q 0 Q 1 Q 2. Now let us start with the state 0 0 0 0, and see when it appears again. And we see that it appears again, not here because we have 0 0 0 1 here, it appears again over here. We have 0 0 0 0 so; that means, this state has appeared after 10 clock periods and therefore, this is a mod 10 counter, as we would expect this is a mod 2 counter, this is a mod 5 counter and therefore the combined counter is a mod 10 counter.

In summary we have seen how to design a synchronous counter satisfying the specified state transition table. They have also looked at how 2 counters can be combined, and what is the modulo number of the resulting counter. That is all for now see you later.