Basic Electronics
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Lecture - 66
Counters

Welcome back to Basic Electronics. In this lecture we will look at a few specific counter circuits. We will start with the binary ripple counter and look at the count up and count down operations. We will then see how a binary ripple counter can be modified to count from 0 to 9 using the direct set and reset flip-flop inputs. Finally, we will look at the meaning of the term synchronous counter and illustrated with an example. Let us start.

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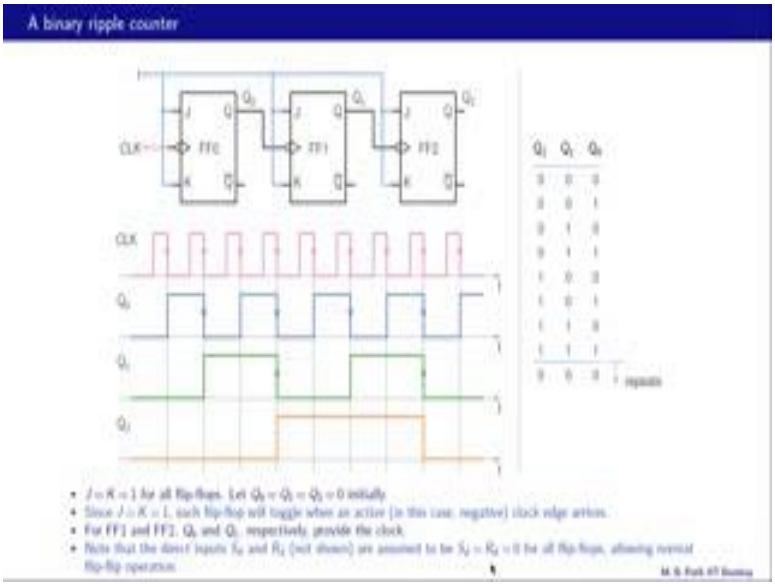

Let us now look at some specific counter circuits. And we will start with this circuit called the binary ripple counter.

So, here is the circuit we have JK flip-flops in this case. 3 of them the J and K inputs are tied together for each flip-flop. And those are connected to 1 so J is 1 here K is 1 here J is 1, here K is 1 here and so on. The clock this signal is connected to this first flip-flop which we have called as flip-flop 0. Whose output is Q 0? And the clock for the second flip-flop comes from the Q of the first flip-flop; that means Q 0 is connected as clock here similarly Q 1 is connected as the clock for the third flip-flop FF 2.

Let us now figure out how this circuit works .as we already said J is equal to K is equal to 1 for all flip-flops. And our starting point is Q 0 Q 1 Q 2 are all 0 initially. Now since J and K are both equal to 1, if we refer to the transition table for the JK flip-flop we find that after each active clock edge the output is going to toggle. So therefore, each flip-flop will toggle when an active clock edge arrives. In this case the active clock edge is a negative clock edge. And that is why we have marked these negative edges here. And we are now in a position to draw these waveforms. Since Q 0 is 0 in the beginning is going to toggle at this point because there is an active is there and the clock is actually serving as the clock for the first flip-flop.

So, here it will toggle to 1 once again when an active clock edge comes it is going to toggle, go back to 0 then go back to 1 and so on. So that is going to repeat for Q 0 like that. Whatever Q 1 for Q 1 this Q 0 acts as the clock so now, we are looking for a negative edge in the Q 0 waveform. And those edges are marked here. So therefore, Q 1 is 0 to begin with is going to toggle at this time going to toggle again over there and so on so that is what Q 1 looks like.

What about Q 2 Q 1 serves as the clock for this flip-flop, and therefore, an active edge for FF 2 is this edge or this edge. So Q 2 which is 0 in the beginning is going to toggle here and is equal to toggle here again like that. Here is the state transition diagram for this counter these are the counter outputs Q 2 Q 1 Q 0. To begin with we have 0 0 0 then we have 0 0 1 then we have 0 1 0 and so on. And after 8 states we come back to 0 0 0 and note that this is decimal 0 this is decimal 1 decimal 2 3 4 5 6 7 and then back to 0. So the counter repeats after this point so it is a modulo 8 counter.

One final remark before we leave this slide, now that the direct inputs S d and R d which are not shown with this picture are assumed to be S d equal to R d equal to 0 for all flip-flops, and that allows normal flip-flop operation. So that is implicit in this entire description.

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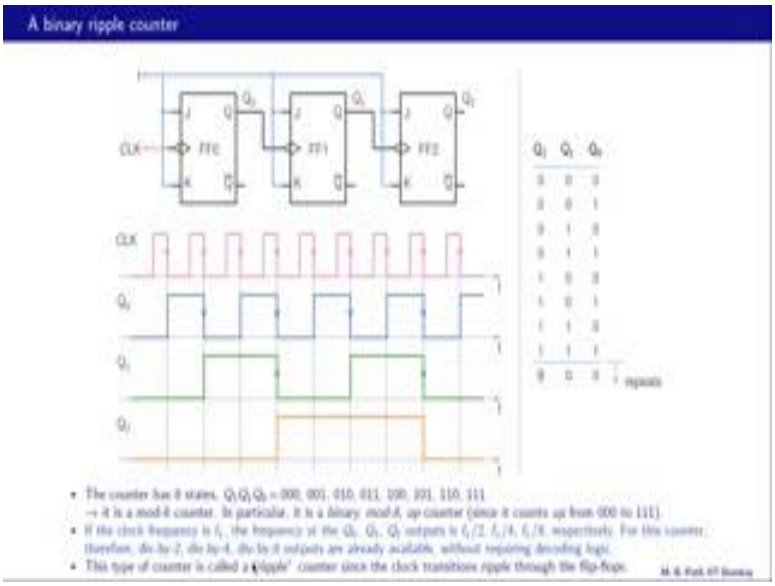

Let us make a few more remarks the counter has 8 states namely Q 2 Q 1 Q 0 equal to 0 0 0 0 0 1 0 1 0 etcetera. Therefore, it is a mod 8 counter. In particular, it is a binary mod 8 up counter. Since it counts up from 0 0 0 to 1 1 1. If the clock frequency is f c, then the frequency at the Q 0 Q 1 Q 2 outputs is f c by 2 f c by 4 and f c by 8 respectively. And that can be clearly seen from this figure here. The frequency of Q 0 is half of the clock frequency. Frequency of Q 1 is half of the Q 0 frequency. And the frequency of Q 2 is half of the Q 1 frequency. So therefore, we have f c by 2 f c by 4 and f c by 8 for these 3 outputs respectively.

So, for this counter divided by 2 divided by 4 and divide by 8 outputs are already available without requiring any decoding logic. This type of counter is called a ripple counter. Since the clock transitions ripple through the flip-flops, and that is easy to see the clock inputs for these 3 flip-flops are not the same. This one gets the actual clock. The clock for this flip-flop comes from the output of the previous flip-flop. And the clock for this flip-flop comes again from the output of the previous flip-flop. So in that sense the clock ripples through these flip-flops. And that is why it is called a ripple counter. So it is a binary ripple up counter.

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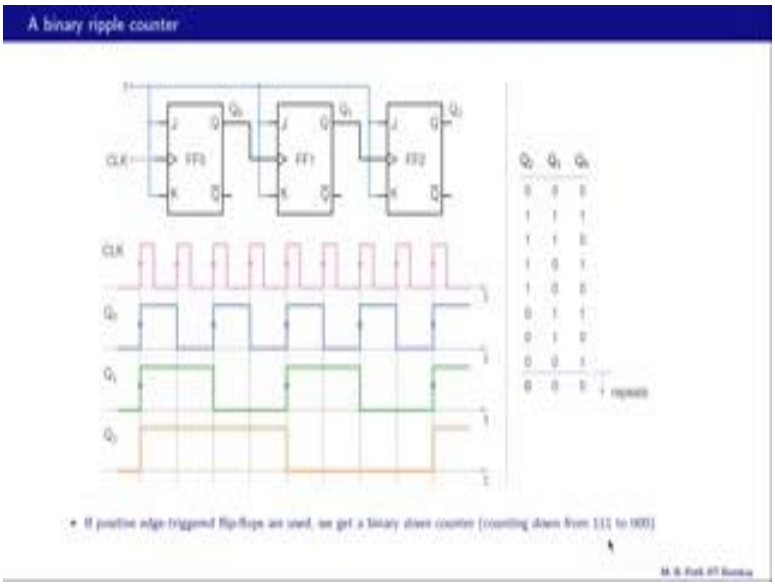

Let us now look at a variation of the previous circuit that we saw. Once again we have 3 flip-flops: FF 0, FF 1 and FF 2. The J and K inputs are tied together and connected to 1. The clock which is shown here is applied to the first flip-flop. The output of the first flip-flop is connected as the clock of the second one, and the output of the second flip-flop is connected as the clock of the third one.

Then only difference between this circuit and the previous circuit is that these flip-flops are positive edge triggered. And as we will see that makes a big difference in the functionality of this counter all right. Now let us start with Q 0. Now for this first flip-flop the clock signal serves as the clock. And that is shown here and the active edge is the positive edge you know and all these activities are marked here. And since J and K are equal to 1: Q 0 is going to toggle after every active edge. And starting with 0 it toggles here toggles and so on.

What about Q 1? For Q 1 Q 0 shows as the clock and therefore, we are now looking for an active edge that is a positive edge in Q 0. So these edges serve as the active edges for the second flip-flop. And since J and K are 1 for this flip-flop as well Q 1 will toggle after every active edge. So it toggles at all of these time points and that we what will get. Now Q 1 serves as the clock for the third flip-flop, and therefore, we are now looking for positive edges in Q 1, and those are marked here all right. And once again for FF 2, J and

K are equal to 1 and therefore, Q 2 is going to toggle after every active edge. So it is going to toggle here, and here so that is the waveform we get for Q 2.

Let us now construct the state transition table for this counter. We begin with Q 2, Q 1, Q 0 equal to 0 0 0. The next state is 1 1 1 followed by 1 1 0 then 1 0 1 and so on. So this is the table 0 0 0 1 1 1 1 1 0 1 0 1 1 0 0 etcetera and then finally, once again we have 0 0 0 and the counter repeats.

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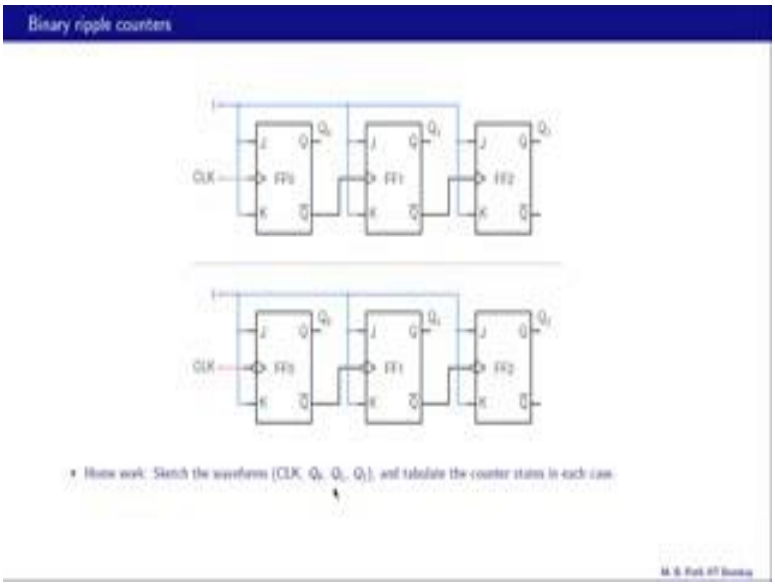

Now, this is decimal 0. This is decimal 7 this is decimal 6 5 4 3 2 1, and back to 0. So in other words we have now got a binary down counter, counting down from 1 1 1 to 0 0 0. There is some homework. Sketch the waveforms that is clock Q 0 Q 1 Q 2 with time and tabulate the counter states in each case. What is the difference between these counters and the once we have seen earlier? In these counters also we have J and K connected together and connected to 1. The clock goes to the first flip-flop so all these are the same as what we have seen earlier the difference is here Q bar of the first flip-flop serves as the clock for the second one and similarly Q bar of the second flip-flop serves as the clock for the third one and the same thing happens here as well.

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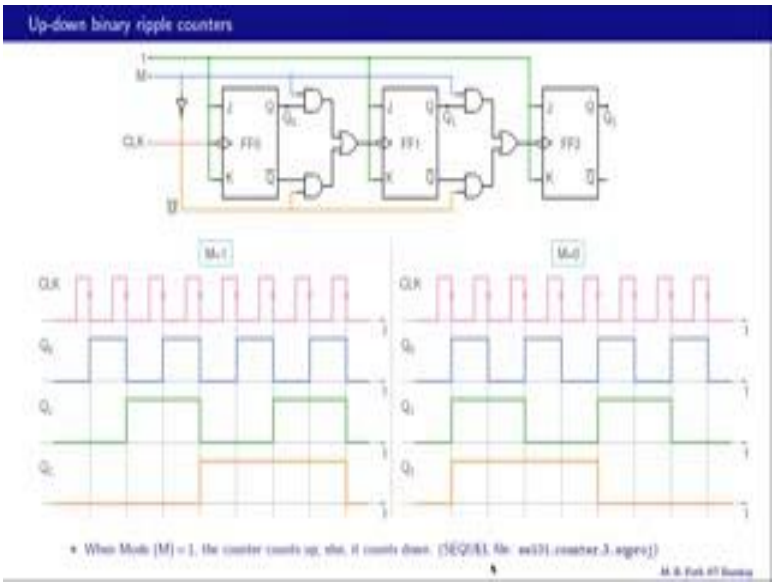

So, workout these waveforms and then you will figure out whether the counter is an up counter or a down counter. We have seen a binary up counter; we have also seen a binary down counter. It turns out that we can combine up counting and down counting into a single counter. And that is what is shown over here. Let us see how the circuit works. First let us note that there are many features which are common with the circuits we have seen earlier. For example, this J and K are connected together for each flip-flop and they are all connected to 1.

The clock goes to the first flip-flop and in this circuit, we have an additional input called M or mode. And here is mode bar. Let us consider the case that M is 1 first in that case M bar is 0, and the output of this and gate is then 0. And therefore, this clock for FF 1 is the same as Q 0, in that case. And similarly we will find that this clock for FF 2 is the same as Q 1. And with these conditions we get the counter circuit that we are already seen earlier, and that is the operation of the counter that is up counting.

Let us now consider the case that M is 0. If M is 0 M bar is 1 of course, the output of this and gate is simply Q bar of FF 0. Now since M is 0 the output of this and gate is 0. And therefore, the clock for FF 1, is the same as Q bar of FF 0. And similarly the clock for FF 2 is the same as Q bar of FF 1. And with these connections you should verify that we get these waveforms here and that is down counting.

So, in summary when mode is 1 the counter counts up else it counts down, and the circuit file is available you can try out this simulation.

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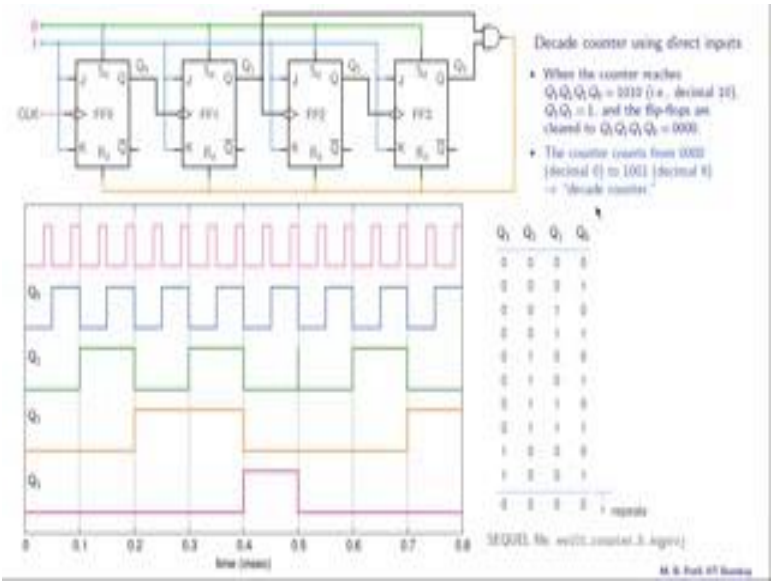

So, far we have considered counters in which the direct set and direct reset inputs were inactive; that means, S d and R d in this figure were equal to 0 and therefore, all the flip-flops operated normally without any interference from the direct inputs. It is possible to use these direct set and reset inputs to our advantage to make up counters with the desired sequence, and here is an example. This circuit is a decade counter; that means, it will count from decimal 0 decimal 1 decimal 2 all the way up to decimal 9 and then back to 0. So that is the operation that this counter performs and let us see how it works.

Let us imagine that the S d and R d inputs are inactive, and see what circuit we have got in that case. So J and K are tied together for each flip-flop and connected to 1. The clock goes to the first flip-flop whose output is connected to the clock of the second flip-flop and so on. Like that. And this is a circuit we have already seen earlier and it is a binary up counter. So it is going to count from Q 3 Q 2 Q 1 Q 0 equal to 0 0 0 0 then 0 0 0 1 then 0 0 1 0 etcetera, all the way up to 1 1 1 1.

Now, the idea is not to allow the counter to go all the way up to 1 1 1 1, but when it reaches 1 0 0 1, then make sure that the next state is not 1 0 1 0 1, but 0 0 0 0 1. If you can do that then we have the desired functionality; that means the counter will count

from decimal 0 decimal 1 all the way up to decimal 9 and then back to 0. And that is what we want to achieve with the S d and R d inputs.

So, let us now look at the connections. S d is 0 for all of these flip-flops. And R d is coming from the output of this gate and what are the inputs to this gate, one input is Q 3 the other input is Q 1. So this Q 3 Q 1 is connected as R d for all of these flip-flops. Now let us look at the S d and R d values for the flip-flops for each of these states. Now S d is always 0 and R d comes from this gate, which is Q 3 Q 1 all right. Now consider the first state 0 0 0 0, Q 3 is 0 Q 1 is 0 so therefore, this output is 0, so we have S d equal to 0 R d equal to 0 for each flip-flop the counter will function normally and goes to the next state.

Once again we have Q 3 Q 1 equal to 0 and the counter goes to the next state. Again Q 3 and it with Q 1 is 0, and we go to the next state and so on. So this continues and what is the condition for the output of this gate to become 1, that is Q 3 equal to 1 and Q 1 equal to 1 and that does not happen anywhere here. And after the state 1 0 0 1 the counter would try to go to 1 0 1 0, and that is when this output becomes 1. In that happens S d is 0 R d is 1 for all flip-flops and they get reset; that means, all of these Qs, Q 3 Q 2 Q 1 Q 0 will become 0 as shown over here. And after this state the counter simply repeats what you did earlier; that means, from 0 0 0 0 it will go to 0 0 0 1 then to 0 0 1 0 and so on. So we have got the desired functionality and now let us look at the waveforms.

So, we start with Q 3 Q 2 Q 1 Q 0 equal to 0 0 0 0 the next state is 0 0 0 1; then 0 0 1 0 and so on as in this table. And finally, we come to 1 0 0 1 that corresponds to this entry in the table this one. After this the counter would try to go to 1 0 1 0 1, but as soon as that happens the output of this and gate becomes 1 and all flip-flops are cleared. And if you notice there is the short spike here in Q 1 and that happens because Q 1 is trying to go to 1 and as soon as that happens all the flip-flops get reset to 0 and we are back to 0 0 0 0 all right. So that is how this counter operates, the circuit file is given here, so you can run the simulation and take a look at the results as well.

So, here is the summary when the counter reaches Q 3 Q 2 Q 1 Q 0 equal to 1 0 1 0 that is decimal 10, Q 3 Q 1 becomes equal to 1 and the flip-flops are cleared to 0 0 0 0 so; that means, this state is never reached. And therefore, the counter counts from 0 0 0 0 decimal 0 to 1 0 0 1 decimal 9 and that is why it is called a decade counter.

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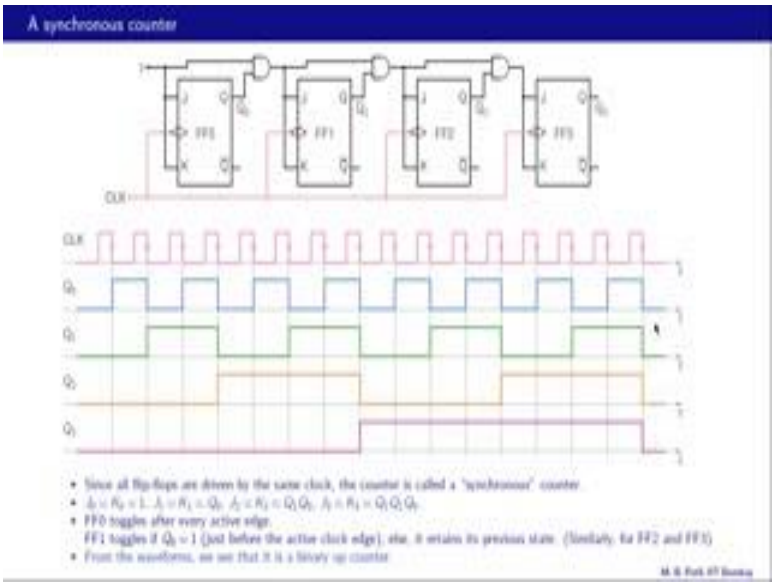

Let us now look at a synchronous counter. What is the meaning of this term; that means, the same clock is going to all the flip-flops in the counter. Since all flip-flops are driven by the same clock the counter is called a synchronous counter.

Now, let us figure out the connections. First of all, they have the same clock the J and K inputs are tied together for each of these flip-flops, for the first flip-flop J and K are connected to 1. For the second flip-flop J and K are connected to Q 0, and it with 1, that is simply Q 0. For the third flip-flop J and K are connected to and of Q 1 and Q 0, so that is Q 1 Q 0. And for the last flip-flop J and K are connected to Q 2 anded with Q 1 Q 0 so; that means, Q 2 Q 1 Q 0.

So, let us summarize we have J 0 equal to K 0 equal to 1 J 1 equal to K 1 equal to Q 0 J 2 equal to K 2 equal to Q 1 Q 0 J 3 equal to K 3 equal to Q 2 Q 1 Q 0. Let us now figure out how this counter works. Since the same clock is applied to all flip-flops they all respond to the same active edge and the active edges are marked over here. The negative edges of the clock since these are negative edge triggered flip-flops. And let us now start with the first flip-flop that is FF 0. Now for this one we have J equal to K equal to 1 and therefore, it is going to toggle every time there is an active edge. So if we start with Q 0 equal to 0 is going to toggle here go to 1 toggle again and so on. So that is what we have for Q 0.

Next let us look at Q 1. Now for Q 1 J is equal to K and that is equal to Q 0. So we need to look at Q 0, just before the active edge. Before the first active edge Q 0 is 0 1; that means, we have J equal to K equal to 0 and so therefore, if Q 1 was 0 here is going to continue to be 0 all the way up to here. Now when this active edge arrives we look at Q 0 just before that active edge and we find that it is 1. So therefore, Q 1 is going to toggle at this point. In the next active edge arrives we look at Q 0 just before that we find that it is 0 so therefore, no change in Q 1 at this point and so on. So in this way we can figure out what is going to happen to Q 1 and this is the result.

Let us look at Q 2 now. For Q 2 we need to look at J 2 equal to K 2 equal to Q 1 Q 0. So we need to look at this function just prior to the active edge. If that function is 0 then there would be no change in Q 2. If it is 1 then Q 2 is going to toggle all right. So let us say Q 2 is 0 in the beginning. At this point just before the first edge Q 1 Q 0 is 0. So no change at this point again Q 1 Q 0 is 0 so no change. At this point Q 1 Q 0 continues to be 0 no change. At this point Q 1 is 1 Q 0 is also one so therefore, Q 1 Q 0 is now equal to 1 and therefore, Q 2 is going to toggle over here.

So, this way we can continue and figure out what is going to happen to Q 2. And this is the result. We can follow the same procedure for Q 3, and now we need to look at J 3 equal to K 3 equal to Q 2 Q 1 Q 0 when this function is 1 then Q 3 is going to toggle otherwise Q 3 is going to continue with it is previous value.

Now, let us look at when this becomes 1 and when we see these waveforms we figure that are going to be 1 here because Q 2 is 1 Q 1 is 1 and Q 0 is 1 here and also it is going to be 1 over here. So Q 3 is going to toggle at this point and also at this point and otherwise it is not going to change. So if we start with Q 3 equal to 0, it is going to stay 0 here toggle to 1 and then back to 0 like that.

So, what kind of counter have we got, from the waveforms we see that it is a binary up counter. So we have 0 0 0 0 0 0 0 1 then 0 0 1 0 and so on all the way up to 1 1 1 1 and then back to 0 0 0 0 so it is a binary up counter counting from decimal 0 to a decimal 15. And we have seen this kind of binary up counter earlier the difference is that we have a synchronous counter here; that means, the same clock is going to all the flip-flops.

To summarize, we have looked at a few counters in this class. We have seen an example of a synchronous counter. In the next class we will see how to design a synchronous counter for a specific state transition table. See you next time.