Basic Electronics
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Lecture – 64
D flip-flop

Welcome back to Basic Electronics. In the last lecture we looked at the transition table for a JK flip-flop and worked out the output waveforms with some given input waveforms for a single JK flip-flop. We will now take simple circuits consisting of more than one JK flip-flop and see how the various waveforms can be obtained by following a systematic procedure. We will then consider another commonly used flip-flop, the D flip-flop and see how we can make a shift register with D flip-flops. Let us get started.

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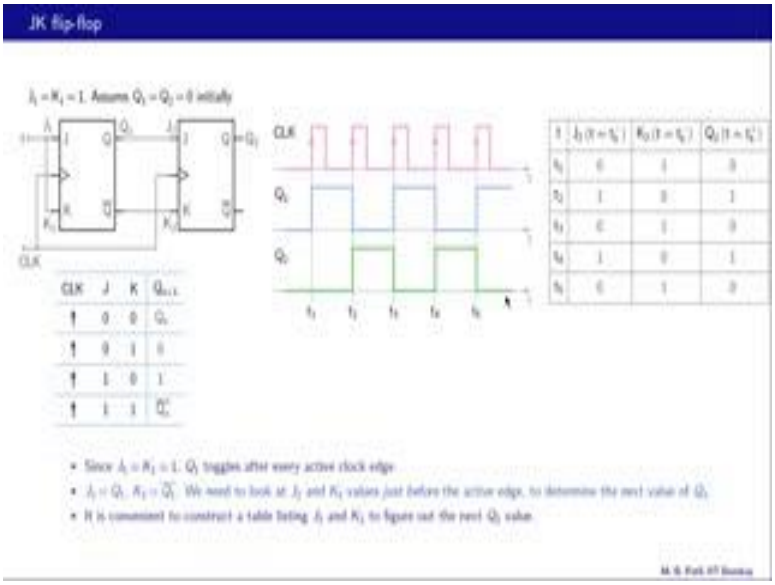

Another example here are 2 flip-flops they are edge triggered flip-flops because we have this triangle here. And their positive edge triggered flip-flops because we do not have a circle, just before the triangle all right. Here is our problem J 1 and K 1 are equal to 1 so these 2 inputs are tied together to 1 and we assume that Q 1 and Q 2 are both 0 initially and then this clock is applied. And we want to figure out what Q 1 and Q 2 would look like with time. This is our transition table. Now in this case since J 1 and K 1 are both 1 we are looking at this row of the table. Q n plus 1 is Q n bar; that means, Q 1 is going to toggle after every active clock edge is going to change after this and so on.

So, that is what it looks like it was 0 to begin with given here changes again and so on. Getting Q 1 was straightforward because the inputs to this flip-flop J 1 and K 1 we were not changing with time, they were always constant equal to 1. And therefore, we could figure out in advance what is going to happen to Q 1, which the second flip-flop the situation is different. J 2 is the same as Q 1 K 2 is the same as Q 1 bar. And since Q 1 changes with time like that these inputs also change with time and therefore, it makes it a little more complex. And we now need to look at J 2 and K 2 values just before the active edge; that means these edges to determine the next value of Q 2. So let us do that.

And we will find it very convenient to have a table listing J 2 and K 2 at the various transition points to figure out the next Q 2 value. So let us prepare such a table there and let us understand what this says. Here is a t, t 1, t 2, t 3, t 4, t 5. T 1 refers to this active edge here. T 2 refers to this active edge and so on. These are J 2 and K 2 values, at t k minus for example, in this row this value refers to J 2 at t equal to t 1 minus.

What is t 1 minus this is t 1, t 1 minus is the time just before that edge. And for that we have J 2 which is the same as Q 1 equal to 0 and K 2 which is the same as Q 1 bar equal to 1. So J 2 is 0 and K 2 is 1, J 2 is 0 K 2 is 1 Q 2 is going to be 0. And since it is already 0 to begin with they are not going to see any change like that all right. Now the next change can happen at the next active edge which is t 2. And we need to look at J 2 at t 2 minus and K 2 at t 2 minus. This is our t 2, t 2 minus is just prior to that and at that time Q 1 is 1 therefore, J 2 is 1. K 2 is Q 1 bar so therefore, that is 0. And we are now looking at J equal to 1 K equal to 0; so Q n plus 1 equal to 1. So the next Q 2 is going to be 1, and that is what we see over here.

And you can figure out the rest of these transitions in a similar manner. The important thing to note is we always look at J and K values just before the active edge.

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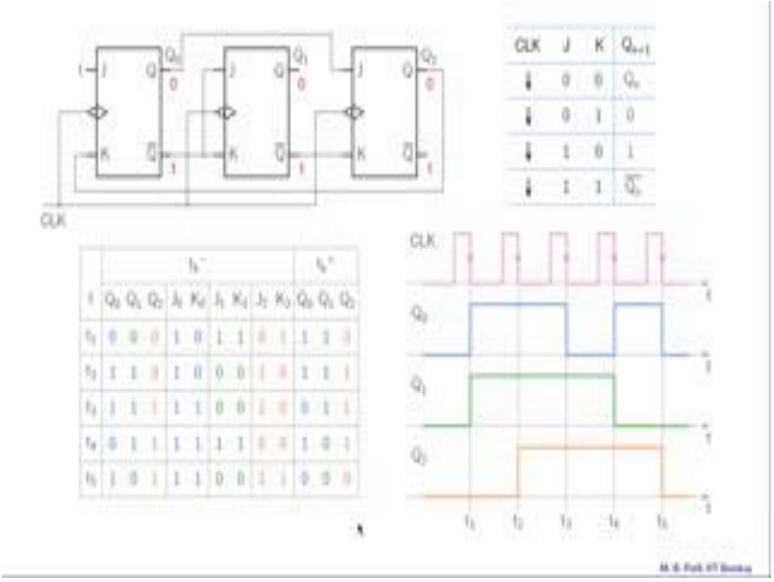

Here is a more complicated circuit. We have 3 flip-flops now. 1 2 3 and all of them are edge triggered, and their negative edge, triggered because we have this circle, where the output of this flip-flop is called Q 0. So this would be J 0 and K 0. This would be Q 0 bar. Similarly, we have J 1 K 1 Q 1 Q 1 bar, J 2, K 2, Q 2, Q 2 bar. Here J 0 is connected to 1 so it is always equal to 1 does not change with time. K 0 is the same as Q 2, J 1 and K 1 are tied together and they are equal to Q 0 bar. J 2 is the same as Q 0 and K 2 is equal to Q 1 bar. So these are our connections this is the clock input and we are also given that Q 0 Q 1 Q 2 are all 0 to begin with and let us see now what happens.

Since the same clock is going to all 3 flip-flops like that. We know that all transitions in Q 0 or Q 1 or Q 2 are going to happen, only after these active clock edges which I marked here with arrows. And now let us proceed with the first transition that is after this first active edge. Let us try to figure out what Q 0, Q 1, Q 2 are going to be after t 1. And we will find this table very convenient. Let us first understand what it is doing. We have t 1, t 2, t 3, t 4, t 5 here those are the active edges t 1, t 2, t 3 and so on. This part of the table corresponds to t k minus; that means, just prior to t 1 or just prior to t 2 and so on. This part of the table corresponds to t k plus; that means, just after t 1 or just after t 2 and so on.

Let us start with t equal to t 1. And at t 1 minus we have Q 0 equal to 0 Q 1 equal to 0 and Q 2 equal to 0. And knowing that and knowing all these connections so J 0 K 0 J 1 K

1 etcetera we can figure out what each one of these is going to be at t 1 minus. J 0 is always 1, K 0 is the same as Q 2 and Q 2 is 0 at t 1 minus so therefore, K 0 is 0. J 1 and K 1 are tied together and they are equal to Q 0 bar, since Q 0 is 0 Q 0 bar is 1. So that is why we have J 1 equal to K 1 equal to 1. J 2 is the same as Q 0 and that is 0 at t 1 minus K 2 is the same as Q 1 bar, at t 1 minus and since Q 1 is 0 Q 1 bar is 1 so therefore, K 2 is 1.

What we can do now is to credit Q 0, Q 1, Q 2 at t 1 plus. So we can fill up this column here knowing this J and K values. For example, J 0, K 0, are 1 0. That brings us here and that says that Q 0 is going to be 1 like that. What about Q 1? J 1, K 1 are 1; that means, Q is going to toggle. So over Q 1 which was 0 earlier, will now become 1. What about Q 2 J 2 is 0 K 2 is 1 that brings us here. So the next Q 2 is going to be 0 like that. So what we are now is Q 0 Q 1 and Q 2 at t 1 plus; that means, just after t 1. And we know already that nothing is going to happen to Q 0 Q 1 or Q 2 until the next active edge comes; that means, between these 2 active edges no further change is going to happen and therefore, we can go ahead and plot these 3 values like that. So Q 0 is 1, Q 1 is 1, and Q 2 is 0.

Now, that brings us to t equal to t 2. At t 2 we have these same values here 1 1 0 we are talking about t 2 minus r, note that minus there. And once again we can figure out what J 0, K 0 are at t k minus and so on. And then go ahead and predicted Q 0, Q 1, Q 2, at t 2 plus etcetera. So we keep following this procedure and then we have the complete waveforms. So here are the waveforms all the way up to t 5. And the corresponding J K values are also given in this table. And you should really go through each of these entries, the ones that we did not look at already figured out why this J 0, K 0 it is 1 0 here.

Why this J 1, K 1 is 0, 0 here and so on. And why these give rise to this prediction, of the next Q values. And that will surely reinforce your understanding of the JK flip-flop transition table.

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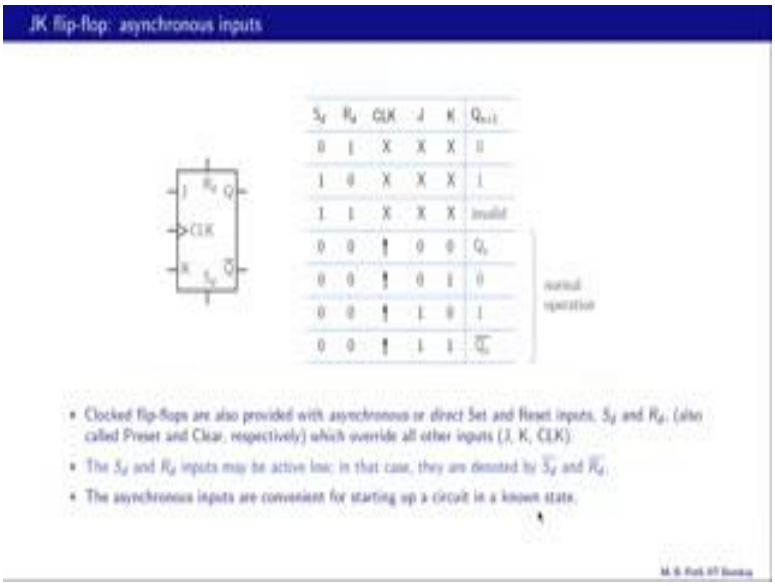

Let us now discuss something called the asynchronous inputs and the meaning of this term asynchronous, is something which is not related to in the clock. And we will see why these are called asynchronous inputs. Let us make a few points first. Clock flip-flops are also provided with asynchronous or direct set and reset inputs; S d and R d. S d and R d which override all other inputs. That is JK and clock. And these inputs are called preset and clear respectively. So S d is called preset. R d is called clear. And we will see why the terminology has come about all right. The S d and R d inputs may be active low; in that case they are denoted by S d bar and R d bar.

The asynchronous inputs are convenient for starting up a circuit in a known state. So that is why they are provided. Also as we will find out later these inputs can be used for making up counter circuits, some of the counter circuits all right. Let us look at how these is S d and R d inputs work. When S d and R d are both 0 these 4 entries here, that corresponds to the normal operation of the flip-flop. We have this active edge since it is a positive edge triggered flip-flop we have this rising edge here of the clock, and these 4 entries we have already seen earlier so that is the normal operation of the flip-flop. When S d is 0, and R d is 1 then Q becomes 0.

Irrespective of these 3 input values and that is why we have shown these as do not care conditions that is x. And now it is clear why these inputs S d and R d are called asynchronous, because the operation is not related to the clock. These inputs simply

override the clock. When S d is 1 and R d is 0, then Q becomes equal to 1. Again it irrespective of these are the 3 inputs and S d equal to R d equal to 1 is not allowed. Now imagine that we have a bunch of JK flip-flops of this type in our circuit and we want to make them all equal to 0 in the beginning.

Now, that can be done by simply making R d equal to 1 and S d equal to 0, for all of them that will force all the Q outputs or the flip-flops to be 0. And similarly we can force Q equal to 1 by making S d equal to 1 and R d equal to 0. So that is why we said the asynchronous inputs are convenient for starting up a circuit in a known state.

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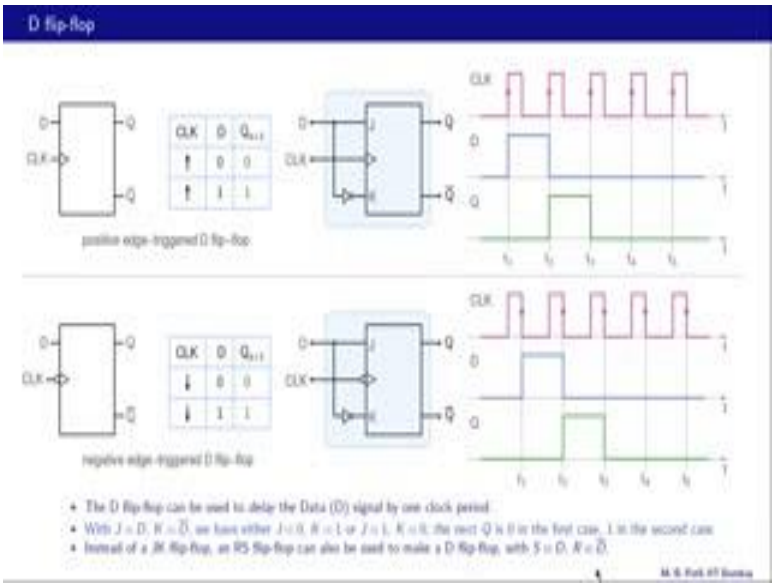

Another useful flip-flop is the D flip-flop, and it can be a positive edge triggered flip-flop or a negative edge triggered flip-flop. It has 2 inputs D and a clock, and the convention for the clock is similar to what we already seen. This triangle indicates that it is an edge triggered flip-flop and these circles here indicate that is a negative edge triggered flip-flop. We can think of a D flip-flop as a JK flip-flop with K equal to J bar, and that input is taken as D. This is a possible implementation of the D flip-flop. And if this is a positive edge triggered flip-flop then so is this. If this is a negative edge triggered flip-flop, then so is this one. And keeping this equivalence in mind between the D flip-flop and the JK flip-flop it is easy to figure out the transition table for the D flip-flop.

Let us consider D equal to 0 first. What does that mean? It means J is 0 and K is 1 and; that means, after the active clock edge Q is going to become equal to 0. And that is what

it says over here. Similarly, if D is 1 then J is 1 and K is 0 and then after the active edge Q is going to become equal to 1 and that is what it says over here. So if d is 0 Q n plus 1 is 0 if D is 1 Q n plus 1 is 1. And the same table is also valid for this negative edge triggered D flip-flop except of course, for the active edge which is a negative transition now.

Let us look at these waveforms now to understand the operation of our D flip-flop. This is our clock waveform and the active edge is marked with an arrow, in this case it is a positive edge this is our D input. And let us see what happens as a result of this input. At t 1 what do we do, we look at the D value just before this active edge and we find that it is 0. And therefore, the Q output just after t 1 is going to be 0. And then of course, it does not change until the next active edge arrives. So therefore, Q is 0 throughout this interval. What happens at this point? At t 2 we look at the input D just before t 2 that s t 2 minus and we find that D is 1 and therefore, just after t 2 over Q is going to become equal to 1 and then it is not going to change again until t 3 and so on.

Let us look at these waveforms now for the negative edge triggered D flip-flop. Here is our clock the active edge is now the negative clock edge. This is our D input and at t 1 we are going to look at D just before the edge and we find that D is 0. So therefore, our Q is going to be 0 after t 1 and then it is going to stay equal to 0 throughout this interval. At t 2 or other t 2 minus we find that D is 1 and therefore, over Q is going to become equal to 1 after t 2. And then it is going to stay t equal to 1 up to t 3 and so on.

Let us summarize, the D flip-flop can be used to delay the data signal by one clock period. So this D is called the data input, and that is why it is denoted by D. And what is the delay that we are talking about, let us compare this waveform and this waveform, and we see that this output is a delayed version of the input and the delay is 1 clock period. And the same thing happens here as well. With J equal to D and K equal to D bar we have either J equal to 0 K equal to 1 or J equal to 1 K equal to 0 and therefore, the next Q is 0 in the first case and 1 in the second case. This we have already discussed. Instead of a JK flip-flop and RS flip-flop can also be used to make up a D flip-flop, with S equal to D and R equal to D bar.

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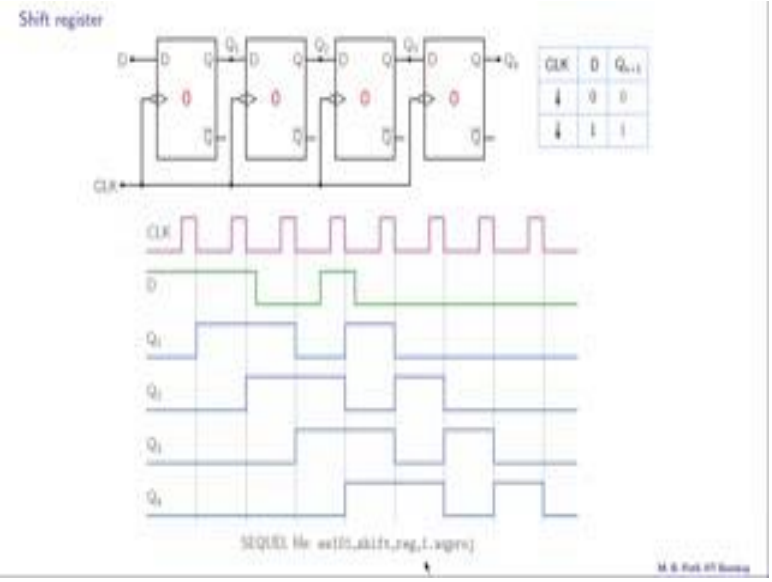

Let us now look at a shift register which can be made up with D flip-flops. In this example we have 4 of them. The output of the first flip-flop is called Q 1 the second Q 2 then Q 3 and then Q 4. The clock is common to all of them and that is shown over here. This D input is applied to the first flip-flop, so this D is shown over here and that is connected to this D 1. The output of the first flip-flop Q 1 is connected as D 2 similarly Q 2 is connected as D 3 and Q 3 is connected as D 4 and now let us see what happens as a result of these inputs.

To begin with we have Q 1 equal to 0 Q 2 equal to 0 and so on. And that is also indicated over here so all Q values are 0. And now the first active edges come along this one, and let us see what happens. Remember we have to look at the d input of each flip-flop just before the active edge. Now for this flip-flop the d input is this d here that waveform and just before this active edge, it is value is 1 so therefore, Q 1 is going to change to 1 and then it is not going to change up to the next active edge. What about Q 2 for this flip-flop Q 1 is the D input and therefore, we should now look at the value of Q 1 just before the active edge and we find that it is 0, therefore, Q 2 is going to remain 0 and again it is not going to change until the next active edge, and the same thing will happen to Q 3 and Q 4 as well.

So, this is what we have after the first active edge Q 1 has become 1 Q 2 Q 3 Q 4 are remained equal to 0. And that is also indicated here 1 0 0 0 all right. Now after the

second active edge, what is Q 1 going to do we need to look at D just before that active edge. D is 1 so Q 1 will be equal to 1 after t 2, or after this active edge here. What about Q 2? We now look at Q 1 because that serves as the D input for the flip-flop here, and Q 1 is 1 just before the active edge and therefore, this Q 2 is going to change to 1, then of course, it is not going to change until the next active edge.

What about Q 3? For Q 3 Q 2 serves as the D input which was 0, just before the active edge, so therefore, Q 3 will stay equal to 0. And similarly Q 4 will stay equal to 0, like that. So now, we have 1 1 0 0. And we can proceed in this same manner and see what happens. And we are not going to go through each step now, but just look at the results. So this is after the next active edge and so on. And we observe that each output is a delayed version of the previous output.

For example, Q 3 is like this, and Q 4 looks exactly like Q 3 except it has got delayed by one clock period. That is 1 observation that we make. And also this D flip-flop has synchronized the transitions with the active edges. For example, over D input was not synchronized with the clock these changes were not at the same time as the clock edges, but because of this D flip-flop the first D flip-flop output Q 1 has got now synchronized with the clock edges. So that is how a shift register works. And you can try out this simulation the circuit file is available.

To conclude, we have seen how the circuits made up of JK flip-flops can be treated in a systematic manner and the output waveforms can be obtained. We have looked at another flip-flop a D flip-flop which may be considered a special case of the JK flip-flop with J equal to K equal to 1. We have seen how D flip-flops can be connected to make up a shift register. In the next class we will look at how a shift resistor and an adder can be used to make a binary multiplier. That is all for now, see you next time.