Basic Electronics
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Lecture – 63
JK flip-flop

Welcome back to Basic Electronics. In the previous class we have seen the broad meaning of edge triggered flip-flops. We will now look at one of the most important elements in this category the JK flip-flop. In particular, we will consider the Master-Slave configuration of the JK flip-flop. And describe it is transition table with the help of an example. After understanding the basic operation of the JK flip-flop we will work out the output waveforms for a JK flip-flop with some given input waveforms. Let us get started.

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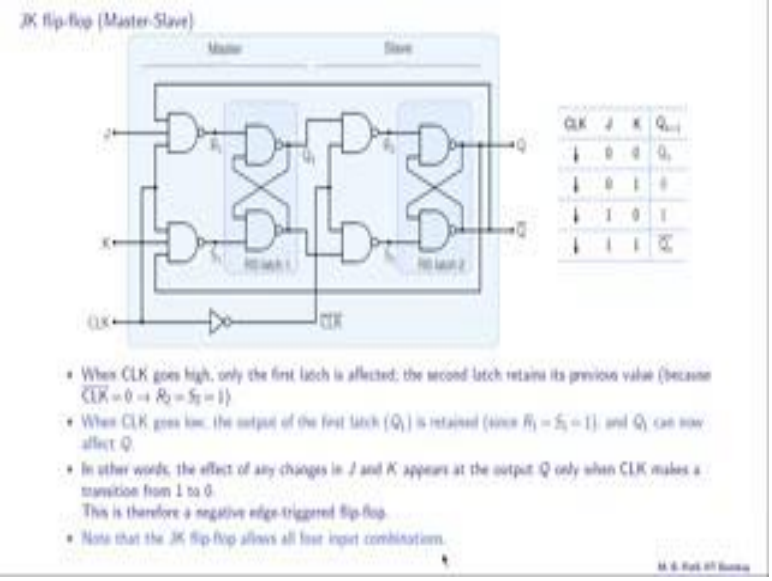

Let us now discuss the JK flip-flop. In particular, the Master-Slave configuration so here is the complete circuit for the JK flip-flop. These are the inputs clock J and K and outputs are Q and Q bar. Now within the JK flip-flop we have a master part this 1, and we have a slave part all right. Now the slave part looks very familiar it is nothing, but the clocked RS latch that we saw previously and the master part is also familiar except we have these 3 input nand gates now. This input is coming from Q bar of the JK flip-flop and this input is coming from Q of the JK flip-flop like that.

Both of these gate the clock signal. This one gets it directly and the second flip-flop the slave flip-flop gets it after inversion. When clock is 1 then there is a possibility of Q 1 changing depending of course, on these inputs J and K and Q and Q bar. And at that time clock bar is 0 so therefore, R 2 and S 2 are both equal to 1 and as we have seen before the output of the second flip-flop the slave flip-flop cannot change in that case. It continues to be whatever it was. Now consider the other situation when clock is 0, then this R 1 and S 1 R 1 and in that situation Q 1 cannot change clock bar is then one and therefore, we can see Q and Q bar change depending of course, on these inputs here so in summary if clock is 1 then the master is active the slave is not active because it is outputs cannot change in that interval. When clock is 0 then the master is inactive and the slave is active.

So, here is the summary. When clock goes high only the first latch is affected the master latch. The second latch retains it is previous value. And when the clock goes low the output of the first latch is retained it continues to be whatever it was. And Q 1 can now affect Q so now, there is a possibility that the slave output can change. In other words, the effect of any changes in J and K appears at the output Q only when the clock makes a transition from 1 to 0 when clock is 1 the data affects Q 1, J and K values. And when the clock goes 0 then this change gets transmitted to the output. So that is how it works. This is therefore, a negative edge triggered flip-flop, because we require the clock to be high and then go low.

And now it should be clear why this configuration is called the Master-Slave flip-flop. When J or K changes that change affects the master first and can cause Q 1 to change and the slave then simply follows. So, this change in Q 1 then affects the output of the slave flip-flop which is Q all right. Now here is the transition table for the JK flip-flop the JK Master-Slave flip-flop. And we come across this new symbol now that indicates a negative going edge in the clock; that means, the clock is going from 1 to 0. So only if that happens all of these entries are valid.

There is this new notation now Q and plus 1 and that is used to denote the value of Q after the nth clock pulse; and where the same token Q n means the value of Q before the nth clock pulse. And as we look at some examples the nomenclature here will become clear all right. Now let us look at this truth table. If J and K are both 0 then Q n plus 1 is the same as Q n. If J and K are both 1, then Q n plus 1 is Q and bar; that means, the

inverse of what it was earlier. If J 0 K is 1 then Q n plus 1 becomes 0 independent of it is past value and similarly if J is 1 K is 0 then Q n plus 1 becomes 1 irrespective of it is past value.

And this is a new feature note that the JK flip-flop allows all 4 input combinations. That is something that did not happen with the RS flip-flop. Let us look at some waveforms.

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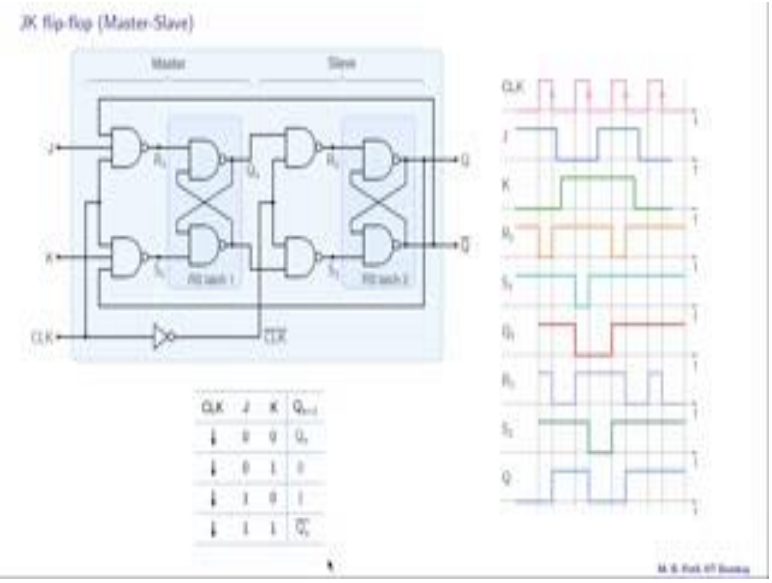

Now, for the Master-Slave JK flip-flop which we saw in the last slide; here is our clock and the active edge of the clock is indicated with this arrow here. And in this case that is a negative going edge because our flip-flop is a negative edge triggered flip-flop. This is the J input and that is the K input. And as a result of these input conditions we want to figure out how these variables R 1 S 1 Q 1 R 2 S 2 Q are going to vary Q of course, is the output of the flip-flop. In the beginning we will assume that Q is 0.

Let us start with some observations before we begin with the plot. These variables R 1 and S 1 would be 1 if the clock is 0 and that holds irrespective of the other inputs. And similarly R 2 S 2 would be 1 if clock bar is 0; that means, clock is equal to 1, so in these intervals when a clock is 0 here or here or here we are going to add R 1 and S 1 equal to 1 as shown here, and in these intervals this one and so on. We are going to have R 2 and S 2 equal to 1. So that is something that we can draw without even thinking of the other inputs to these gates.

Let us consider this interval in which clock is high, and as we just mentioned then clock high R 2 and S 2 R 1 no matter what the other variables are. And what can you say about Q if R 2 and S 2 are 1, R 2 equal to 1 S 2 equal to 1 this latch will hold it is output and therefore, Q does not change so Q remains equal to 0. All right now let us look at R 1 when clock is 1; that means, this input is 1 R 1 is the nand of J and this input which is Q bar and since Q is 0 Q bar is 1 J is also 1 and therefore, R 1 is equal to 0. What about S 1 S 1 similarly is the nand of K and Q and since K is 0, S 1 is going to be 1.

Now, if R 1 is 0 and S 1 is 1; that means, Q 1 is going to be 1. That is what we have shown over here. Let us now talk about this interval in which clock has become low once again. And as we discussed R 1 and S 1 are going to be 1 in this interval. If R 1 is 1 S 1 is 1 then this latch is going to hold it is output which is Q 1. So therefore, Q 1 cannot change. So we have R 1 equal to 1 S 1 equal to 1 and Q 1 remains what it was. What about R 2? R 2 is simply Q 1 bar, because this input is now 1. And that is what happens here Q 1 is 1 so R 2 it is 0. And S 2 is the complement of R 2 that is equal to 1. And now because R 2 is 0 and S 2 is 1 the output of this latch has changed to 1. And that is what we have shown over here. So the flip-flop output has now switched from 0 to 1.

Next let us take this interval in which clock is high, and as we discussed earlier in this interval R 2 and S 2 are going to be 1, and because R 2 S 2 are both 1, Q cannot change and that is what we see over here all right. What about R 1 R 1 is the nand of J and Q bar our J is 0 so R 1 is going to be 1 what about S 1, S 1 is the nand of K and Q, Q is 1 and K is also 1. So therefore, S 1 is going to be 0. If R 1 is 1 and S 1 is 0; that means, this latch is going to be reset to 0 and that is what we see over here.

This interval now clock is 0. So R 1 and S 1 are going to be 1 and Q 1 is not going to change like that. R 2 is Q 1 bar so that is 1 S 2 is the same as Q 1 that is 0 and now with R 2 equal to 1 and S 2 equal to 0 Q is going to be reset to 0; the output of this second latch.

Next this interval in which clock is high and we know that R 2 and S 2 are going to be 1 now, and therefore, Q is not going to change like that. What about R 1? R 1 is the nand of J and Q bar; Q bar is 1 and J is also 1 so therefore, R 1 has gone to 0, what about S 1, S 1 is the nand of K and Q. K is 1 and Q is 0. So therefore, S 1 is 1. If S 1 is 1 R 1 is 0, Q 1 is going to change to 1. Next interval clock is 0, so therefore, R 1 is going to be 1, S 1

is going to be 1, and Q 1 is not going to change. What about R 2 is the same as Q 1 bar and S 2 is the same as Q 1. So we have S 2 equal to 1 R 2 equal to 0 and therefore, Q is going to change from 0 to 1.

In this interval clock has become 1, therefore R 2 and S 2 are going to be 1 and Q will continue with what it was like that. R 1 nand of J and Q bar J is 0 so therefore, R 1 will be 1, S 1 nand of K and Q and K 0 so therefore, S 1 is also going to be 1. So we have R 1 equal to 1 S 1 equal to 1 so Q 1 is not going to change so that is what the situation is in this interval. The last interval, now they have clock equal to 0. So therefore, R 1 is going to be 1, S 1 is going to be 1 Q 1 will stay where it was at that. R 2 is Q 1 bar 0 S 2 is the same as Q 1, so 1 and Q will be determined by S 2 and R 2 so if S 2 is 1 R 2 is 0 Q will be equal to 1. So that is our overall flip-flop output waveform as a result of these input conditions.

So, as we have seen a lot of activity goes on inside this circuit, when we apply some input conditions like these and it can get a little mind boggling sometimes, but there is some good news. And that is we have this transition table. And we can use this table to go from the input conditions directly to the output Q of the JK flip-flop. And let us see now how that can be done. Let us start with Q equal to 0. And from this table we know that Q can change only after a negative clock edge. So only after this time can Q change? And now let us figure out whether Q changes from 0 to 1 or 2 may is equal to 0. And that is decided by this table entry here.

So just before this active edge which is the negative edges in this case of the clock let us look at the values of J and k. So just before that edge J is 1 and K is 0. Now let us refer to this table J equal to 1 and K equal to 0, and Q n plus 1 is 1 here. So therefore, the output is going to change to 1 at this point. And then nothing is going to happen to the output until the next active edge comes that one. And what is the situation just before this active edge J is 0 and K is 1. And that brings us to this row; that means, Q n plus 1 will be 0 and that is what happens over here.

Again nothing changes up to the next clock edge the next active edge and before that transition just before that we have J equal to 1 and K equal to 1, which means our Q n plus 1 is going to be Q n bar so; that means, the output is going to toggle. Since it was 0 earlier it is now going to become 1 and once again the output will stay constant up to the

next clock edge which is that one, and before that clock edge we have J equal to 0 K equal to 0, that brings us to this entry in the transition table and that says that Q n plus 1 is equal to Q n; that means, Q will continue to be what it was since it was 1, it will continue to be 1.

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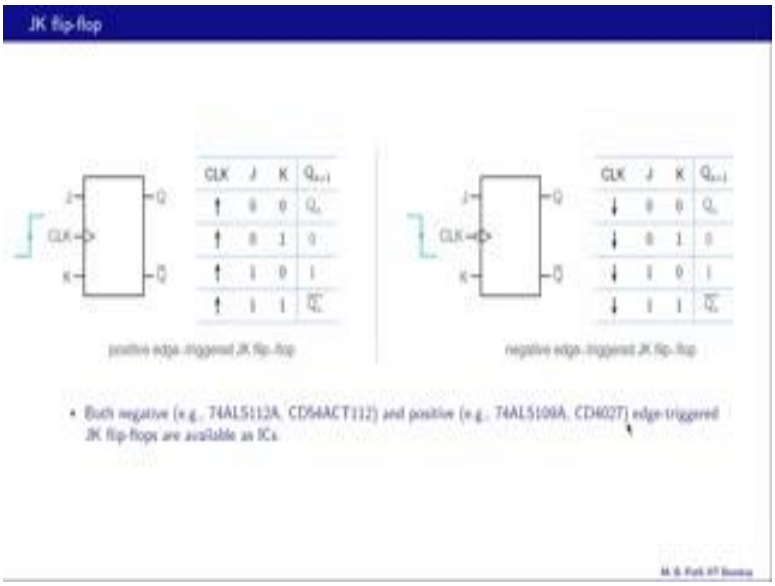

So, that is how simple it is. We really do not need to tax our minds with what goes on inside the flip-flop. And this transition table makes things nice and easy. JK flip-flops can be made either as positive edge triggered flip-flops or negative edge triggered flip-flops. We have already looked at the functionality of this one earlier that is the transition table for a negative edge triggered flip-flop.

And similarly here we have a positive edge triggered flip-flop. And that is the table for it. The only difference is here we have a positive going clock edge as activate, here we have a negative going clock edge as the activate edge. Otherwise these n keys are identical. And commercially both negative and positive edge triggered JK flip-flops are available as ICs. Here are some examples.

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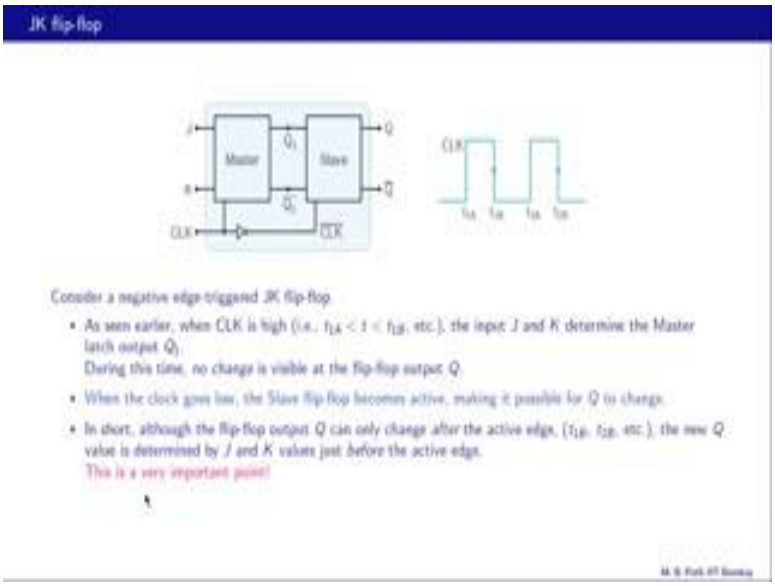

We would now like to make a very important point about the operation of JK flip-flops in particular edge triggered JK flip-flops. And we will do that by taking a negative edge triggered JK flip-flop as an example had shown here. This is the clock these are the active edges. The positive edge is denoted by t 1A the negative edge by t 1B for the first clock pulse. And for the second clock pulse the positive edge is t 2A and the negative edge is t 2B. As we have seen earlier when the clock is high for example, in this interval between t 1A and t 1B the J and K inputs determined the state of the master latch the output of the master latch is Q 1. During this time clock bar is 0 and therefore, the slave is not enabled. It is output does not change, that is Q does not change and Q is the flip-flop output.

So, during this time we do not see any change in the flip-flop output. Although things are happening inside the flip-flop in the master part all right now. When the clock goes low the slave flip-flop becomes active the master does not allow any changes anymore in Q 1 the slave flip-flop becomes active, and now this change which happened in Q 1 in the earlier phase that is clock equal to 1 phase, it gets transferred to the slave output which is Q.

In short, although the flip-flop output Q can only change after the active edge; that means, just after t 1B or t 2B the new Q value is determined by the J and K inputs just before the active edge; that means, just before t 1B or just before t 2B etcetera. So in

order to figure out what is going to happen to the flip-flop output after the active edge we need to look at the inputs just before that particular active edge. And that is a very important point and they must remember this point when we look at circuits which involved JK flip-flops.

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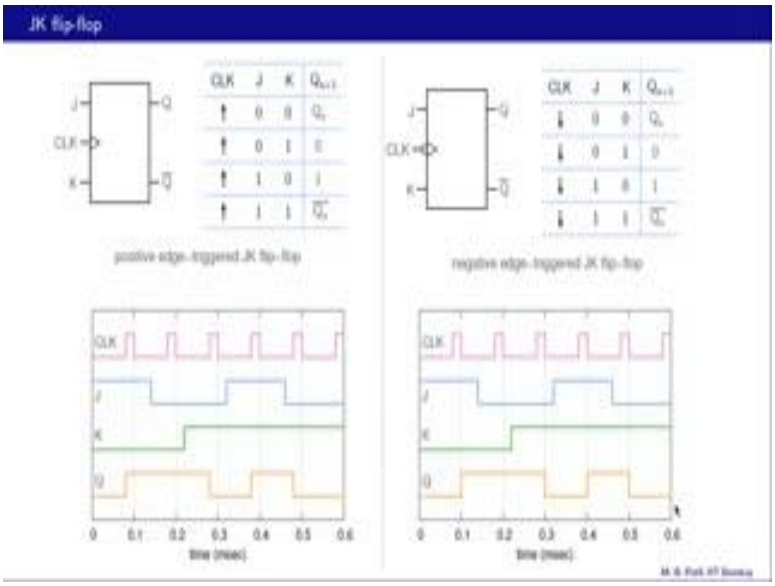

Let us now look at an example. And let us start with a positive edge triggered flip-flop. Here is the transition table these are our inputs clock J and K. And Q is given to be 0 in the beginning all right. Now the first change that we expect can only happen after the active edge which is a positive edge in this case and in order to figure out what that changes we need to look at the J and K inputs. Just before this edge and in this case J is 1 K is 0 we now go to this table J is 1 K is 0 so Q n plus 1 is going to be 1, and that will happen just after the active edge. So that is what we see over here.

Next change will happen at this active edge, and just before that J is 0 K is 0 and in that case Q n plus 1 remains equal to Q n so therefore, this Q equal to 1 will continue until we come to the next clock edge, the active edge. At that point or just before that active edge we have J equal to 0 K equal to 1, and then we expect Q n plus 1 to become 0. And that is what we see here the next active edge is here. And just before that we have J equal to 1 K is also equal to 1 so we look at this entry in the transition table and we see that Q n plus 1 each Q n bar; that means the output of the flip-flop toggles.

And since it was 0 earlier it will become one like that and after that we have this active edge before that we have J equal to 0 K equal to 1 there and therefore, Q n plus 1 will become 0 like that and when the next active edge comes this one, just prior to that we have J equal to 0 K equal to 1 and Q n plus 1 then becomes 0. And since it is already 0, we do not see any change.

Let us now consider the same inputs being applied to a negative edge triggered JK flip-flop. And as we have committed earlier the only difference between the 2 transition tables is the active edge. We have a positive clock edge as the active edge here, we have a negative clock edge has, a active edge and you are increased to go through all the transitions in the waveforms and verify that the cube waveform looks like this.

To conclude we have looked at the JK flip-flop. In particular, the Master-Slave configuration, we have seen why the J and K input values just before the active edge determined the output of the flip-flop just after the active edge. This is an extremely important point and is therefore, worth repeating here. Although the Master-Slave JK flip-flop is a complex circuit we found that is behavior can be represented by a simple transition table, and using this transition table we worked out the output waveforms for a JK flip-flop with some given input waveforms.

In subsequent lectures we will look at some practical applications of the JK flip-flop, until then goodbye.