Basic Electronics
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Lecture - 62
Latch and flip-flop

Welcome back to Basic Electronics. In this lecture we will look at a latch made up with NOR gates. We will then look at an application of an RS latch namely chatter removal. After that we will introduce the clock signal which plays a very important role in digital systems. We will see how a clocked RS latch works. Finally, we will look at the meaning of an edge triggered flip flop. Let us start.

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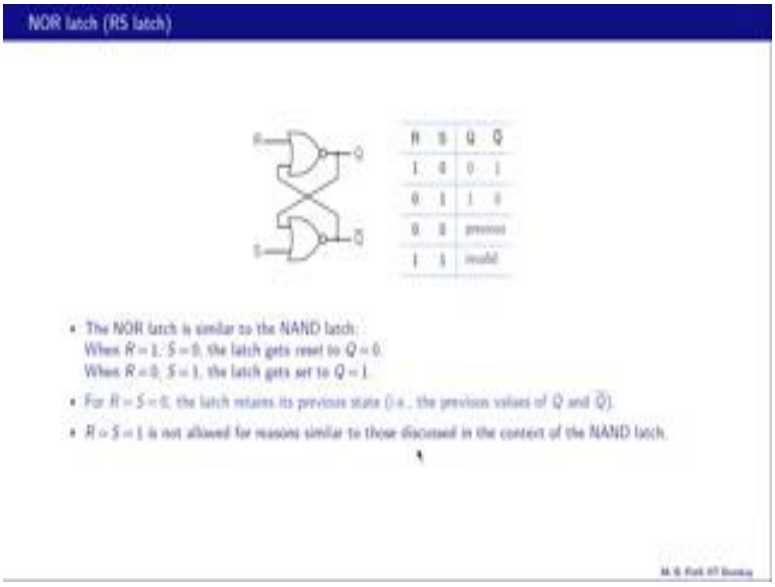

We can also make up latch using NOR gates. And that is shown over here. Let us see how it works. This input it turns out is the reset input, this is the set input, that is the Q output of the latch and that is the Q bar output of the latch. When R is 1 and S is 0 so we have 1 here as soon as R becomes equal to 1 no matter what the other input is Q will become 0. We have 0 here and we have S equal to 0 then Q bar becomes equal to 1. That explains the first entry. So with R equal to 1 S equal to 0, we have Q equal to 0 and Q bar equal to 1 and in the same fashion we can also figure out that for R equal to 0 and S equal to 1, we will get Q equal to 1 and Q bar equal to 0. So this is our reset input

because when it is active the latch output gets reset to 0, and this is our set input because when that is active the latch output gets set to 1.

When R is 0 and S is 0 the large continues to hold it is previous state. For example, if Q is 0 and Q bar equal to 1, then that state will continue. And if Q was 1 and Q bar was 0 then that state will continue. And that happens because when R is 0 this output is simply the not of this output, and similarly when S is 0 this output is the not of that output all right. Now when R and S are both equal to 1 that condition is termed invalid, for the same reasons that we discussed in the context of the nand latch.

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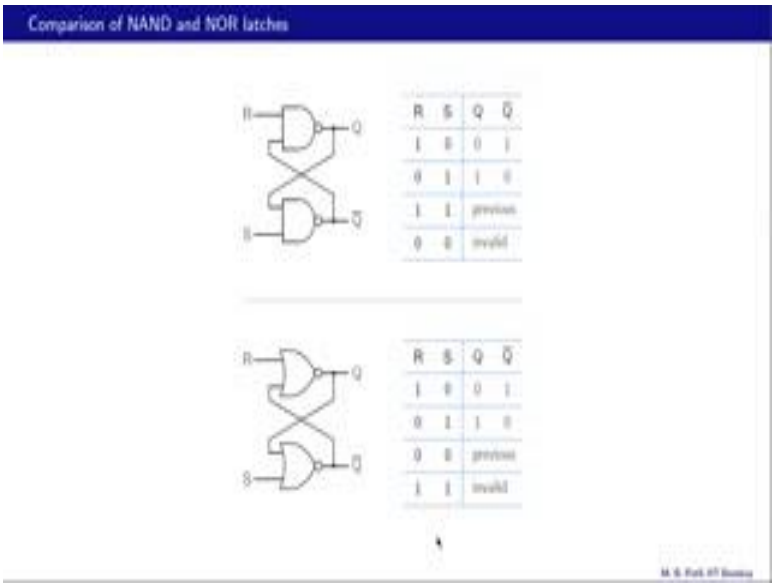

Here is a comparison of the nand and nor latches. The basic functionality of these 2 latches is similar. When reset is active and set is inactive, either there or here the output gets reset to 0 over there as well as here. When set is active and reset is inactive the output gates set to 1. Similarly, here the difference is in these 2 entries. For the nand latch the condition R equal to 1 S equal to 1 corresponds to the previous state continuing as the next state whereas, for the nor latch that condition is R equal to 0 S equal to 0. In this case R equal to S equal to 0 is invalid in this case R equal to S equal to 1 is invalid.

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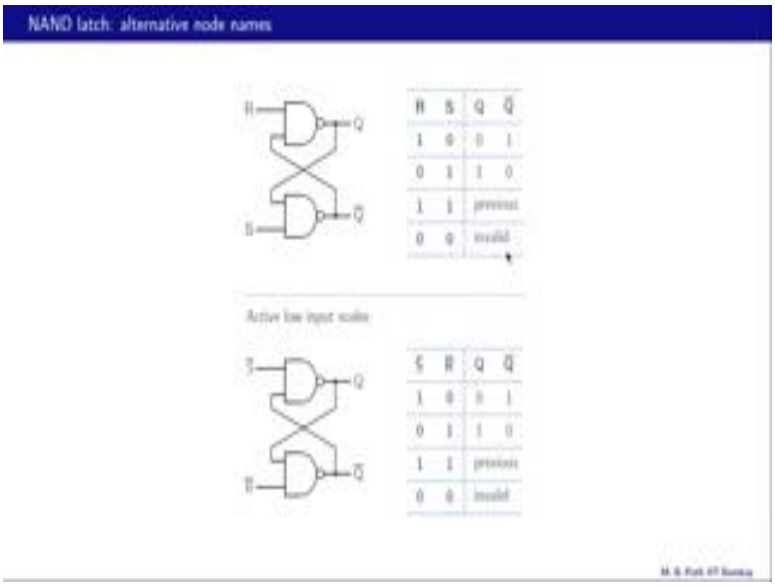

Otherwise these 2 latches are similar. Instead of having active high inputs, like we saw in this nand latch, we can also have active low inputs. And that circuit is shown over here. We have S bar now and R bar. And S bar is active when it is low so; that means, S bar equal to 0 corresponds to S equal to 1 in this configuration, in the top configuration all right. Let us try to understand the table now for this circuit. If S bar is 1 R bar is 0 what does it mean; that means, the reset input is active set input is inactive and that corresponds to this first entry over here.

Similarly, when S bar is 0 and R bar is 1; that means, the set input is active the reset input is inactive that corresponds to this row here R equal to 0 and S equal to 1. When S bar and R bar are both 1 that situation is the same as R and S equal to 1 here and therefore, the previous output of the latch continues and that is indicated by previous here. And similarly when S bar and R bar are both 0 that is the same situation as R and S both 0 in the top configuration and that condition is invalid in both cases.

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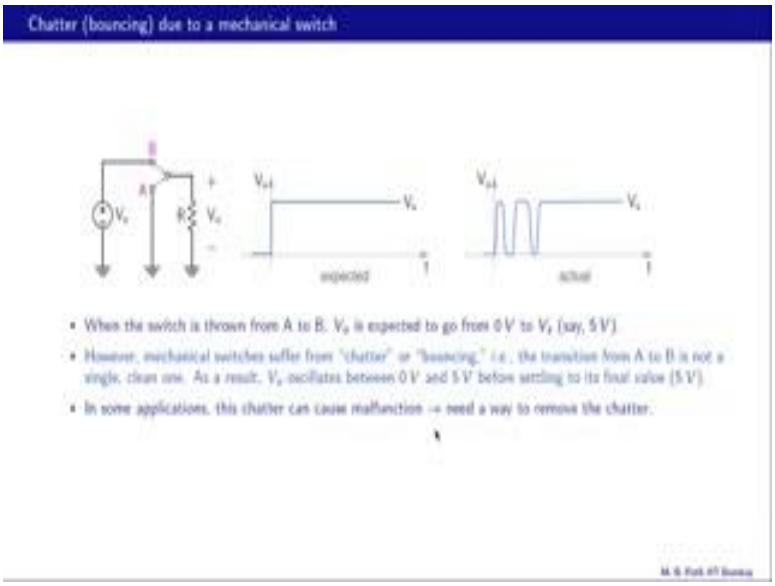

Let us now look at a simple application of the RS latch. Let us look at this circuit. We have a power supply here V s say 5 volts. We have a switch here the switch position can be either like that or like that. And then we have a load R. That is our output voltage across the load. Now when the switch is thrown from A to B our output voltage is expected to go from 0 volts to V s say 5 volts. When the switch is in that position a then V o is of course, 0 and when the switch is thrown to that position then we expect V o to be 5 volts like that.

Let us say that the switch position is changed from A to B at t equal to 0 right here, then this is what we would expect as the waveform for V o. In reality what we get is this waveform for example, and instead of one single transition from 0 to 5 we have some other strange waveform and finally, it settles down at 5 volts. Now this happens because mechanical switches suffer from chatter or bouncing that is the transition from A to B is not a single clean transition. There are times when the switch is neither firmly in this position nor in that position. And that gives rise to these oscillations. As a result, V o oscillates between 0 volts and 5 volts before settling down to it is final value over there.

So, clearly there is a problem. Instead of a single transition we have now got this strange waveform. And in some applications this chatter can cause malfunction. For example, if we are counting this low to high transitions, using an electronic circuit we will feed that V o waveform to that electronic circuit and the electronic circuit will then count this low

to high transitions. So what we expect is that the count will go up by 1 when we turn the switch from A to B in reality what will happen is the count will go up by 3 because there is 1 transition here another transition here and a third transition here. So clearly there is a problem and we need a way to remove this chatter.

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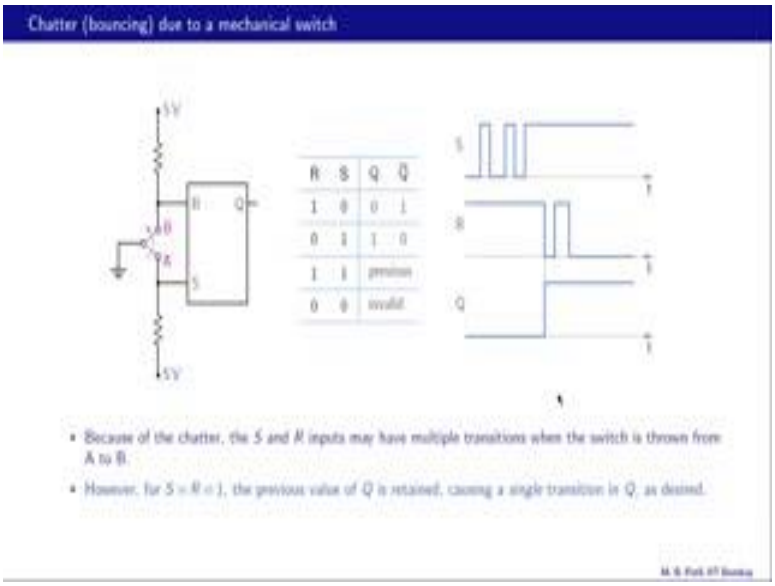

Let us now consider this circuit, which uses an RS latch. Here is the mechanical switch which has this chatter or bouncing problem, which we want to remove. Consider 2 positions for the switch position A in which this connection is open input S is 0 and input R is pulled up to 5 volts, because this part is open circuit. When the switch is in position B then R gets connected to 0 this is an open circuit. And S gets pulled up to 5 volts; that means, as we change the switch position from A to B we go from S equal to 0 R equal to 1 this situation here to R equal to 0 S equal to 1.

So, our intention is to go from this situation S equal to 0 R equal to 1, that is the switch in position a to this position where S is 1 and R is 0 that is the switches in position B, and for this condition S equal to 0 R equal to 1 we have Q equal to 0 and for this condition S equal to 1 R equal to 0 we have Q equal to 1, so the transition that we want is Q going from 0 to 1. And there is a problem because we have this mechanical switch and that gives these oscillations in the S input as well as in the R input.

Let us now check whether these oscillations in S or R inputs, give us the same problem that we saw in the last slide that is multiple transitions in the output. Let us start at this

point S equal to 0 and R equal to 1, this first row here Q is 0 like that, and now at this point S goes from 0 to 1 R continues to be 1 so we now have S equal to 1 and R equal to 1 and; that means, that Q will continue with it is previous value which was 0. So Q continues to be 0 at this point S changes from 1 to 0 and once again we have S equal to 0 R equal to 1 this row here and Q remains equal to 0.

So, that happens all the way up to this point. At this point R changes from 1 to 0 S has already reached it is final destination that is S equal to 1. So in this interval we have R equal to 0 S equal to 1 R equal to 0 S equal to 1 so Q will become 1, so Q will go from 0 to 1 here, and now in this interval RS changed again to 1 so we have S equal to 1 R equal to 1, but Q will now hold it is previous value which is Q equal to 1. So therefore, Q does not change and finally, we have S equal to 1 R equal to 0 S equal to 1 R equal to 0 and Q remains equal to 1 like that. So therefore, we have now achieved a single clean transition in the output although we do have a mechanical switch which gives us bouncing problems. And this process is called debouncing.

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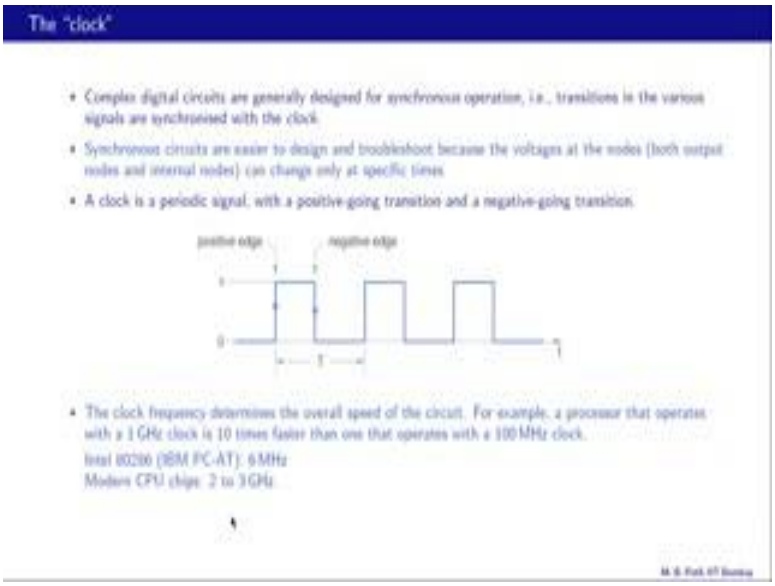

Let us now talk about the clock, which is periodic signal used to synchronize various operations that happen inside for example, microprocessor or a complex digital system in general. So complex digital circuits are generally designed for synchronous operation that is transitions in the various signals are synchronized with the clock, so that is the function of the clock. To take an example from real life we have day and night and that

provides some synchronization to us we all get up at about the same time we go to the office we work together as a team toward a certain output. Now imagine that we did not have day and night. Then we would all get up at various times, go to office at different times and there would be no such thing as team work. And clearly that situation would be very chaotic and inefficient.

And the clock serves a similar purpose in a complex digital system. It turns out that synchronous circuits are easier to design much easier to design and troubleshoot because the voltages at the nodes both output nodes and the nodes which are internal to that digital system, can change only at specific times, that makes a big difference.

Let us now look at what a clock is a clock is a periodic signal with a positive going transition and a negative going transition. So here is the clock. This is 1 period the period is T it has got a positive edge going from 0 to 1 and it has got a negative edge going from 1 to 0. And it is the clock frequency given by 1 over T which determines the overall speed of the circuit. For example, a processor that operates with a 1 gigahertz clock is 10 times faster than one that operates with a 100 megahertz clock.

Here are some examples the intel 8286 processor one of the early processors which was used in IBM PC-AT had a clock rate of 6 megahertz, whereas today's computers the PCs that we use have CPUs which operate at 2 to 3 gigahertz. So that is 500 times faster than the IBM PC-AT. So that is how dramatically things have changed.

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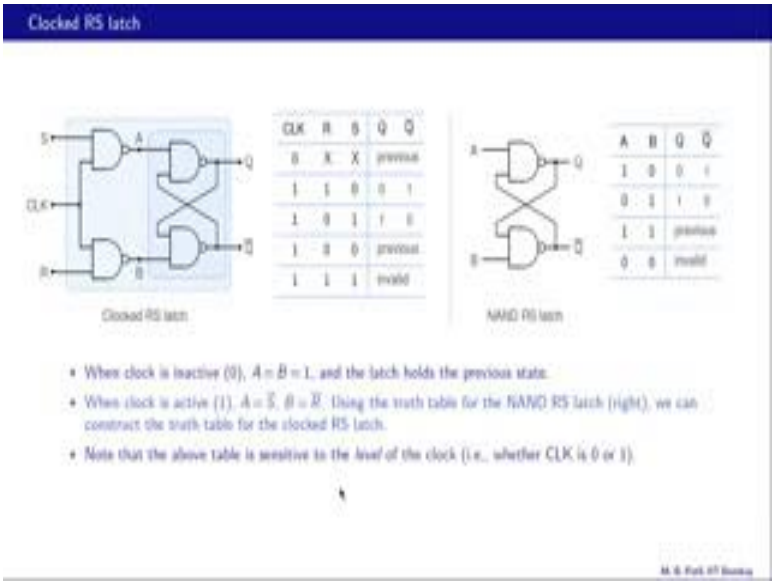

Let us now look at a clocked RS latch. So it has this additional clock input, apart from S and R inputs. And it has got this block which is already familiar to us it is reproduced over here that is the nand latch. And what we will do is call these inputs A and B because S and R would be reserved for these inputs here in the clocked latch. Now in terms of these inputs the operation of this latch is described over here. When A is 1 B is 0 Q is equal to 0. When A is 0 B is 1 Q is set to 1. When both are 1 then the latch holds it is previous state there is no change in Q or Q bar. And A equal to B equal to 0 is invalid as we have seen earlier.

Let us now look at the clocked latch, with clock equal to 0. If clock is 0 then A would be 1 B also would be 1, and that is irrespective of S and R; that means, S and R are do not care conditions in this case. So that is what this is. Now if A and B are 1 then we are referring to this row here; that means, Q and Q bar will continue with their previous values like that. So that explains this first row over here so as long as clock is 0 the latch outputs do not change. So for anything to happen we must have clock equal to 1 as in these subsequent entries.

When clock is 1 A is S bar and B is R bar. And knowing that and knowing this table we can now construct the rest of the entries in this table here these 4 entries. Let us take R equal to 1, in that case B would be R bar that is 0, S equal to 0 A would be S bar or 1, so we have a equal to 1 B equal to 0 that is this row here; that means, Q would be 0 and that is what we have over here.

Let us take this row now R is 0 so therefore, B is 1 S is 1 therefore, a is 0 so A is 0 and B is 1 that brings us to this row here and; that means, Q would be 1 like that. What about R equal to is equal to 0; that means, both A and B would be 1; that means, Q would be the previous value of Q like that. And when R and S are both 1; that means, A and B would be 0 0 and that condition is invalid.

Here is the summary. When clock is inactive that is 0. A and B are both equal to 1 and the latch holds the previous state. This entry here when clock is active or 1 then A is S bar B is R bar and using the truth table for the nand RS latch on the right hand side this table we can now construct the truth table for the clocked RS latch this 1. And let us remember that the above table is sensitive to the level of the clock whether the clock is at

level 0 or at level 1. Later we will see flip flops which are sensitive to transitions in the level either from 0 to 1 or 1 to 0.

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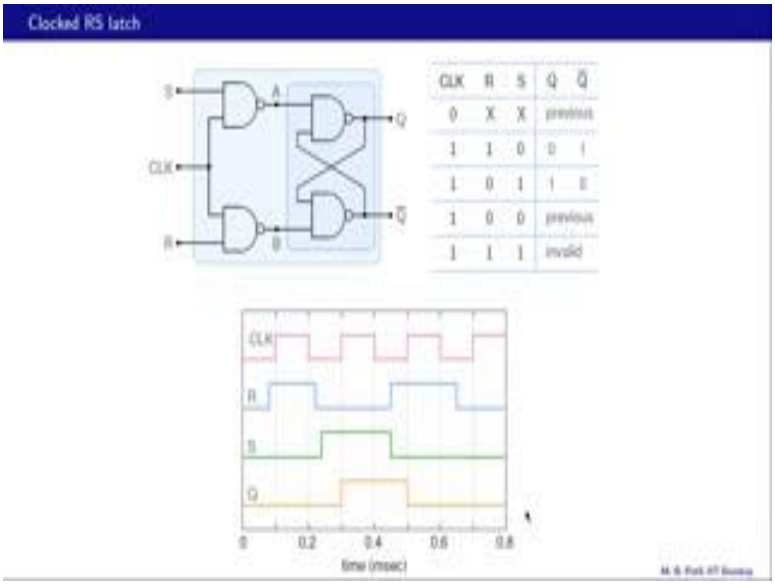

Let us now try to understand these waveforms for the clocked RS latch using this table here which we looked at in the last slide. So here is the clock waveform, periodic. Here is the R input given to us and here is the S input. And let us assume that the latch starts in a state Q equal to 0. So at t equal to 0 we have Q equal to 0. Now as a result of these inputs and the clock waveform, let us see what Q should be, point number one, nothing would happen when clock is 0 so up to this point nothing is expected to happen because when clock is 0 Q just continues with it is previous value so that happens up to here.

All right now in this interval clock is equal to 1 and R is 1 S is 0, so we look up this entry now R is 1 S is 0 and Q is shown here as 0. So Q will continue to be 0 in this interval. Now we have clock equal to 0 so that thing is expected to happen we do not even need to look at R and S. So we draw this Q equal to 0 parts here. Now the clock has become 1 there R is 0 S is 1 R is 0 S is 1 so Q has become 1 and that is why we have shown this transition here. Once again clock has become 0 there and therefore, this will continue.

At this point clock turns one again we have R equal to 1 S equal to 0, Q becomes equal to 0. So we have a transition now from 1 to 0. Now clock is 0 in this interval so Q cannot change and in the last interval here clock is 1, R is 0 S is 0 R is 0 S is 0 so; that means Q

would be it is previous value. So Q will continue to be 0. And that is our complete Q waveform.

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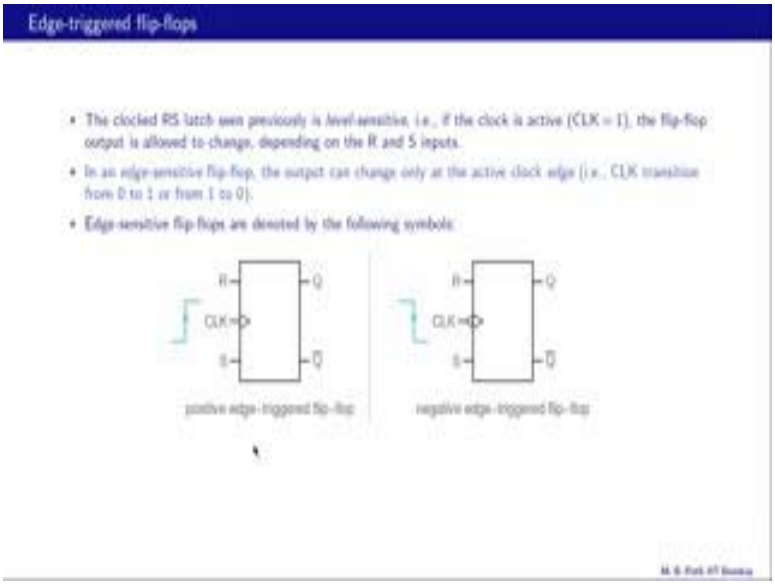

Let us now talk about edge triggered flip flops, which are very commonly used. The clock RS latch which we have seen earlier is level sensitive as we remarked earlier as well; that means, it is operation is sensitive to the level of the clock whether the clock is 0 or 1. If the clock is active clocks equal to 1 the flip flop output is allowed to change depending on the R and S inputs. If clock is 0 then Q cannot change it continues with it is earlier value.

On the other hand, in an edge sensitive flip flop the output can change only at the active clock edge; so level equal to 0 or level equal to 1 is not sufficient. What is required is an edge that is clock transition from either 0 to 1 or from 1 to 0. And here are the symbols for edge triggered flip flops or edge sensitive flip flops. Here is a positive edge triggered flip flop; that means, it is triggered by a positive edge in the clock. What is the positive edge? It goes from 0 to 1. This is the symbol for a negative edge triggered flip flop. It is triggered by a negative edge in the clock, which goes from 1 to 0 like that.

Now, the common feature of these symbols is this triangle. That triangle indicates that it is in edge triggered flip flop. And whether it is a positive edge triggered flip flop or a negative edge triggered flip flop is indicated by this circle here. If we have a circle here, then that is a negative edge triggered flip flop. And absence of the circle indicates that it

is a positive edge triggered flip flop. So, from the symbol we should be able to make out whether it is an edge triggered flip flop and if so whether it is a positive or negative edge triggered flip flop.

Let us summarize we have introduced a very important concept called the clock. We have seen an example of a clocked latch; we have also seen what is meant by an edge triggered flip flop. In the following lectures we will consider some specific edge triggered flip flops and their applications. See you in the next class.