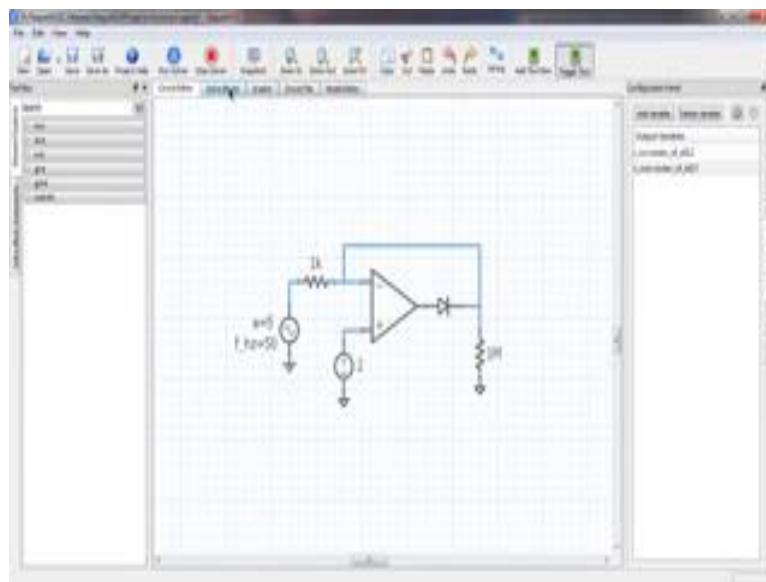


**Basic Electronics**  
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**Lecture - 47**  
**Precision Rectifiers (Continued)**

Welcome back to Basic Electronics. In this lecture, we will continue to look at the precision clipper and clamper circuits, which we saw in the previous lecture. We will also take a second look at the half-wave rectifier based on the super diode; and in particular look at its response to an input signal with a relatively higher frequency. So, let us begin.

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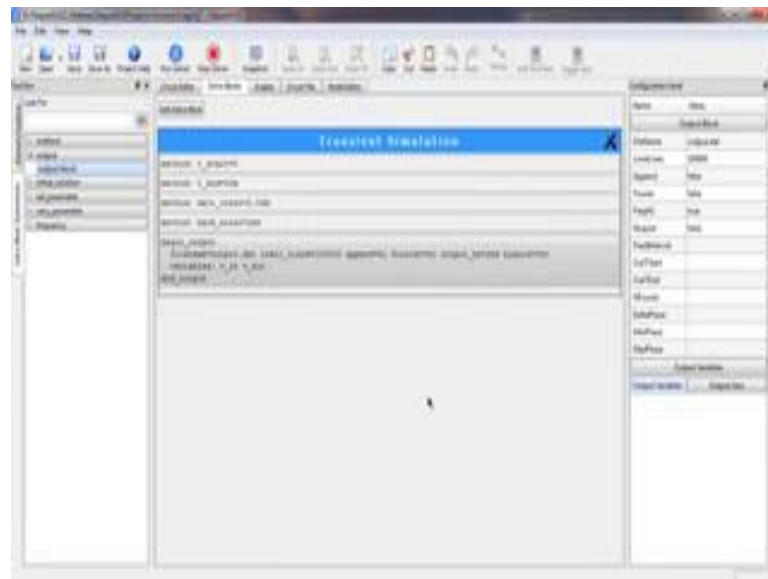


Let us simulate the circuit that we just looked at this circuit here; and verify its operation. To begin with let us create the components that we require. We will use the 741 op-amp, registers of course. Then we require a diode, we will use the spice diode model. We require a DC voltage source for  $V_R$  that is called VSRC DC. We require an ac voltage source as the input voltage that is VSRC AC. And we also require the reference node that is ground.

Our next step is to make the connections. So, let us do that. Let us now assign the component values this resistance it can be 1 k, and we will consider the case in which  $r_1$  is much larger than this  $r$  here. So,  $r_1$  could be let say 1 mega ohm like that. This  $V_R$

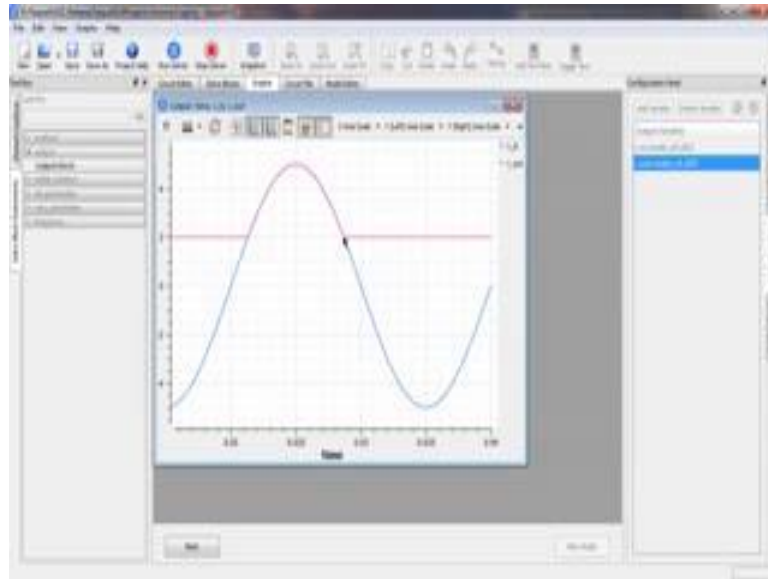
could be 2 volts, later we can change it if we want. This is our input voltage, we can make the amplitude equal to 5 volts, and select a relatively low frequency let say 50 hertz because a 741 op-amp is not going to work at higher frequencies. We can also display these values. So, this has amplitude of 5, and frequency 50 hertz. Our next step is to define the output variables. We will define two output variables, one - the input voltage; and the second - the output voltage. We can change these names v in and v out. We can now go to the solve block section and define the solve blocks.

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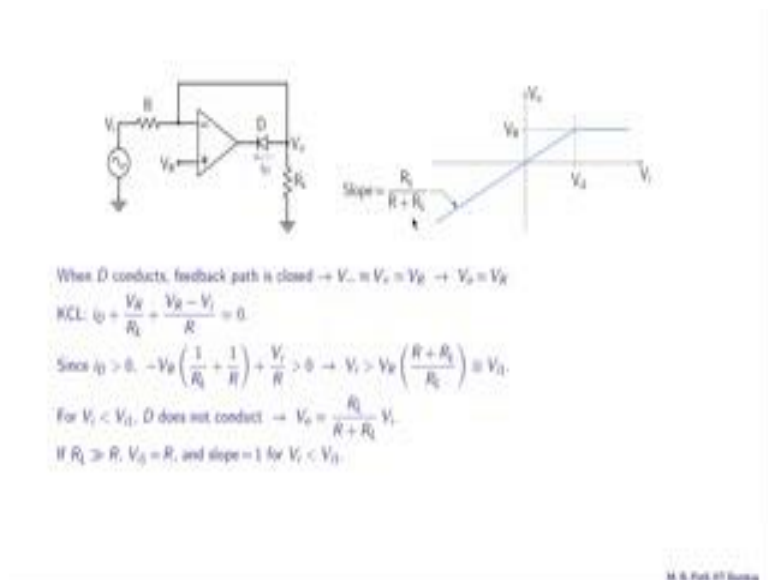
Let us now define our solve block. We want to do transient simulation. So, we need to change this DC to transient like that. Our time period is 20 milliseconds. So, let say we simulate for two cycles that is 40 milliseconds with a time step of 0.02 milliseconds for small time step compared to the period. And now we need to get the output block and the output block we will select both v in and v out.

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Let us run the simulation now and look at both v in and v out together. So, this is what we have let us look at only the steady part. So, if  $V_i$  is less than 2 volts - this part here, our  $V_o$  is 2 volts that is  $V_R$  and other wise  $V_o$  is equal to  $v_i$  as we would expect.

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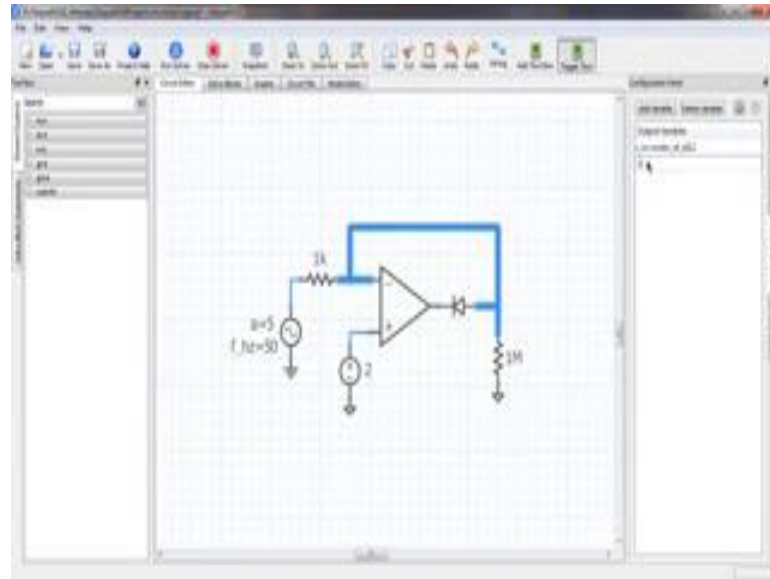
Here is our second circuit the only difference between this circuit and our previous circuit is that the diode has now been reversed. Let us see what it is doing. First, when the diode conducts, the feedback path is closed like that; and we can expect  $V_{\text{minus}}$  and  $V_{\text{plus}}$  to be nearly equal; and since  $V_{\text{plus}}$  is equal to  $V_R$ ,  $V_{\text{minus}}$  is also equal to  $V_R$ .

And since  $V_o$  and  $v_{\text{minus}}$  are the same where  $V_o$  equal to  $V_R$ . Let us now look at the diode current and in particular let us write the KCL equation at this node here. We have three currents  $i_D$  this current and this current, which is the same as the current through  $R$  that means  $i_D$  plus  $V_R$  by  $R_L$  that is this current. Since  $V_o$  is equal to  $V_R$  plus this current, which is equal to  $V_R$  minus  $V_i$  divided by  $R$  that should be equal to 0.

Now, since the diode current can only be positive, we get this condition minus  $V_R$  times  $1$  over  $R_L$  plus one over  $R$  plus  $V_i$  by  $R$  greater than 0; and that implies that  $V_R$  must be greater than  $V_R$  times  $R$  plus  $R_L$  over  $R_L$ . Once again let us define this quantity as  $V_{i1}$ , and since this factor  $V$  is greater 1;  $V_{i1}$  is generally greater than  $V_R$ . In the other case that is  $V_i$  less than  $V_{i1}$  the diode does not conduct, so we do not have this current here; and  $V_i$  then divided between  $R$  and  $R_L$  and  $V_o$  is given by voltage division. So,  $V_o$  in that case is  $R_L$  by  $R$  plus  $R_L$  times  $V_R$ . So, to summarize if  $V_i$  is greater than  $V_{i1}$  the output voltage is equal to  $V_R$  otherwise the output voltage is  $R_L$  by  $R$  plus  $R_L$  times  $V_i$ .

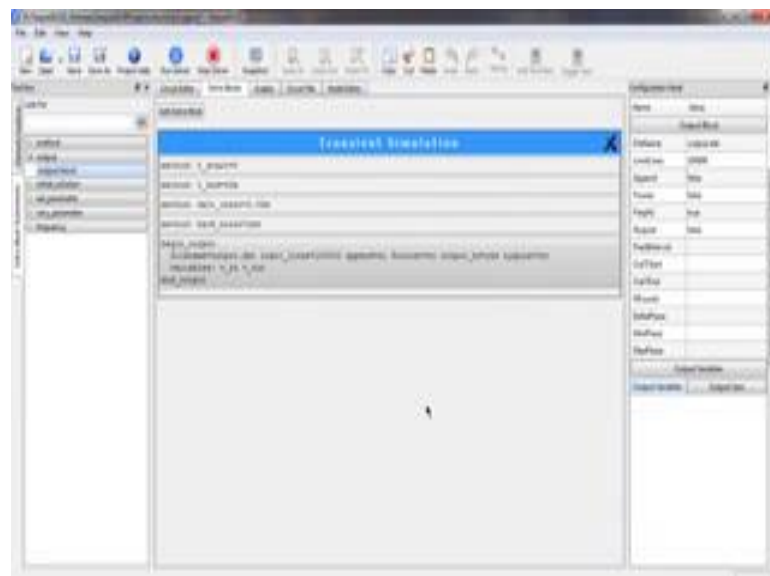
Here is the graph of  $V_o$  as a function of  $V_i$  this is the  $V_o$  axis that is the  $V_i$  axis. If  $V_i$  is greater than  $V_{i1}$  that means this region  $V_o$  is equal to  $V_i$  a constant; otherwise, we have the straight line which passes through the origin and has a slope of  $R_L$  by  $R$  plus  $R_L$ . So, this circuit is also a clipper and its clips voltages which are greater than  $V_{i1}$ . And once again as a special case, let us consider  $R_L$  to be much larger than  $R$ , in that case our  $V_{i1}$  is equal to  $V_R$  because this factor becomes equal to 1, and a slope of this straight line also becomes equal to 1.

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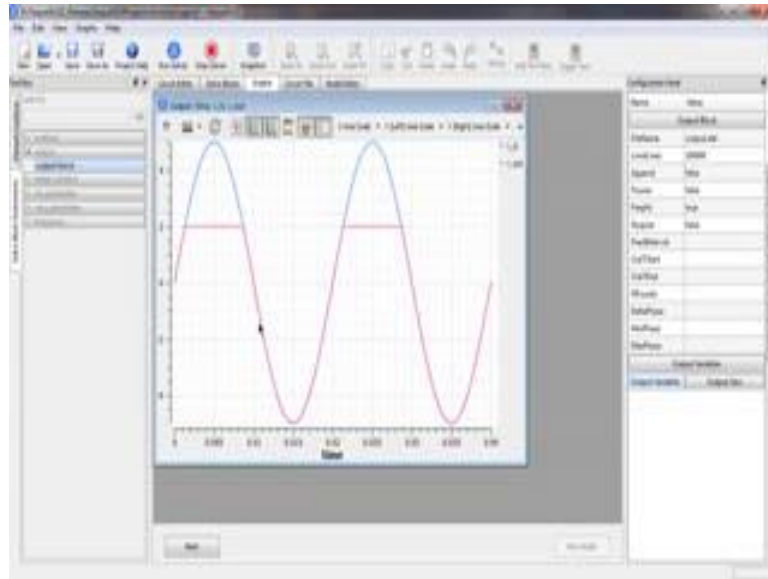


Let us simulate the circuit now and verify that the functionality we have predicted is actually observed in the simulation results. This is our previous circuit. All we need to do now is to reverse the direction of this diode. So, let us do that we select the diode first control x, control v, and now we can reverse the diode by pressing R two times, make the connections. You need to add this node voltage here as the output variable. So, let us do that and we will call that V out.

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Let us now go to solve blocks; we need to add  $v_{out}$  over here in the output variables. And now we can simulate the circuit, so that is our result. And as we expected, if  $V_i$  is greater than 2 volts that is  $V_R$ , our output voltage is constant that is equal to  $V_R$ ; otherwise,  $V_o$  and  $V_i$  are equal over here.

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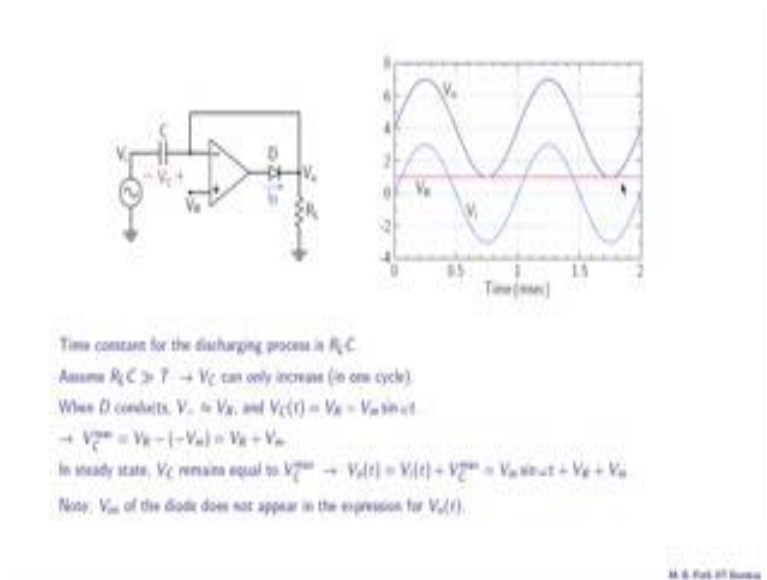
Clipping and clamping

- What is the function provided by each circuit?
- Verify with simulation (and in the lab)

M. G. Park of Sonoma

So, we have looked at two of the circuits so far this one and this one. And they are both precision clippers that means, the diode voltage drop  $V_R$  does not appear in the  $V_o$  versus  $V_i$  relationship. Let us proceed further and look at these other two circuits.

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Here is our third circuit. And we have a capacitor now. Let us see what it is doing. We have defined the capacitor voltage with plus here and minus here. If the current through the capacitor flows in that direction then  $V_c$  will increase; if the current flows in the other direction like that then  $V_c$  will decrease. Now, the key point in understanding this circuit is that if the capacitor voltage has to decrease, the current has to flow like that and that can only happen if the current flows through  $R_L$ , because the diode does not conduct in that direction.

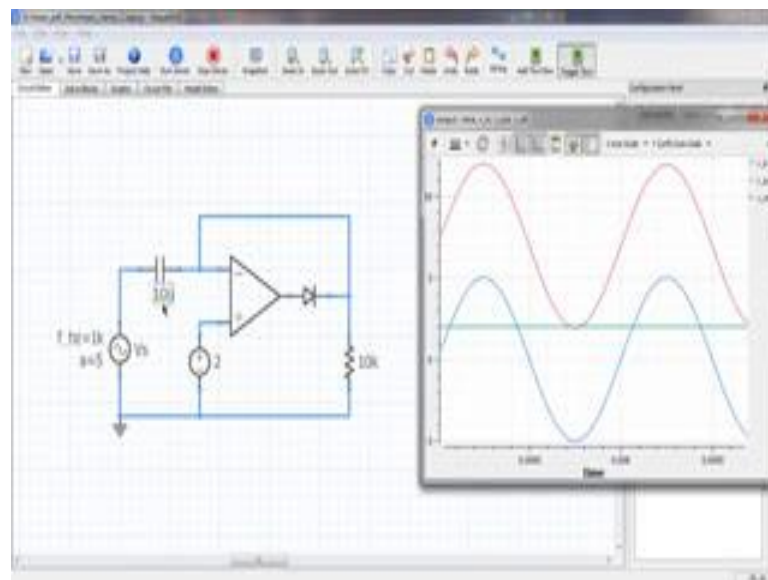
So, the time constant for the discharging process that means, the process of decreasing  $V_c$  is  $R_L C$ , because the diode is not in the picture. And if  $R_L C$  is much larger than one period of the input voltage then in a given cycle  $V_c$  can only increase, so that is a very important conclusion, and we can use that to see what the circuit is doing. Let us consider the interval in which the diode  $D$  conducts and that happens the feedback loop is closed  $V_{\text{minus}}$  and  $V_{\text{plus}}$  would be nearly equal and therefore,  $V_{\text{minus}}$  would be equal to  $V_R$ . And what is the capacitor voltage in that case the capacitor voltage is  $V_{\text{minus}} - V_i$  that is  $V_R - V_i$  or  $V_R - V_m \sin \omega t$ .

Now, this quantity is maximum then this  $V_m \sin \omega t$  is minimum. And what is the minimum value of  $V_m \sin \omega t$  it is simply  $-V_m$ . So, therefore, we have  $V_c^{\text{max}}$  equal to  $V_R - (-V_m)$  or  $V_R + V_m$ . And as we mentioned once the capacitor voltage reaches this maximum value, it cannot decrease any more as long as

this assumption holds. And therefore, in steady state we can say that  $V_c$  remains equal to  $V_{c \max}$ . And therefore,  $V_o$  the output voltage is  $V_i$  plus  $v_c$  which is  $V_i$  plus  $V_{c \max}$  like that that is equal to  $V_m \sin \omega t$  plus  $V_R$  plus  $V_m$ .

And notice that the on voltage  $V_{on}$  of the diode does not appear in this expression. Here is an example the input voltage has an amplitude of 3 volts. So, it varies between plus 3 and minus 3. This is our  $V_R$  equal to 1 volt. And our output voltage is  $V_i$  plus  $V_R$  plus  $V_m$  and that essentially serves to clamp  $V_o$  exactly at  $V_R$  as we see in this plot.

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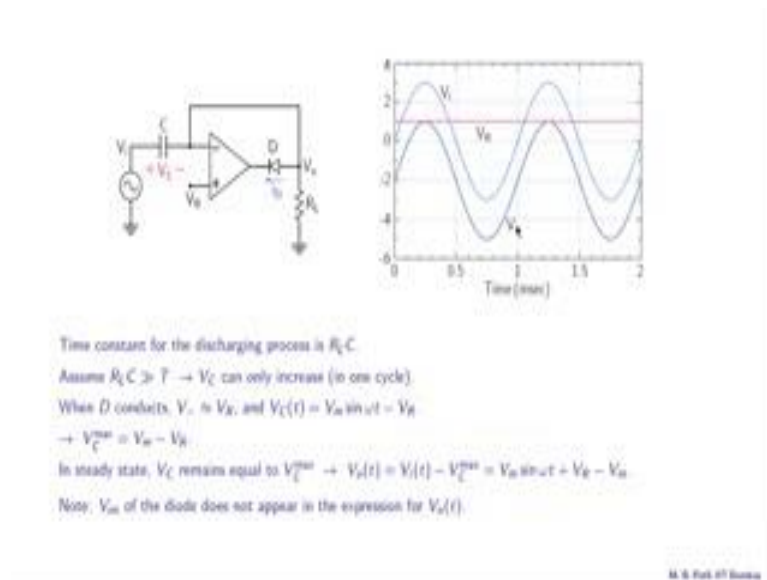


Let us look at the simulation results now. The capacitance we have chosen is 10 micro and  $R_L$  is 10 kilo ohms. So,  $R_L$  time  $C$  is 10 k times 10 micro or 100 milliseconds. Let us now see how that compares with the period of the input waveform. The input voltage has a frequency of 1 kilo hertz; that means, the time period of 1 millisecond. So, we have to compare 1 millisecond with  $R_L$  times  $C$  which is 100 milliseconds. So; obviously, 100 milliseconds is much larger than 1 millisecond. And our assumption that  $R_L$  times  $C$  is much larger than  $t$  is satisfied.

Let us look at the plots now. The blue graph is the input voltage; it has amplitude of 5 volts. So, it goes between plus 5 and minus 5. The green line is our  $V_R$  that is 2 volts and red one is the output voltage. So, as we would expect the output voltage has the same amplitude as the input voltage, but it is shifted up such that it is clamped at  $V_R$  that is 2 volts.



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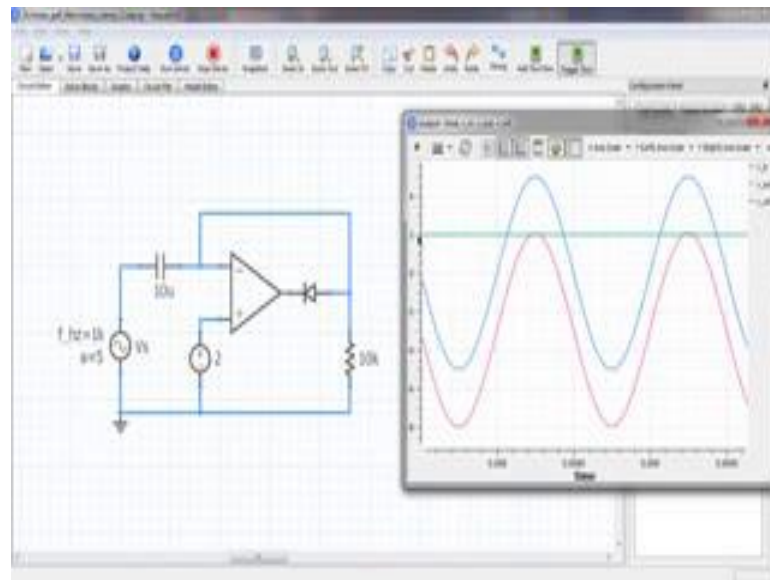


Now, let us consider our last circuit; it is quite similar to the previous circuit except the diode direction has been reversed. And note that we have indicated  $V_c$  with a plus here and minus here. If  $V_c$  has to increase, the capacitor current must flow like that; and if  $V_c$  has to decrease and the capacitor current must flow in the opposite direction like that. Let us now consider the case in which  $V_c$  is decreasing, that means the capacitor is discharging. Now, the only way that can happen is if the current path is through  $R_L$  and then through the capacitor and that is because the diode cannot conduct in this direction. In other words, the time constant for the discharging process is  $R_L C$ ; and if  $R_L C$  is much larger than  $T$ , the time period of the input waveform then in a given cycle  $V_c$  can only increase.

Let us consider the interval in which the diode is conducting that means, this would not loop is closed and  $V_{in}$  and  $V_{out}$  are nearly equal that means,  $V_{in} - V_{out}$  is equal to  $V_D$ . And the capacitor voltage in that case is  $V_{in} - V_D$  that is  $V_m \sin \omega t - V_D$ . And the maximum value of  $V_c$  is simply  $V_m - V_D$ . So,  $V_c^{max}$  is  $V_m - V_D$ . Then the capacitor voltage reaches this maximum value  $V_m - V_D$  it cannot decrease as long this condition is satisfied. And therefore, in steady state  $V_c$  remains equal to  $V_c^{max}$  and the output voltage is then given by  $V_{in} - V_c$  that is  $V_{in} - V_c^{max}$  or  $V_m \sin \omega t + V_D - V_m$ . And as in the previous case, the diode voltage drop  $V_D$  does not appear in this expression for  $V_o(t)$ .

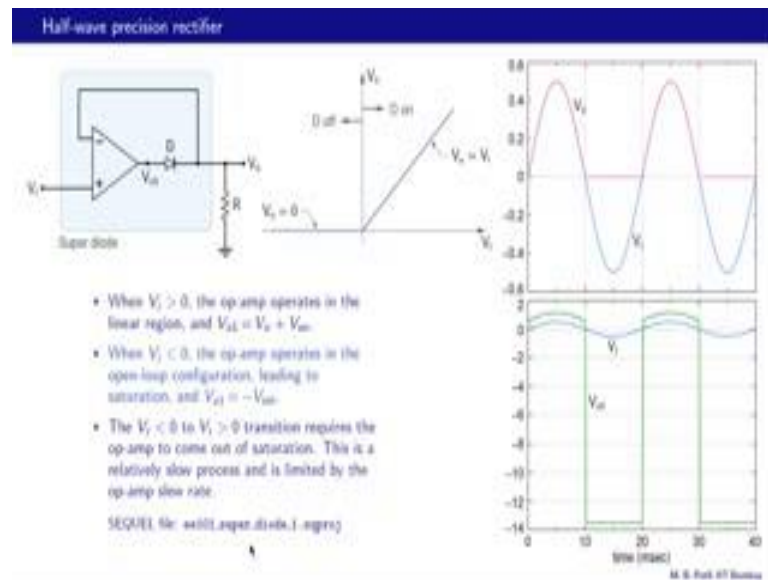
Let us now look at the plots. This is our input voltage with an amplitude of 3 volts. So, it varies between plus 3 and minus 3 that is  $v_R$  which is equal to 1, volt and that is our output voltage. So, the output voltage in this case has got shifted downward and it has got clamped precisely at  $V_R$ .

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Let us look at the simulation results now. The circuit shown here is identical to our previous circuit that means, you have the same  $C$  value here, same  $R_L$ , same frequency; the only difference is that the diode has been reversed. Here the plots this is the input voltage it has an amplitude of 5 volts, so it varies between minus 5 volts and plus 5 volts. That is our  $V_R$  equal to plus 2 volts and the red graph is the output voltage. And as we expect it was being shifted downward, and it has got clamped at  $V_R$  that is 2 volts.

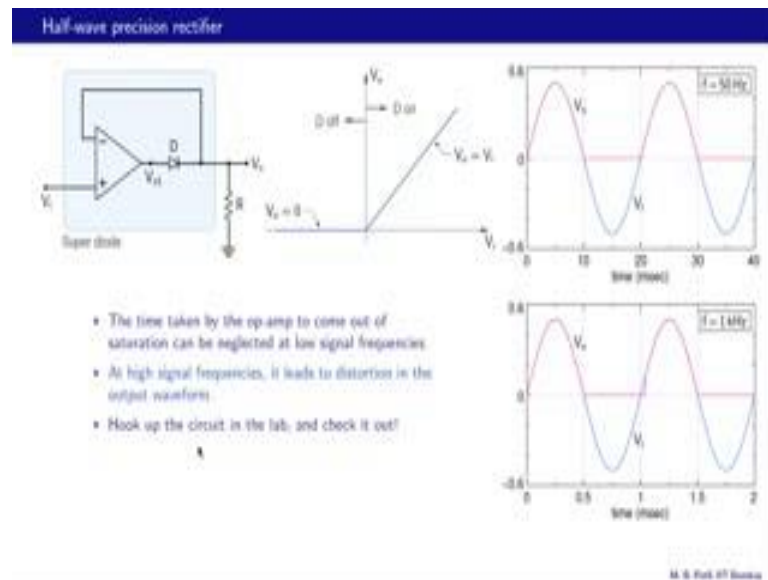
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Let us make a few comments on the super diode circuit. Here are some sample waveforms. This is the input voltage that is the output voltage. And the green one here is  $V_{o1}$  - the op-amp output. Now, when  $V_i$  is greater than 0, the op-amp operation in the linear region as we have seen before, and  $V_{o1}$  is  $V_i + V_{on}$  and when  $V_i$  is greater than zero  $V_{o1}$  and  $V_i$  are the same. So, therefore,  $V_{o1}$  is equal to  $V_i + V_{on}$  as we can see over here. When  $V_i$  is negative, the op-amp operation the open loop configuration and that leads to saturation and  $V_{o1}$  becomes equal to minus  $V_{sat}$  that is what we see over here. So, in this region, the op-amp is operating in the linear region, here it is in saturation region linear region again and so on. So, this transition from negative values of  $V_i$  to positive values of  $V_i$  requires the op-amp to come out of saturation.

For example, here the op-amp is in saturation; here it is in linear region. So, at this point, the op-amp has to come out of saturation and  $V_{o1}$  has to go from minus  $V_{sat}$  to whatever that is. Now, this process is relatively slow and it is limited by the op-amp slew rate. And this is a problem, because this process is slow, and therefore we cannot operate the circuit at higher frequencies. We can look at this sequel file and plot all of these waveforms.

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We have seen that the time taken by the op-amp to come out of saturation is a matter of concern, but if the input frequency is slow then this time is of no consequence, and it can be neglected. Let us take a look at an example of that situation here. Now, input signal frequency is 50 hertz in this case. So, the period is 20 milliseconds and we do not really see any problem, this is our output voltage and it looks like what we would expect. But at high signal frequencies, this time for the op-amp to come out of saturation leads to distortion in the output waveform. Let us see an example of that now.

So, here we have a signal frequency of 1 kilo hertz and we notice that there is a problem at this point. What is happening here,  $V_i$  is going from negative values to positive values, the op-amp is coming out of saturation; and it is taking some time to do that and therefore, we see this problematic waveform here. So, clearly this is not a very desirable situation and should be avoided. And this effect shown here is very real, it can be observed in the lab, and you should definitely hook up the circuit and check it out.

To summarize, we looked at the precision clipper and clamper circuits. We saw that the diode voltage drop  $V_D$  gets effectively eliminated in those circuits. We then looked at the speed limitation of the half-wave rectifier circuit based on the super diode and found that the speed is limited because the op-amp enters the saturation region. In the next lecture, we will look at a half-wave rectifier, which overcomes this limitation. So, see you later.