Basic Electronics
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Lecture – 39
Op-amp nonidealities

Welcome back to Basic Electronics. In out treatment of op-amp circuits so far, we have treated the op-amp as been ideal with more second order effects so to say. A real op-amp shows slight variations from the ideal behaviour; and in this lecture, we will look at two such nonidealities namely offset voltage and bias currents. We will start with the offset voltage, look at its origin, and then learn how to represent the offset voltage with an equivalent circuit model. We will also look at the effect of the offset voltage on the performance of two of the circuits we have studied earlier namely the inverting amplifier and integrator. We will then look at the offset null arrangement in the 741 op-amp. So, let us begin.

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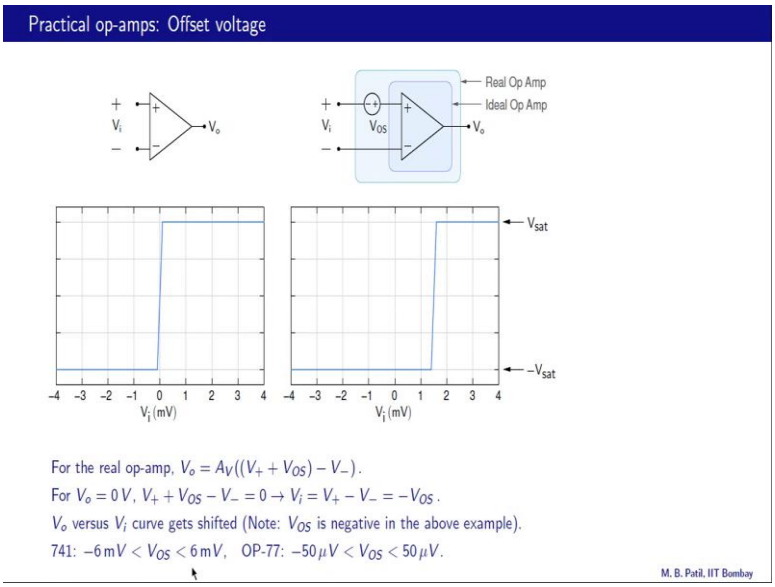

So far we have been talking about ideal op-amps. We now want to look at some of the non idealities in practical op-amps, starting with so called offset voltage. Let us see what that is. Here is an op-amp, and here is the V o versus V R relationship for the op-amp. Note that the scales are different this is millivolts and that will be volts; typically, this would be like minus 10 volts that would be plus 10 volts something of that order. And as

we have seen this part here is the linear region of the op-amp; and this one and this one is the saturation region. And the slope of the V o verses V i curve in the linear region is of course, very high that represents the open loop gain of the op-amp; and for the 741, it is something like hundred thousand.

For an ideal op-amp, the linear region would actually go through 0 0 that means, when V i is 0, V o would also be 0, but that is not what happens in a real or practical op-amp. For a real op-amp, this situation is more likely something like this. And we notice that this linear region is now shifted with respect to 0 by a certain voltage, and this is because of something called the offset voltage. Now, let us see where the offset voltage is coming from, what its origin is and then we will see how to represent it.

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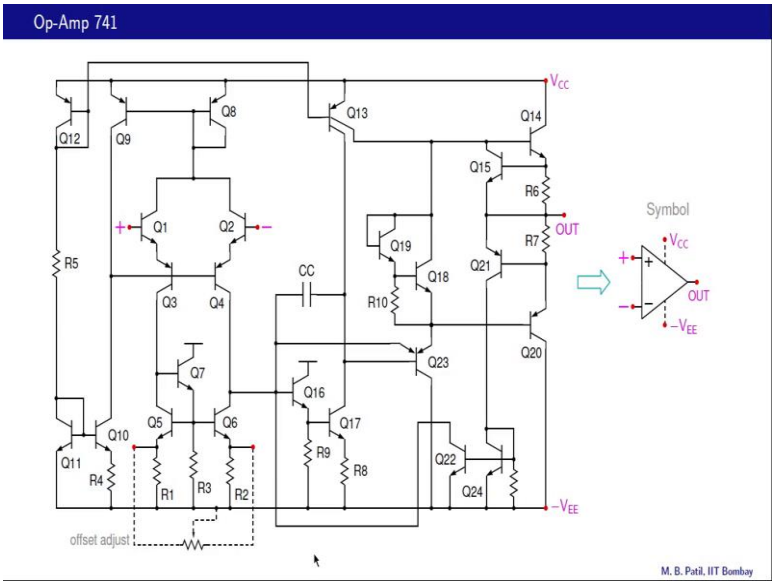

Here is the internal circuit of the 741 op-amp, which we have seen before. This is the non-inverting input terminal that is the inverting input terminal. Now, ideally Q 1 would be the same as Q 2 in all respects, Q 3 and Q four would be the same, and Q 5 and Q 6 also would be the same. And when V plus and V minus are made equal then because of symmetry, the output voltage would be exactly 0. Now, that is not what happens in real life. In reality, the transistors would be close, but not quite identical, and there would be small differences between the two. And therefore, it give rise to the offset voltage that means, the V o versus V i curve gets shifted as we have seen in the last slide.

Let us now see how to represent the effect of this offset voltage. This is out ideal op-amp; this is our real op-amp. Now, in the real op-amp model, we have this box here, which is actually the ideal op-amp. And on top of that, we have this voltage source here. Now, this voltage source represents the effect of this offset voltage is called V os. So, this is the same model as we have been using no offset. And real op-amp is represented by this combined model. We now want to figure out the relationship between this voltage here and V os. So, let us begin with an equation which describes V o in terms of V plus and V minus of the real op-amp. What do we know about V o, we know that V o is A V times the difference between these voltages.

So, what is this voltage, it is V plus of the real op-amp plus V os that quantity. What is this voltage, it is V minus of the real op-amp like that. Now, we want to ask the question for what value of V i - this V i will be O be 0 and that will give us this V i here for which V o is 0. So, all we need to do now is to put V o equal to 0 in this equation then we get V plus plus V os minus V minus equal to 0, this equation here. What is V plus minus V minus that is V i. So, therefore, we get V i plus V os equal to 0 or V i equal to minus V os.

Now, in this particular example, V o is 0, when V i is something like 1.5 millivolts and that is minus V os. So, V os for this particular op-amp is minus 1.5 millivolts. The sign of V os is not so important its magnitude is really what we are concerned about. Let us now look at some typical numbers. For, the 741 the offset voltage is something like 6 millivolts or smaller in magnitude; and for op 77, V os is much smaller 50 microvolts. So, clearly op 77 is much better than 741 in terms of the offset voltage.

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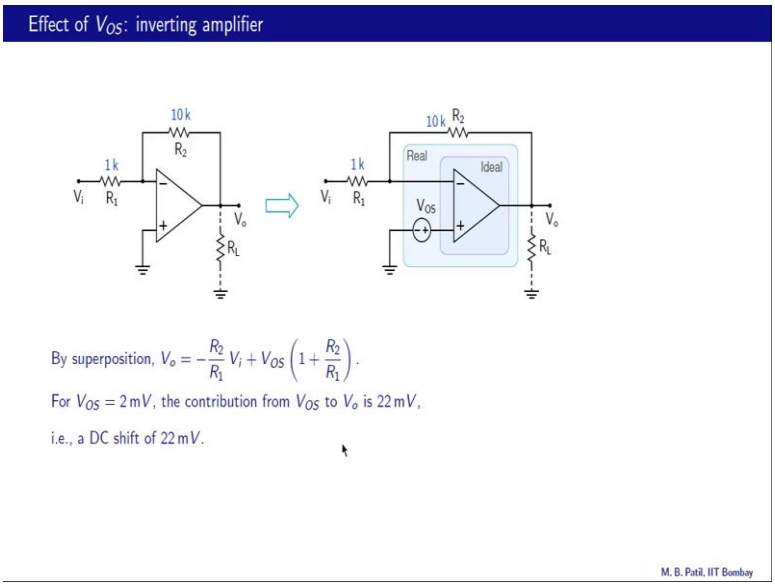

Let us now look at the effect of the offset voltage on an inverting amplifier. Here is an example, R 2 is 10 k, R 1 is 1 k. So, the gain of this amplifier is minus 10 k divided by 1 k that is minus 10. This is our real op-amp now. So, we replace that with the model that we have seen in the last slide; this model here, which consist of this part which is the ideal op-amp with no offset voltage, and the voltage source which represents the offset voltage.

Now, how do we go about finding V o in this case? The easiest way to do is to use support position, because we have two independent voltage sources V i and V os. Note that V os is not really a voltage source in real life but as far as circuit analysis is concerned, we can surely treat it as a voltage source, and therefore we can use super position. So, by superposition, we get two contributions this first contribution is when V os is 0, and V i is kept as it is and that is simply our good old inverting amplifier with the gain of minus R 2 by R 1, so that is the first term.

The second term represents the effect of the offset voltage. So, we keep V os and deactivate V i that means, we ground this and then we see that we have V os here and R 1 is going to ground here. And therefore, the circuit looks just like a non-inverting amplifier and we can use the expression that we derived for the gain of a non-inverting amplifier, and the output voltage would be V os times 1 plus R 2 by R 1.

So, this part here is the contribution from V os. Now, in this case, let us take an example let V os be 2 millivolts, then this would be 2 millivolts times 1 plus 10 k by 1 k, so 1 plus 10 - 11 times millivolts, which is 22 millivolts. So, the output voltage would now show a shift of 22 millivolts because of V os being nonzero.

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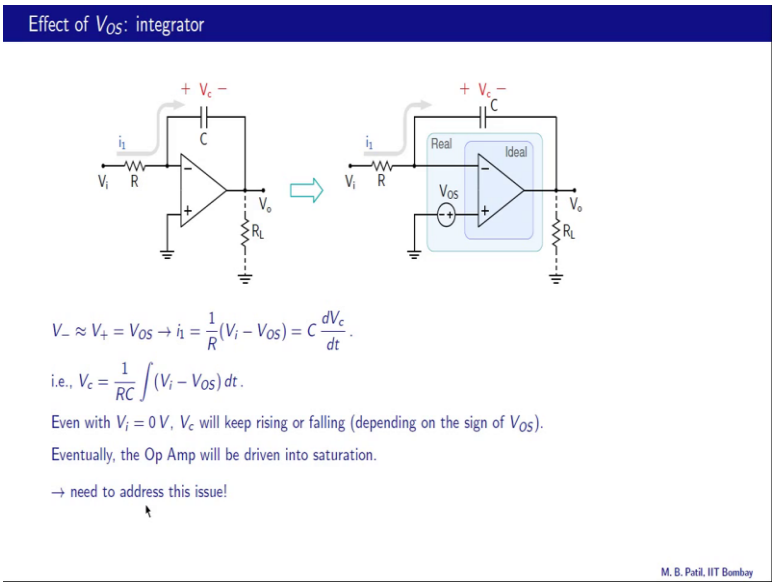

Let us consider an integrator circuit now, and see how it performance is affected by a nonzero offset voltage. Here is a circuit this is a real op-amp with a nonzero V os. So, we replace that with this model here. Once again, this part is the ideal op-amp and the effect of the offset voltage is represented by this voltage source. Now, for the ideal op-amp, we know that V plus and V minus are nearly the same. Since, V plus is V os, V minus is also equal to V os. What does it mean that means, this current R 1 is V i minus V os divided by R that equation; and because the input current of the op-amp is 0 that current will also go through the capacitor and therefore, we can write i 1 equal to C dV c dt and we get this equation here.

In other words, in the capacitor voltage marked here is given by V c equal to 1 over R c integral of V i minus V os dt. And now there is a problem, let us consider the simple case when V i is 0. How do we get them, we get V c equal to 1 over R c integral of minus V os dt, where V os is a constant voltage, however small. Now, because of this relationship what will happen is V c will keep on rising or falling depending of course, on the sign of V os, and eventually the op-amp will be driven into saturation and that is a perfect

disaster we definitely want to avoid that kind of situation. And therefore, we definitely need to address this issue; we need to do something to the integrator circuit, so that this does not happen.

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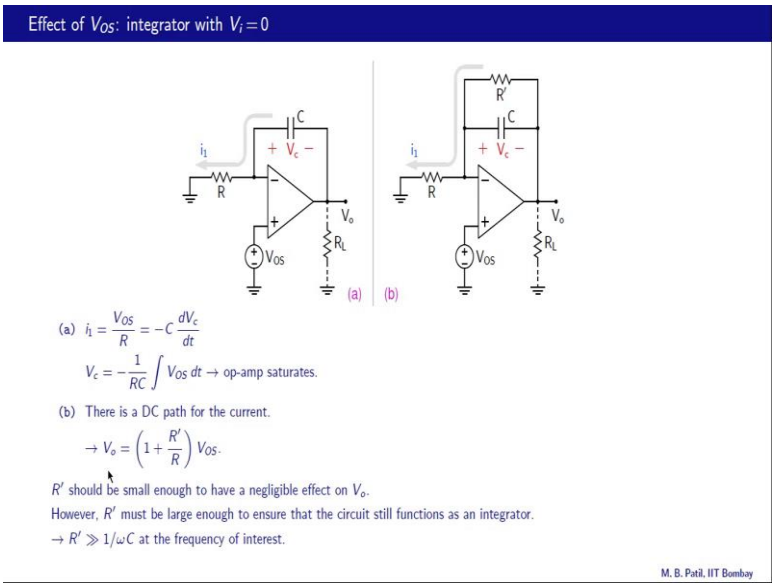

Here is an improved integrator in figure b here. And what is a difference between these two circuits, we have a register R prime connected in parallel with C here and we will see how that helps. What we will do is we will consider both of these circuits our earlier integrator circuit and the improved integrator circuit with V i equal to 0. So, this node which is otherwise equal to V i is grounded in both cases. And now let us see what happens in each of these cases.

Case a, the non-inverting input is at V os. So, therefore, V minus is also equal to V os; i 1 is equal to V os divided by R and therefore, this currents is also equal to V os by R and that current is minus C d Vc dt. So, as we saw before, V c is then minus 1 over R c integral V os dt. Now, this integral will keep rising if V os is positive or it will keep falling if V os is negative, in other case the op-amp will saturate which is something that we definitely do not want.

Let us now look at case b. In this case, there is a DC path for the current, this path here. And in steady state, there is no current through the capacitor it is an open circuit and the circuit looks just like a non-inverting amplifier with input equal to V os. So, therefore, the output is going to be V os times 1 plus R prime divided by R. So, the op-amp would

not saturate. Let us make a few comments on R prime now. R 1 should be small enough to have negligible effect on V o. For example, if we R prime equal to R and V os is 1 millivolt then this entire V o would be 2 millivolts, which may be small enough and we would be probably willing to accept it that is one consideration.

Second - R prime must be large enough to ensure that the circuit still function as an integrator. For example, if we have a square by we applied here instead of grounding it. So, the input voltage V i is actually a square wave then we would accept a triangular wave at the output that is the function of the integrator as we have seen before. And if our R prime is small enough then the functionality of the integrator itself would be disturbed and we certainly do not want that. So, what does it mean in terms of frequency domain, we want the impedance of R prime to be much larger than the impedance of the capacitor which is 1 over omega C in magnitude.

So, at the frequency of interest, we would like to satisfy this condition R prime much greater than 1 over omega C. If you do that then this circuit b will do our job the op-amp will not saturate and what we will see is a DC shift at the output given by this voltage here. So, with the square wave input instead of making V i equal to 0, we apply square wave here. Our output now will still be a triangular wave as we would expect with amplitude which is determined by the component values R and C and the period of the input waveform and the voltage values of the input we form. And in addition, we will only have this small DC shift at the output.

So, our basic functionality is retained and we will only see this additional shift at the output. In some op-amps, there is a provision to nullify or minimize the effect of the offset voltage and that arrangement is called offset null. In the 741 op-amp, for example, these two terminals are brought out as fence 1 and 5 of the IC. And the user is supposed to connect a part between those two terminals with the wiper connected to the power supply minus V EE. To nullify the offset voltage what the user does is to connect the non-inverting input and the inverting input together, let say to ground change this wiper position until V o is made 0 or as small as possible.

Let us try to understand what is happening when we change the wiper position here. What we are doing is connecting in parallel with R 2, some resistance and connecting in parallel with R 1 the remaining resistance of the part. So, essentially we are changing R 1

and R 2 when we change the wiper position and that helps to restore the balance between currents in these two branches eventually reflecting at the output. So, this offset null facility is indeed a very useful facility and it is particularly relevant in applications where we cannot tolerate a DC shifts that result from an offset voltage.

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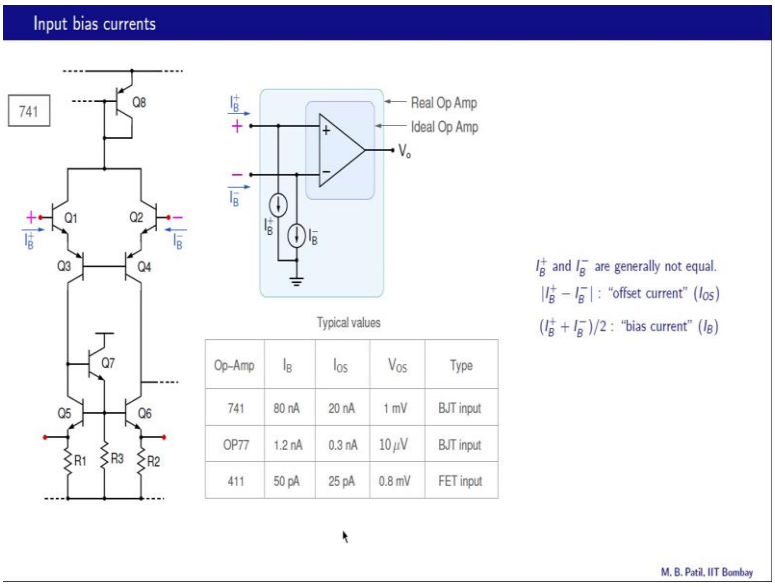

There is another non-ideality that we need to consider for some applications and that is the input biased currents. What do we mean by input bias currents? At the non-inverting terminal, we have this base current going in; at the inverting terminal, we have this base currents going in and these currents are called the input bias currents. Now, when we analysed circuits we said that these currents are small because they are base currents or transistors and they are definitely much smaller than the collector currents. And that would have been ignoring these currents, but they become relevant in some applications.

And let us now see how to represent the effect of these bias currents with a model. So, here is the model that we can use to represent the input bias currents, this is the overall real op-amp which has nonzero input bias currents. This rectangle here is the ideal op-amp, which has no bias currents; and bias currents are external to this ideal op-amp and they are represented by these current sources.

So, what do we see at the non inverting input we see this currents I B plus going in and we also see at the inverting input this I B minus going in. What it means is that this ideal op-amp still has zero input currents; and with this equivalent circuit, we can represent the

effect of the input bias currents and also analyze circuits in a simple manner because we can use all the features of the ideal op-amp in circuit analysis. It turns out that I B plus and I B minus are generally not equal; and with a four defined two additional quantities bias current denoted by I B as the average of I B plus and I B minus; and offset current denoted by I sub os as the difference between I B plus and I B minus.

Let us now look at some typical numbers; for op-amp 741 I B is 80 nano amperes and I os is 20 nano amperes. So, the offset current is surely much smaller than the bias current in this case a factor of 4 smaller. For op 77 I B is 1.2 nano amperes much smaller than I B for 741 and I os is 0.3 nano amperes; op-amp 411 which is a FET input op-amp I B is even smaller only 50 pico amperes where as I os is typically 25 pico amperes. So, there is a wide variety of op-amps available in the market, and we need to make a judicious choice depending on our application.

To summarise, we looked at the meaning of offset voltage of an op-amp and an equivalent circuit to represent it for circuit analysis. Using this model, we looked at how the performance of an inverting amplifier and an integrator is affected by the offset voltage. We found that for the inverting amplifier, offset voltage gives rise to a DC shift at the output; for the integrator, the effect of offset voltage is more series as it causes the op-amp to saturate. We looked at how to correct this situation. We also looked at the offset null arrangement in the 741 op-amp. We have then started with the input bias current of an op-amp. And we will continue with that in the next class. So, see you next time.