Basic Electronics
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Lecture No - 18
Diode circuits (continued)

Welcome back to Basic Electronics. In this class we will continue our discussion of clamper circuits; we will consider a circuit which provides a negative level shift. We will then see how a clamper and a peak detector can be combined to make up a voltage doubler circuit. With the help of the concepts we have learnt we will solve an interesting problem and get further insight into diode circuits. So let us start.

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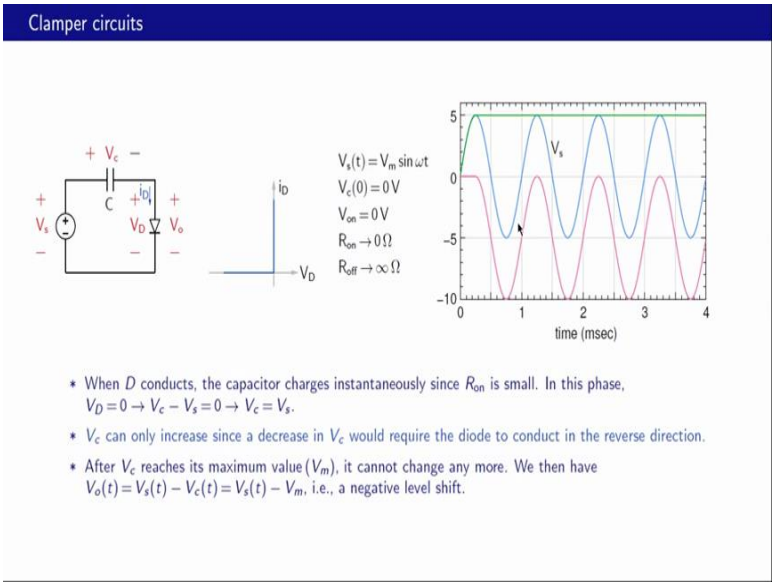

Let us look at another clamper circuit, it is quite similar to the previous one except now the polarity of the diode is reversed and everything else is the same. And first we will consider the ideal diode model with V on equal to 0 volts V s of t is still the same V m sin omega t and V m is 5 volts. So, V s is varying between 5 and minus 5 volts. Note that the polarity of V c is now plus here and minus here.

Once again we will make a few observations and then relate that to the graphs that we will see. First when D conducts the capacitor charges instantaneously, this point is clearly no different than the previous circuit and that is because R on is small and therefore R on times C which is the time constant V is also small. And in this phase V D

is equal to 0, so therefore V c plus 0 minus V s is equal to 0 and therefore we get V c equal to V s. Second point V c can only increase since a decrease in V c would require the diode to conduct in the reverse direction. And this point again is the same as our previous circuit except the polarity of the capacitor voltage and the polarity of the diode are now reversed.

So this point the second point means that we see can go on increasing up to a maximum and then stay constant and that is what this is. After we see reaches its maximum value which comes out to be V m, it cannot change any further and we then have V o of t which is V s minus V c equal to V s minus that constant which is V m; and this a negative level shift. So, V s minus V m, so that is a negative level shift and that is where the circuit is different than the thing is one.

Let us now look at the plots. Now in the beginning other capacitor voltage is 0 and V s starts increasing over there. And since V s comes across the diode and that is a positive bias the diode starts conducting and therefore the capacitor starts charging. And as we have seen the capacitor starts instantaneously, so V c becomes equal to V s. So, V c which is the green line and V s which is the blue line coincide here and the red one is the output voltage and because the diode is conducting in this phase it has 0 volts across it; and therefore the output voltage is 0.

And at this point V c as already reached its maximum and that is V m which is equal to 5. So, subsequently V c is going to stay at that value like that. And then we have this equation to describe V o of t which is V s minus V n. So, if this is V s our V o it is simply a level shifted version of V s. And note that the shift is now downward.

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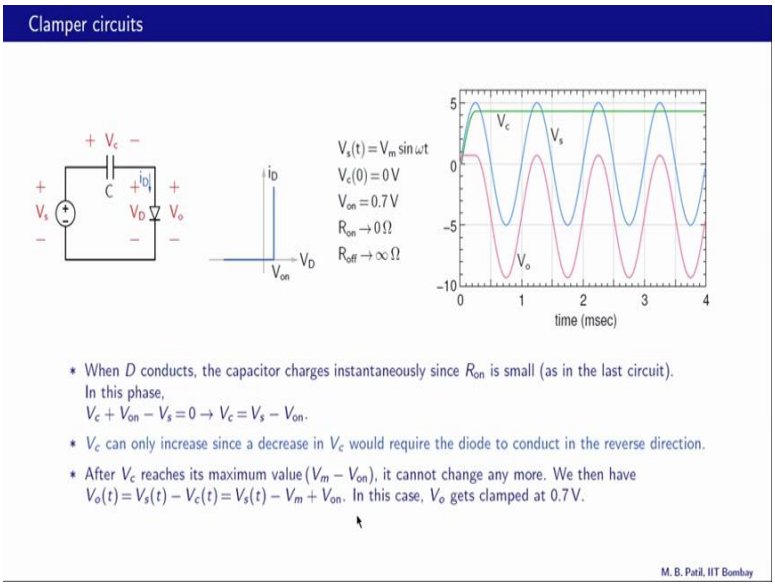

Here is the same circuit as the last slide except we now have beyond of 0.7 volts. Let us quickly go through the results in this case. In the last circuit V c reached a maximum of 5 volts and stayed there, in this case it does not goes to that it goes up to 4.3 volts and stays constant. And let us go through the observations that we went through earlier and relate those to on the graphs.

When D conducts the capacitor charges instantaneously; once again since the time constant is small as in the last circuit and in this phase we have V c plus V on minus V s V c plus V D which is beyond, so the diode is conducting minus V is equal to 0 and that gives us V c equal to V s minus V on. Second point we see can only increase because a decrease would call for the diode to conduct in the reverse direction which is not possible. Third point; after V c reaches its maximum value and what is the maximum value now; what is the maximum value of V s? That is equal to V m which is 5 volts, so the maximum value of V c is V m minus V on which is 5 minus 0.7 which is 4.3.

After V c reaches its maximum value it cannot change anymore for the same reasons we discussed earlier. And we then have V o of t is equal to V s of t minus V c V s minus V c which is V s minus V m plus V r, so it turns out to be V s minus 4.3 volts; earlier this was minus 5 volts and now it is minus 4.3 volts. So, that is really the only difference and in this case the output voltage gets clamped to 0.7 volts; that value there is 0.7 volts and

earlier if you remember it was 0 volts. So, not much difference really except for the small changes because of V on.

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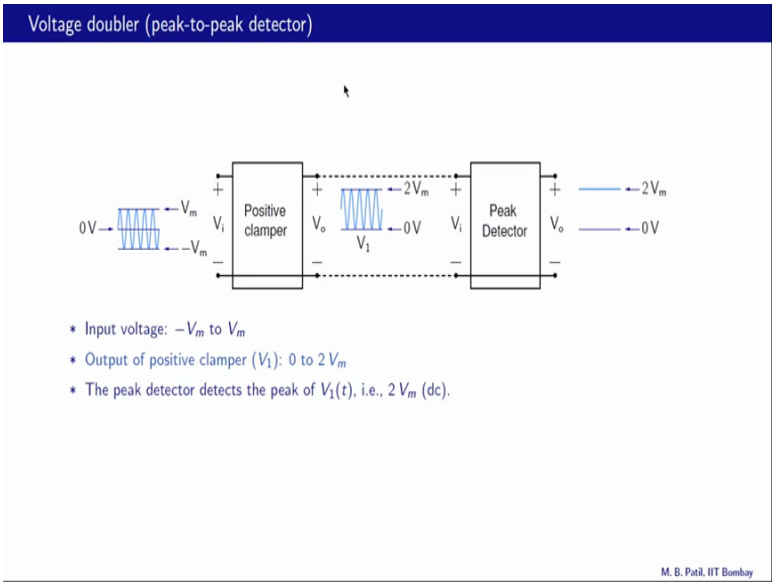

We have seen how clamper works; we have also seen how a peak detector works. We can put these together to make voltage doubler circuit, also called the peak-to-peak detector. So, this figure shows the basic idea behind this combination. The input voltage is a sinusoid from minus V m to plus V m as shown here. The output of the positive clamper that is this circuit which provides a positive level shift is from 0 to 2 V m and it is otherwise identical to the input voltage. So, the input voltage just gets shift and it now goes from 0 volts to 2 V m.

And now the peak detector detects the peak of this voltage; and what is the peak of this voltage? This is 0 this is 2 V m, so the peak of this waveform is 2 V m. So the output of the peak detector is then expected to be a D c voltage of 2 V m. In other words from a sinusoid; going from minus V m to V m we have generated a D c voltage which is double the amplitude, so 2 times V m and that is why this circuit is called this combination is called a voltage doubler.

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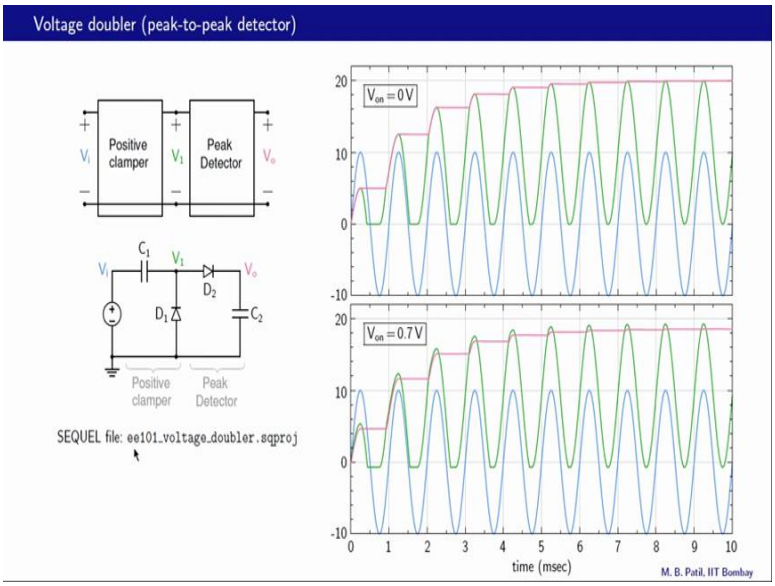

Here is an implementation of the voltage doubler. This first part consisting of C 1 and D 1 is a positive clamper, it provides a positive shift and we have seen this earlier. The second part consisting of D 2 and C 2 is a peak detector and we have also looked at this circuit earlier. And now let us look at the waveforms V i V 1 and V o to see how the circuit works. Here are the waveforms for the case where V on for the diodes is 0 volts that is they have ideal diodes. The blue curve is the input voltage, the green curve is V 1 it is also color coded. So, this blue that is green and output voltage is in the pink color.

And as we have seen before V 1 is just a level shifted version of V i and it is clamped at 0 volts. So, it goes from 0 to 2 V m if the input goes from minus V n to plus V n. The peak detector simply detects the peak of this waveform the green waveform which is V 1 and the peak is this level here and that is 2 times V m or 2 times 10 in this example which is 20 volts.

It is interesting to note that it takes a few cycles for the output voltage to build up to the steady state. In practice of course we are only interested in this part and we really do not care about what happens in the beginning. But if you are curious it is a good idea to plot the diode currents and the capacitor voltages and try to figure out why it is taking so many cycles to reach the steady state. The circuit file for this example it is available and you are encouraged to run the simulations. Now let us look at the case where V on is 0.7 volts; and as we have seen before the positive clamper now clamps V 1 at minus 0.7

volts rather than 0 volts in the earlier case and therefore V 1 does not go to 2 V m while goes to 2 V m minus 0.7 volts. Also the peak detector does not detect the peak of V 1, but its output is the peak of V 1 minus 0.7.

So we have two diode voltage drops involved and therefore the output the pink line here is 2 V m which is 20 volts minus 1.4 volts. And that is a circuit file available to you to run this simulation and look at the various waveforms.

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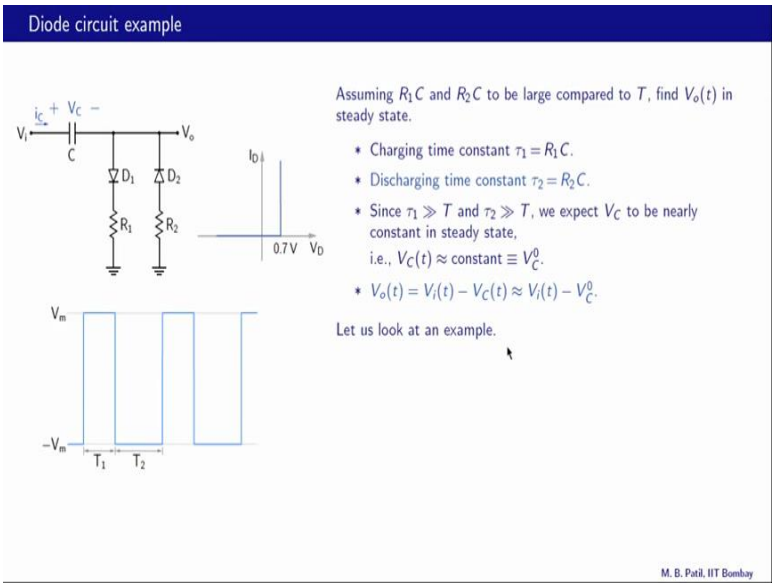

Let us now consider this circuit with two diodes. It is somewhat similar to the clamper circuit that we have seen earlier, the difference is in those circuits we had only one diode here we have two diodes. So, in the clamper circuit the capacitor voltage could only increase because there was no path for the capacitor to discharge. This situation is different we have a charging path for the capacitor through this D 1 and there is also a discharging path for the capacitor through D 2 like that.

Let us look at the problem statement now: here is the input waveform going from minus V m to plus V m this could be say minus 10 volts to plus 10 volts. The high interval; that means, the interval in which the voltage is high is marked as t 1 over here and the low interval is marked as t 2. And the i V relationship for the diode is given over here. So, when the diode conducts it has a voltage drop of 0.7 volts and for any voltage less than 0.7 volts it does not conduct the current is 0. Here is the problem statement assuming R 1

C and R 2 C to be large compared to t find V o of t in steady state: V o is the output voltage here.

What are these quantities R 1 C and R 2 C? Let us look at this circuit; the charging path is like that. So, we see that the charging time constant is the product of R 1 C. So, R 1 C is the charging time constant. What about discharging? The discharging path is like that and therefore R 2 times C is the discharging time constant. This problem does appear to be somewhat complicated, but we have two simplifying factors. One: we are dealing with steady state; that means periodic steady state. And second: these time constants are given to be large compared to t; that means that they are large compared to t 1 and t 2 as well. And this will have implications for our analysis as we will see.

Let us now make a few observations about this circuit and then write equations and figure out what V o of t should be. Charging time constant tau 1 equal to R 1 C as we have already seen; discharging time constant tau 2 is R 2 times C. And since t 1 since tau 1 and tau 2 are both much greater than t the period of the input waveform we expect V c to be nearly constant in steady state. And why is that? What is the meaning of tau 1 much larger than t? So that means, if the capacitor is charging for example, that charging process is going to be very slow; that means in this time the capacitor voltage will hardly change, its going to charge do slowly that we will not even notice the difference in this interval.

Similarly, if the capacitor is discharging we will not really notice any difference in one interval like t 2 because it will discharge so slowly over several cycles. So, because of that we can say that the capacitor voltage in steady state can be treated as a constant. And let us denote that constant by V c with a superscript 0. And now we can get back to V o of t; what is the V o of t? It is V i minus V c, so V o of t is V i of t minus V c of t. And the huge simplification that is made possible by this assumption is that the capacitor voltage is a constant. So therefore, our steady state output voltage it is simply the input voltage minus this constant V c it is superscript 0 the steady state value of the capacitor voltage.

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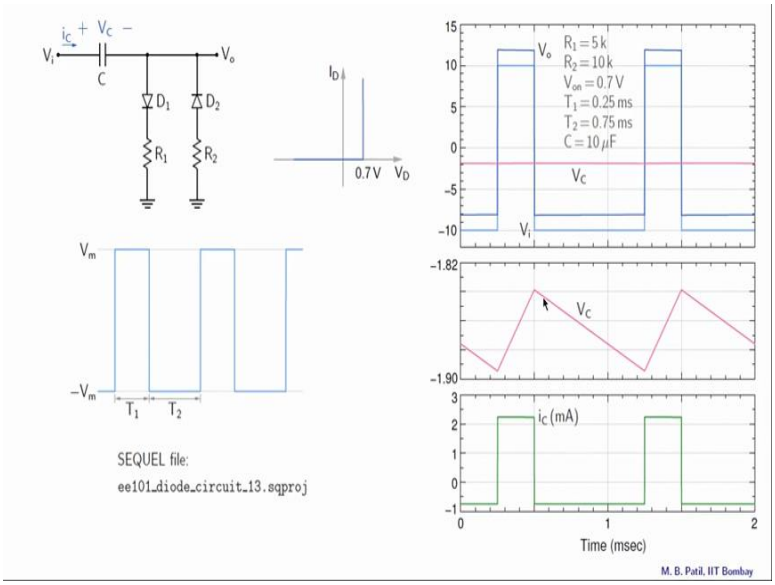

So let us look at an example and verify that these actually happen and then we will derive an expression for V o of t in steady state. Here is an example: the input voltage is going from minus 10 to plus 10; that means, our V m is 10 volts t 1 the interval of high input voltage is given to be 0.25 milliseconds and t 2 the interval of low input voltage is given as 0.75 milliseconds. The other component values are R 1 is equal to 5 k R 2 equal to 10 k; the turn on voltage of the diode is 0.7 volts and the capacitance is 10 micro per heads.

Now let us check whether the condition given in the problem statement that is R 1 C and R 2 C being very large compared to t 1 and t 2 is valid or not. What is R 1 times C 5 k times 10 micro per heads; so that is 50 milliseconds and 50 milliseconds is surely large compared to any of these numbers. What about R 2 times C? 10 k times 10 micro so that means 100 milliseconds and that too is large compared to t 1 and t 2. So, the condition stated in our problem is indeed valid. About the capacitor voltage we said that we expect V c to be approximately constant and that is observed over here and what is that value this is 0 volts this is minus 5, so V c is about minus 3 volts.

Now to proceed further let us look at V c in an expanded form. Here is the capacitor voltage as a function of time, and we see that it is nearly constant but not exactly constant it varies between about minus 1.9 volts 2 minus 1.84 volts. And during this interval and the input voltage is high, the capacitor voltage rises and that corresponds to

charging of the capacitor through D 1. During this interval in which the input voltage is low the capacitor voltage decreases and that corresponds to discharging of the capacitor through D 2. And you note that our capacitor voltage waveform is periodic, this value is the same as the V c value after one period that is this one; and that is the meaning of periodic steady state.

Let us now look at the capacitor current that is what it looks like. And notice that it is consistent with our comments so for about the charging and discharging of the capacitor. During this interval when the capacitor is charging i c is positive and during this interval and the capacitor is discharging i c is negative. Let us try to understand why there is a charging phase and a discharging phase in the first place. So, let us consider this situation in which V i is constant equal to plus V m, so we do not have these changes we just have a constant V m as the input voltage; just a D c voltage.

And what do you expect to happen? Initially there will be a capacitor current, but as t tends to infinity as we approach the steady state all voltages will become constant, so therefore V c will become constant C D V C D t which is i c will become 0 and the capacitor will look like an open circuit. There would not be any voltage drop over there and the entire input voltage V m would then appear across the capacitor.

So this end of the capacitor would be at V m and this other end of the capacitor would be at 0. In other words V c would have become equal to V m, so that is exactly what is happening in the charging phase. So, the capacitor voltage is trying to go all the way up to plus V m in this case; of course, it does not quite happen because we then have this transition of the input voltage. And so therefore the discharging starts.

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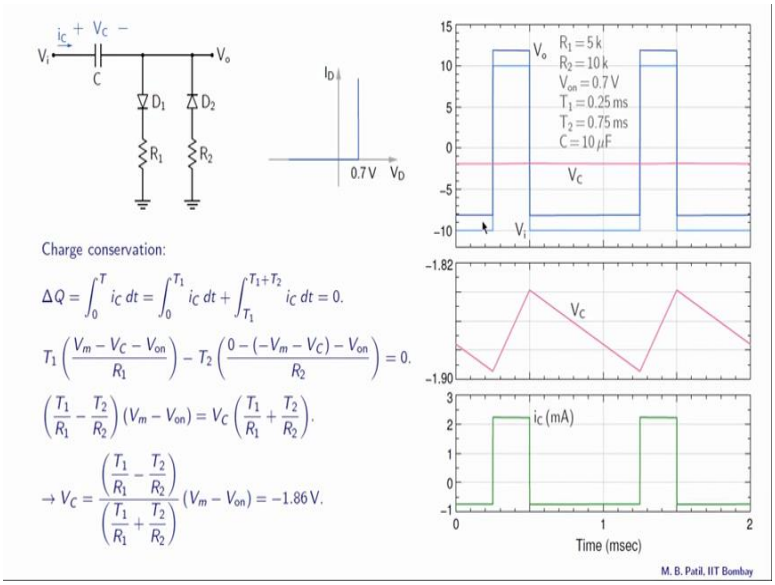

Now, we want to find the value of V c approximately assuming it is nearly a constant. And for that purpose we will use charge conservation, we have come across this concept also when we discussed R c circuits. And it has to do with periodic steady state; and what the situation we have here is periodic steady state everything is periodic V c, i c, V on, V o.

In particular the charge on the capacitor is also periodic and we are going to use that to figure out what V c should be. So, what is the charge the change in the charge on the capacitor in one period it is 0 to t i c D t that is because i c is D q D t. And this we can split into two parts: integral over 0 to t 1 this phase and integral from t 1 to t 1 plus t 2 that is this phase. And these two together should add up to 0 because we do not expect any change in the capacitor charge between 0 and t equal to capital T.

And we can see in this figure that it is actually happening this area which is the first integral is positive, because this is our 0. And the second integral is this area and that is negative, it turns out that they are equal in magnitude and opposite in sin so they add up to 0. Next what is i c in this interval? It is V m minus V c this is plus V m minus V c and minus V on the voltage drop across R 1 and that divided by R 1 that is over i c that is because the charging path is like that and that is a constant; merely a constant because V c is nearly a constant.

Therefore, the integral is simply that constant multiplied by t 1, so that is what this term says. What about i c in the discharging phase that current? Let us find the voltage drop across R 2 in the discharging phase and that will give us the current that V R looking for. So, let us see what this node voltage is: first this is minus V m and the capacitor is discharging, so minus V m minus V c so this node is at minus V m minus V c. So, the voltage drop between these two nodes is 0 minus minus V m minus V c that is this entire voltage drop here and from that we need to subtract the voltage drop across the diode D 2 which is V on.

So that is what we have done over here. So, that gives us the voltage drop across R 2 and that divided by R 2 will give us the correct. Now it is a simple matter of solving this equation for V c. Let us take V c on one side and we get t 1 by R 1 plus t 2 by R 2 times V c here and everything else on the other side. And that gives us the value of V c. And for this example with the numbers given here V c turns out to be minus 1.86 volts. And of course, it agrees well with our simulation results. Once we know V c we know V o as well because V o is simply V i minus V c. So, V o is going to be V i minus minus 1.86 volts, so V i plus 1.86 volts. So, that is a positive shift of V i. So, this is our V i w right looper and V o is the same as V i except for a positive shift of 1.86 volts.

In summary we have seen how a voltage doubler works. They have also considered an interesting diode circuit which could be analyzed using the concepts involved in the clamper and peak detector circuits. In the next class we will see how diodes can be used in rectification; that is convergence of an AC voltage to a DC voltage; until then goodbye.