Basic Electronics
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Lecture - 17
Diode circuits (continued)

Welcome back to Basic Electronics. In this lecture we will look at diode circuits involving a capacitor. As we will see the presence of a capacitor adds a new dimension and we will see how to analyze some of these circuits. We will first look at the peak detector circuit we will then consider a clamper or a level shifter circuit in which the output waveform is a level shifted version of the input waveform. So, let us begin.

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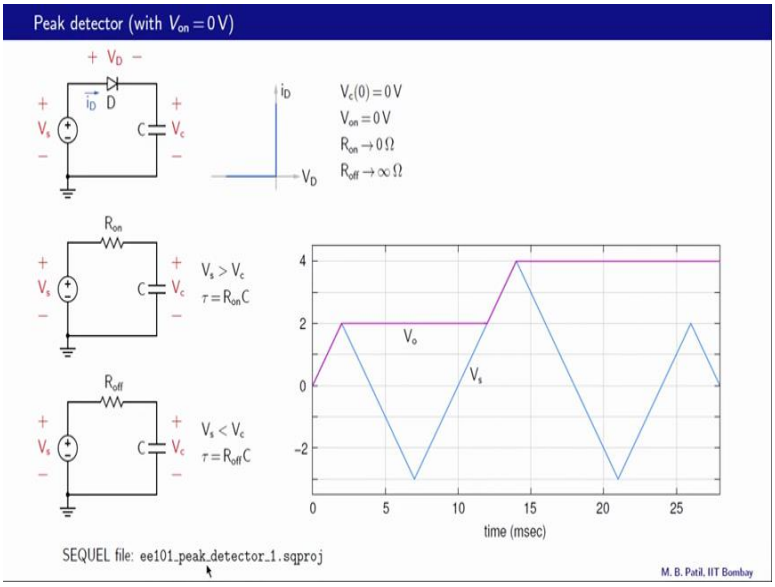

Let us consider this circuit with a diode and capacitor; the configuration is fairly simple just these two connected in series, but it is very different than the circuits we have considered so far which had diodes and resistors. And let us take a look at in what way the circuit with a capacitor is very different than a circuit with diodes and resistors.

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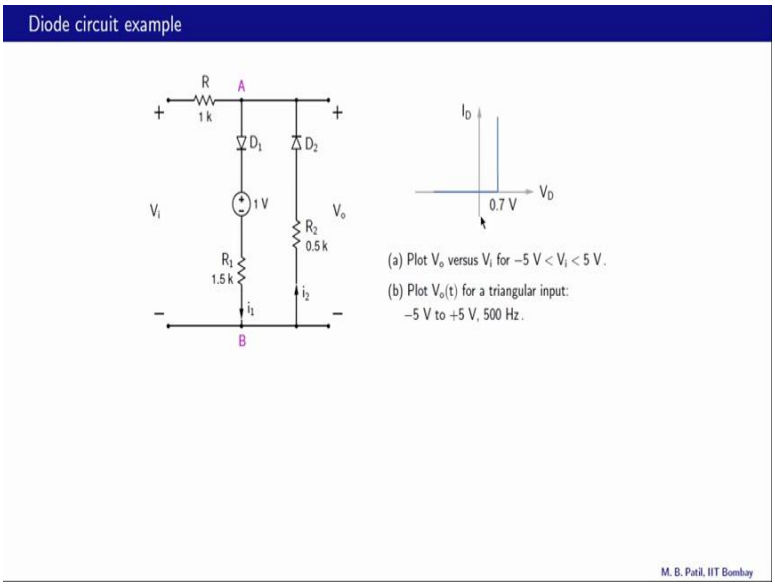

For example here is a diode circuit which we looked at earlier. Now for this circuit in principle it was possible to take some value of V i figure out whether for that input voltage the diode D 1 was conducting or not conducting, whether the diode D 2 was conducting or not conducting. And then solve the KCL, KVL equations to figure out what the output voltage would be. And, in fact we could consider not just one V i value but a whole range of V i value for which the diode D 1 was on and D 2 was off for example. And then figure out what V o versus V i would be for that particular range of values.

Once we had considered all the possible cases then we could plot V o versus V i for this given input range. And having obtained this information we could then proceed with plotting V o as a function of time for a given triangular input. And this was possible because all elements here are static; for example, for the resistor we have V equal to R times i static relationship. For this voltage source we have V equal to 1 volt that is constant, again a static relationship. For this diode we have i versus V as given by this graph, again a static relationship there is no time anywhere. And there was no dynamic element such as a capacitor. So, when the capacitor is included things become different and that is what we will look at in the next slide.

Coming back to our original circuit we see that there is this capacitor which now introduces dynamic behavior in the circuit, because the capacitor current i c is C D V c D

t; that is not a static relationships like we equal to i R, it is dynamic because the current the capacitor current depends not only on the present value of V c, but also on what happened in the past because it depends on the rate of change of V c. So, that is the complication and we therefore need to consider how the capacitor is charging or discharging when we look at circuits like this which have capacitors.

So, let us get started with this particular example. We will assume that the diode is ideal it has a non voltage of 0 volts. The capacitor voltage V c is initially given to be 0, the input voltage given by this graph is applied and we want to find V o as a function of time. And we assume that the diode is ideal, it is on resistance is 0 and off resistance is infinite.

Let us redraw this circuit for two situations: one the diode is conducting, so its resistance its R on, second diode is not conducting and its resistances are R off. R on is very small R off is very large. So, let us look at the situation at t equal to 0, we have the input voltage equal to 0 the output voltage which is the same as the capacitor voltage also equal to 0. So, the p end of the diode is at 0 volts the n end is also at 0 volts; that is the situation at t equal to 0.

Now, the input voltage starts rising; the capacitor voltage is 0 volts at the beginning, so this n end of the diode is at 0 volts. And now this voltage is going up as the input voltage increases. So, the diode turns on starts conducting and we have this circuit now coming into the picture. So, the capacitor starts charging through the diode. And what is the time constant for this process? It is R on times c, which is very small because R on is a very small resistance ideally 0. So, the time constant for the charging process is a very very small time and much smaller than any of these times that we see in this graph.

In other words the charging process is going to be instantaneous, so the capacitor voltage is simply going to follow the input voltage. And that is what we show over here in the pink color. Beyond this point what happens? Now the capacitor voltage has reached 2 volts and the input voltage has started dropping. So, the n end of the diode is 2 volts and the p end is now going below 2 volts as a result the diode is now under reverse bias and we are operating somewhere in this region. So, the current is 0, the diode is replaced by resistance R off which is very large ideally infinite and if the current is 0 then the capacitor voltage cannot change. So, the capacitor voltage becomes constant at 2 volts

like that. And that continues right up to this point, because throughout this interval the p end of the diode is lower than the n end which is that 2 volts.

Now the input voltage starts rising above 2 volts and once again by the same logic. The capacitor starts charging and the charging process being instantaneous because of this very small time constant, the capacitor voltage will once again simply follow the input voltage like that. At this point again the input voltage becomes slower than the capacitor voltage and the capacitor voltage becomes constant.

So, this circuit is actually detecting the peak of the input voltage: one peak here other peak here, so the capacitor voltage becomes constant and the constant value is the peak of the input waveform, the last peak of the input waveform. That is why this circuit is called the peak detector. And the circuit file is available you can run this simulation and look at these results.

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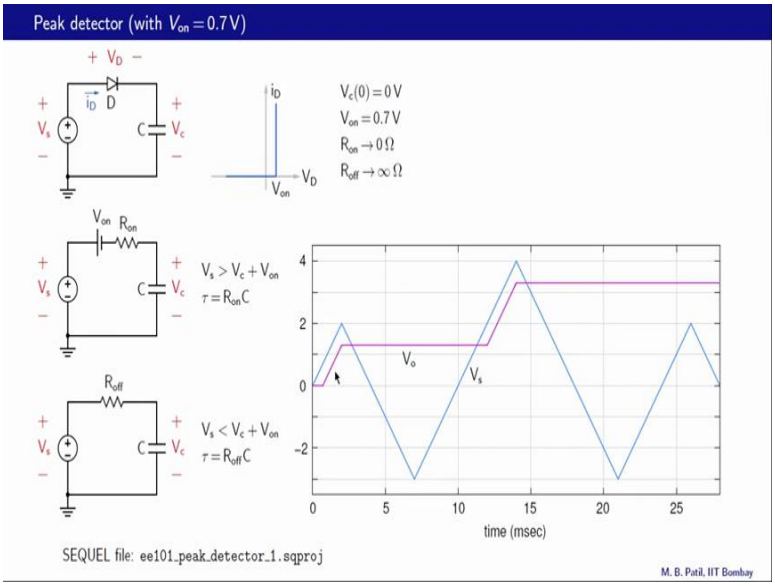

Let us consider the same circuit once again, but with a more realistic diode model with V o equal to 0.7 volts and otherwise ideal that is with R on equal to 0 and R off equal to infinity.

So, these are the equivalent circuits when the diode is conducting- we replace it with a battery or a voltage source, V on that is 0.7 volts, in series with R on. And when the diode is not conducting we replace it with R off large resistance. What is the condition

for the diode to conduct its p end, the voltage at its p end must be greater than the voltage at its n end by V on or 0.7 volts. That means, V s must be greater than V c by 0.7 volts and that is what it says here V s must be greater than V c plus V on.

And in that case this equivalent circuit applies, and as seen from the capacitor the even in resistance is R on and therefore the time constant is R on times c. And as we have seen before this is a very small time, because R on is a very small resistance ideally 0. And if V s is less than V c plus V on then the diode does not conduct and we have then this circuit representing the original circuit, and tau is R off times c and since R off is very large ideally infinite, tau is infinite.

Let us start at t equal to 0 we have the capacitor voltage equal to 0, and the input voltage also equal to 0, and now the input voltage starts rising. But unless the input voltage becomes equal to 0.7 volts the diode cannot conduct, and therefore the capacitor voltage remains at 0 volts. So, let us see that part of the plot there. So, that is this part here. And now when V i or V s becomes 0.7 volts at that time the capacitor voltage would simply follow the input voltage; why because the time constant for that process is very small ideally 0.

But it will follow the input voltage with a difference of 0.7 volts, because this voltage here is not V s but V s minus V on and that is this straight line here. What happens after this? After this the input voltage starts decreasing and the difference between this end and that end which is V D becomes less than 0.7 volts and therefore the capacitor voltage cannot change we are now in this situation and becomes a constant. At this time the difference between V s and the output voltage V c becomes 0.7 volts and the diode once again starts conducting. We have this equivalent circuit and once again the capacitor voltage starts following the input voltage with a difference of V on like that.

Now, at this point the input voltage V a starts decreasing, and therefore V D becomes less than 0.7 volts the diode stops conducting, and we have this situation. And there is no way the capacitor voltage can change anymore, because the current here is 0. And that is what we have here. So, the output voltage in this case is quite similar to our previous example where V on was 0 except for this difference between V s and V o.

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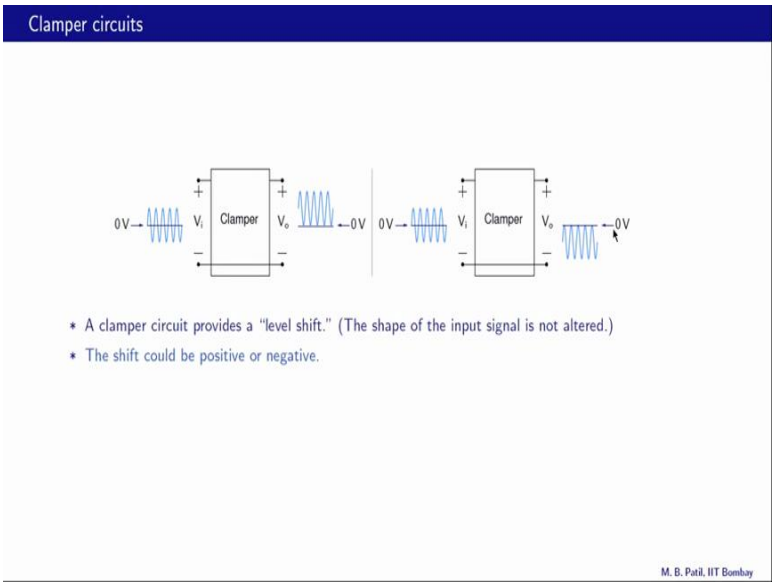

Let us look at another application, and that is called the clamper. We have an input voltage here going from minus V m to plus V m; for example this could be minus 10 volts this could be plus 10 volts centered around 0 volts.

When we pass this input voltage through this circuit called clamper what we get at the output is a level shifted version of the input waveform. So, this input waveform has got shifted up and now the lowest value of this output voltage is 0 volts. In other words the output voltage has got clamped at 0 volts and that is why this circuit is called a clamper. So, clamper circuit provides a level shift. And note that the shape of the input signal is not altered. So, if this is sinusoid the is also a sinusoid, if this is 20 volts peak to peak this would also be 20 volts peak to peak and so on.

Now, this shift that we are talking about could be positive or negative. In this circuit it has been positive, because in our input voltage the lowest value was negative now the lowest value is 0 volts. Here is a clamper which provides a negative shift. So, this is our input voltage as before and now this entire waveform has got shifted down to give us the output voltage, and the output voltage is now clamped at 0 volts but the level shift has been negative.

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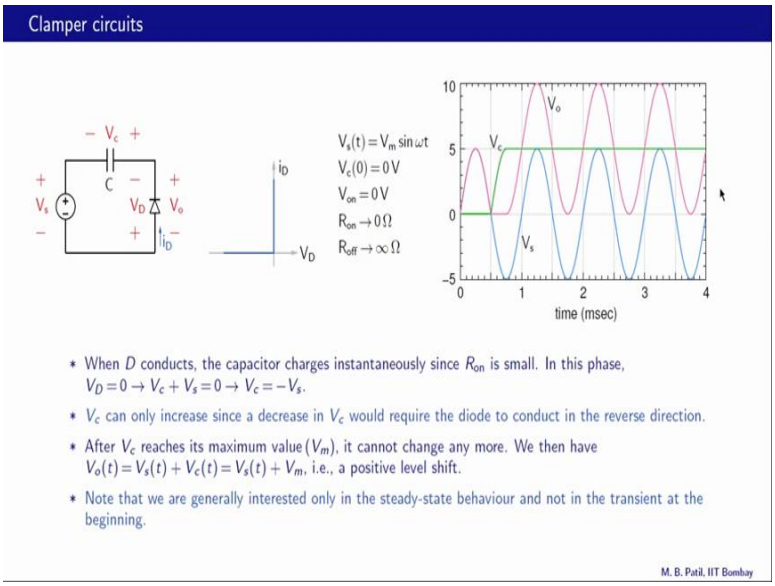

Here is an implementation of the clamper circuit very simple just a diode and capacitor in series. And for simplicity let us assume this ideal i V curve for the diode with V on equal to 0 volts R on equal to 0 R off equal to infinity. The input voltage is shown here in blue; its V m sine omega t V m is 5 volts, so the input voltage goes from 5 to minus 5 and as we shall see the output voltage is a clamped version of the input voltage.

Let us understand the operation of this circuit now. What we will do is make a few observations first and then look at the implications of those observations. First when D conducts the capacitor charges instantaneously since R on is small; that means, time constant which is R on times e is small. And in this phase V D is 0 this voltage is 0 because we have V on equal to 0 volts. And what does that mean? That means, V c plus V s should be equal to 0 because there is no voltage drop across the diode and that tells us that V c would be equal to minus V s in this phase when the diode is conducting.

Second observation V c can only increase; note that V c is marked as plus here and minus here so the capacitor current is the same as the diode current; and since the diode current can only be positive V c can only increase. And that is because a decrease in V c would require the diode to conduct in the reverse direction which is not possible.

Third observation after V c reaches its maximum value which turns out to be V m and we will see that in the plot. After that point it cannot change anymore, why? Because it cannot decrease for this reason and so it cannot change. We then have V o of t equal to V

s of t plus V c of t and this is simply coming from KBL V o of t let us go like this V o of t minus V s of t minus V c of t equal to 0. Therefore, we have this equation.

And now since V c has become a constant we can say that V o of t is V s of t plus that constant and that constant turns out to be V m which is the amplitude of the input voltage. So, what does it mean? It means that the output voltage is a shifted version of the input voltage and the shift is given by this constant here which is positive. So, we have got a positive level shift in this case. At t equal to 0 the capacitor voltage is 0 and now the input voltage starts rising.

Let us see what happens as a result of that; with V c equal to 0 this V D is the same as minus V s because of these opposing polarities. Now, if V s becomes positive; that means, V D is becoming negative therefore, the diode does not conduct the current in the circuit is 0 and the capacitor voltage cannot change. So, it remains at 0 volts. What about the output voltage? In this interval the output voltage is the same as V s because its capacitor voltage is 0 volts, and that is the situation up to this point here.

The green curve here is the capacitor voltage it has remained at 0 and the red one is the output voltage. And as we have seen the output voltage and the input voltage are identical because the capacitor voltage is 0 up to this point. Now what happens? Now the input voltage becomes negative, so the n end of the diode is now negative with respect with the p end and therefore the diode conducts.

What happens when the diode conducts? We already have figured that out. So, V c becomes equal to minus V s because of this negligibly small time constant of the circuit and that is seen over here. So, this is V c and that is equal to minus V s this is our V s or if V s is going negative V c equals positive. What about the output voltage during this interval? Now the diode is conducting in this interval and therefore there is no voltage drop across the diode and output voltage is 0 and that is what we see over here. And now we note that the highest value that we see can acquire is the negative of the lowest value of V s the input voltage and it has already achieved that. So, if this is minus V n equal to minus 5 volts the capacitor voltage is plus V m or plus 5 volts.

So now, the third point after V c reaches its maximum value V n it cannot change anymore, because any change would now require the capacitor the diode to conduct in

the negative direction which it cannot do. Therefore, the capacitor voltage now becomes constant and then we have V o of t equal to V s of t plus V m; let us see that in the graph.

Now the capacitor voltage has become a constant equal to plus V m and this is our level shifted output. So, our input is from minus 5 to 5 and output is from 0 to 10 volts. So, it is identical to the input except for a level shift of plus V m. Before we leave this example we should make a comment; and that is we are generally interested only in the steady state behavior of this circuit so that means, this part here. And we have really discussed all of this only to understand the circuit better, but in practice we really do not care about what exactly happens over there.

And in fact, if you go to the lab and hook up this circuit and watch the waveforms on the oscilloscope we will not even see this part because by the time you connect everything start your function generator and oscilloscopes and so on all the transients would have died out and you will only see the steady state picture and that is what we are also interested in.

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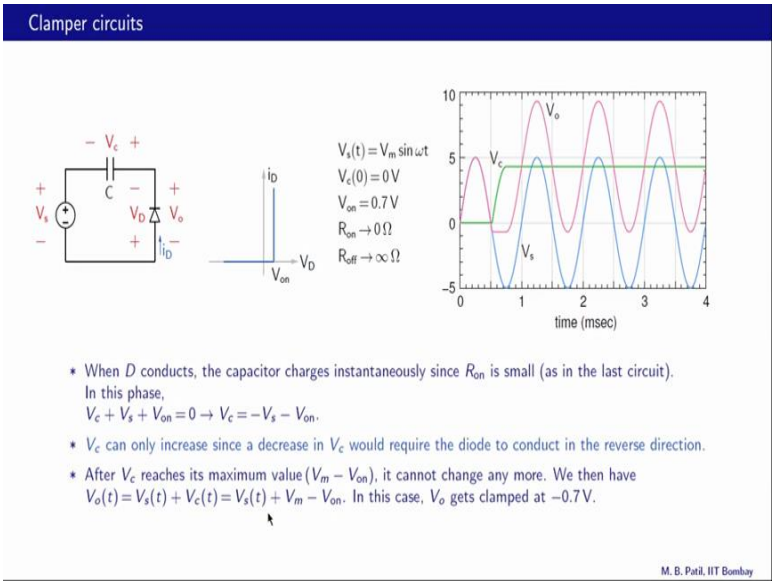

Let us now consider the same circuit, but with a more realistic diode model that is with V on equal to 0.7 volts. And here are the capacitor voltages and output voltage waveforms. We notice that they are qualitatively quite similar to what we saw in the last slide. So, let us try to understand the small difference that we see between these plots and the previous ones.

Once again let us make a few observations and then we will relate these observations to the actual plots. First when D conducts the capacitor charges instantaneously and that is definitely true because our R on is still small 0 ideally, and therefore the time constant is small and that is no different from the last circuit we considered. And in this phase we can say that we V c plus V s plus V on is equal to 0 that simple KBL V c plus V s plus V D which is V on equal to 0. And that tells us that V c must be equal to minus V s minus V on.

Second point and once again it is similar to what we saw in the last slide. V c can only increase since a decrease in V c would require the diode to conduct in the reverse direction which is not possible. So therefore, this voltage V c can only go on increasing once it reaches a maximum value it cannot change any more. And that is the third point after V c reaches its maximum value. In this case what is the maximum value? That depends on what is the minimum value of V s here. What is the minimum value of V s? The minimum value of V s is minus V m which is minus 5 volts. So, minus V s is plus V m at this instant, and therefore V c reaches its maximum value which is V n minus V on and after that it cannot change anymore.

So, we then have V o equal to V s plus V c as before V o is V s plus V c and that is V s plus V m minus V on. In the earlier slide we had these V o equal to V s plus V m and this V on was not there. So, that is clearly the only difference and we observe that over here. So, instead of reaching 10 volts V o reaches now 10 minus 0.7. So, that is V s of t plus 5 minus 0.7; so V s of t plus 4.3. And since V s of t has a maximum value of five we have 5 plus 4.3 which is 9.3 volts. And in this case V o gets clamped at minus 0.7 volts as we can see in this plot here. So, the lowest value of V o in the earlier case was 0 volts and now it is minus V on which is minus 0.7 volts.

To conclude we have looked at two new diode applications in this lecture: peak detector and clamper. We have seen that the analysis of these circuits is very different from the diode circuits we have seen earlier, and therefore they have added a new dimension to our understanding. That is all for now, see you in the next class.