Fabrication of Silicon VLSI Circuits using the MOS technology
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Lecture 06
Diffusion

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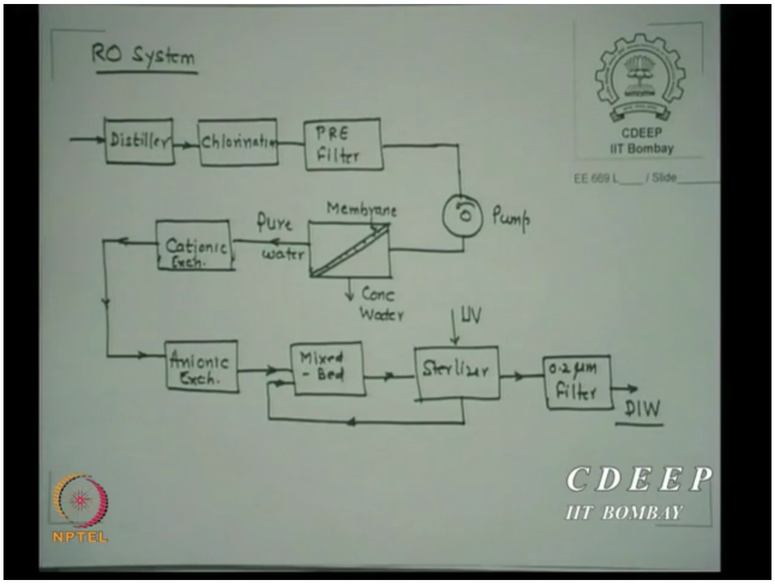

For the last lecture we fuel two transparencies or two foils were not shown, so first I will show them and then start the process of diffusion. As I said water is the major reagent for us in the VLSI lab and we need a very highly pure water and I other day calculated the water resistivity is one of the quality marker which is around 18 mega ohm centimeter. Here is typical reverse osmosis system which is installed in every VLSI fab lab which creates this DIW which is called deionized water, DIW.

What we do is we had a distiller in which water is first boiled and then the wafers are collected. And then this water which is now after distillation there relatively pure water is available, is then added some chlorine compounds and they, that is called chlorination. And once it passes through chlorination, much of the bacterias are actually killed here. Chlorine is a very strong oxidizing agent, chlorination is very strong process in which most of the bacterias are actually removed. At least they are killed if they are not removed.

Once this slightly better bio-water is available, we pass it through a pre-filter which is a standard filter. It actually stops much of the high sized particles, maybe around 0.5 micron and above. This is called pre-filter. Then there is a pump followed by RO system, this is my RO system. Now please remember many of you might not have done a course anytime in chemistry or chemical so seriously but we use that very often, is called reverse osmosis. Why this word reverse?

Osmosis is a process which says if you have a concentrated solution and if you have a dilute solution on the other side of the membrane, then according to because of the osmotic pressures on the membrane, the water from lighter side actually go towards concentrated side to dilute it. Water moves from lighter concentration or pure water will go to the (sol) which is already concentrated to dilute it out.

That is the process of osmosis. However what we really want, the other way, I want water which is already concentrated. I want to get little lighter water or purer water, so I pass through membrane and since membrane will actually do the opposite process which is called osmosis we pump it from the other side and force reverse osmosis process. All home these days have this RO system, so it is exactly is there.

You have to clean this membrane every three months and every one year you have to change as well. So what happens? This so called good bio-water clean, removed many particles. Much of this pre-filter also has carbon filter which is called charcoal, ignited charcoals. And they actually absorb some other kinds of bio-impurities as well. Once this water which is concentrated here with the impurities passes through membrane, you get a lighter water which is purer, without impurities. This is why we say it is a reverse osmosis.

Once you get pure water out of this membrane, then we actually pass through a resin, a huge bunch of cylindrical tubes are there, big ones through which water is pushed from below and comes from the top side. And this whole container contains a resin and that resin has a property that it is cationic in nature which means it will remove sodium, potassium. Many of these first order compounds or elements will be actually removed as OH ions with OH ions. Once much of the NaOH or KOH or soluble such are removed, they actually are absorbed in the resins and the still purer water without those elements actually come out of cationic resin. This cationic resin water, then is passed through anionic exchanger which is another resin.

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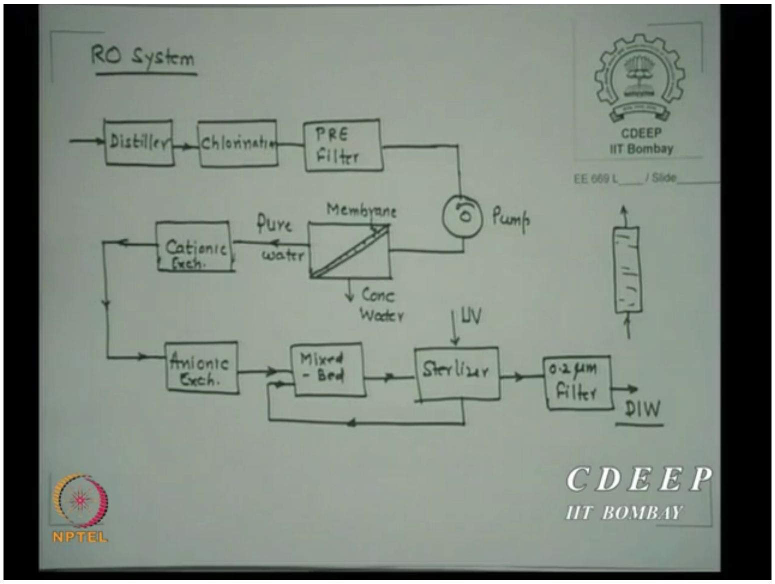

And please remember the way it is always pushed is something like if this is your cylinder which contains resin, the water is pushed from here and taken from here. When this water enters, it starts reacting with the resin and much of the hard impurities like metal impurities like copper, gold, strontium, calcium, magnesium, all are then are removed in this process. And the water which comes out of anionic exchange and they are retained in the resin itself.

And the pure water comes up and then it passed through a mixed bed column. The mixed bed column is actually a mixture of cationic and anionic exchanges, 50-50. There are two mix bed columns kept, one anionic first, cationic second. The second one is cationic first, and you actually pass through both of them so that whatever traces of those other impurities would have left out of this exchange and this exchange can still be taken out in the sand or the resin and much pure water is available out of this.

Please remember since we are removing ions, other day I said we are looking for 18 mega ohm centimeter resistivity of water which essentially means it is deprived of H, OH ions itself and they form only H2O. There are no ions possible because ions means conductivity will actually increase and therefore resistivity will decrease. So we wish to see that purer water, so the taste of, of course there is electrolyte cell which I have not shown which, actually water can pass through it and show how, I think it is normally displayed these days, how much resistivity water you are getting.

Now further for anything biased things are still coming out, are then we actually shine ultra-violet light and it gives most of the bacterias. Some companies have another filter here called DI-earth, earth-atomic filter which actually removes bio-materials. So companies do not have. And after that filter, we have a very fine filter, 0.2 micron or lower, part filter which is a small membrane, this is what is it called, polypropylene films, run-over which have grills, grids on that.

And most of these all particles of larger than 0.2 or even lower are actually removed in this final filter. And the water which you receive then is deionized water, highly pure, no contaminant. Because please remember why we are worried about, because water is going to be used after every step what I do and therefore it should not have any ions of its choice because at the end I am going to introduce very small amount of impurities of my choice.

If the concentration is already changed something else, then I do not know what impurities I am adding because they will be actually sitting into many association sites. So worry is that water has to be highly pure. So this is a typical RO system. Earlier we did not have RO, we have normal like Aquaguard also and other companies have without RO systems. In this there is additional feature because it purifies much more. Membranes are very, very strong concentration gradient changer.

So we use that, however as I say membrane is, it is a bio-material and has to be always clean. And therefore you need much more cleaner water to clean the membrane. So there is difficulty in all this but anyway this is how the waters are actually cleaned up.

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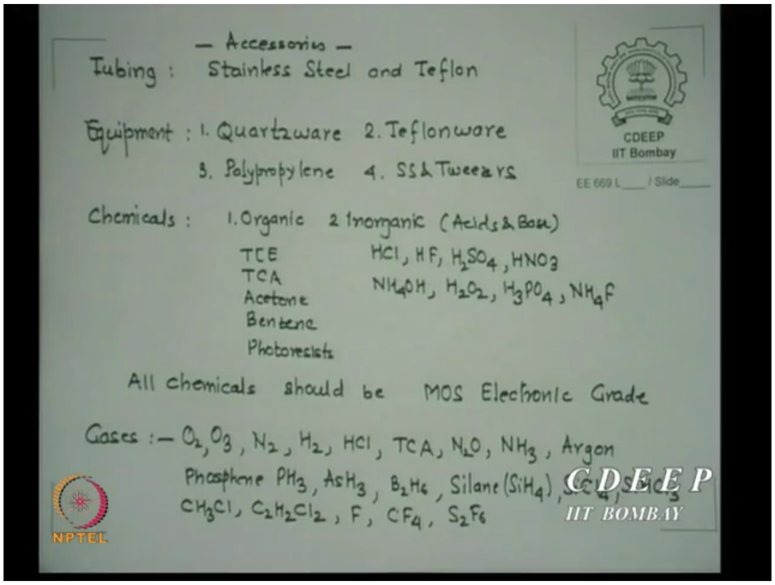

– Accessories –

Tubing : Stainless Steel and Teflon

Equipment : 1. Quartzware 2. Teflonware
3. Polypropylene 4. SS & Tweezers

Chemicals : 1. Organic 2 Inorganic (Acids & Base)

1. Organic	2 Inorganic (Acids & Base)
TCE	HCl, HF, H_2SO_4, HNO_3
TCA	NH_4OH, H_2O_2, H_3PO_4, NH_4F
Acetone	
Benzene	
Photoresists	

All chemicals should be MOS Electronic Grade

Gases :– O_2, O_3, N_2, H_2, HCl, TCA, N_2O, NH_3, Argon
Phosphene PH_3, AsH_3, B_2H_6, Silane (SiH_4), $SiCl_4$, $SiHCl_3$
CH_3Cl, $C_2H_2Cl_2$, F, CF_4, S_2F_6

In a lab there are many kinds of things which we have to work with. There are tubes which carries gases, sometimes water line and they are made of two materials. Either stainless steel or Teflon. Teflon is a very famous polymer which actually one always say nothing sticks, so he is a Teflon person, Teflon face person. Nothing sticks of him, kitna bhi bolo kuch asar nahi. That is the Teflon thing.

It is, normally there are both colored and non-colored Teflons are used. But the best Teflons are white-colored which means no other impurities other than Teflon itself. And therefore Teflon tubes are normally white, now Teflon everything which we actually use in the lab are either Teflon or at the some time polypropylene ones. Or mostly the gases pass through stainless steel. Please remember stainless steel is also of different qualities, 304, 306, 316.

If you are really a hard-core engineer in a lab, you will have to know which tube to buy. 316 is very costly, it is, it does not have chromium inside but it has chromium coating outside which is why it has become stainless. And it does not affect much of the grease, much of the other things and it is highly pure steel.

It has much less carbon content because we are not looking for hardness. So this 316 stainless steel tubes are used and of different sizes, quarter inch, half inch, 1 inch, 2 inch depending on the flow you are looking for. Then we have equipments which are used along with, in the process, are quartzware. Everything has to be quartzware and even including tweezers and many many things which we use there are either quartz material to racks, tubs, everything are made of quartz or some time Teflon. Either of them, no other species are allowed in.

Sometimes if the initial cleaning is to be done, removal of grease or something, it can be done in normal polypropylene which is also highly pure. We use tweezers, of course this word now is almost gone. Earlier we used to have wafer size of 3 inch, maybe 4 inch. So a tweezer, I could hold it because its mass was not very high. With 12 inch wafers we need probably 2-handed two tweezers and even then you do not know it may break.

Nowadays we just replace it with gongs they say and then you put into rack immediately or rack to rack transfer. From one rack you put to other rack. But if you are using SS, I mean tweezers, then they should be SS or Teflon. SS, I have not used with any S8s because they will be attacked. Only water or some such material where we can use. Stainless steel, highest quality stainless steel is 316. The chrome, carbon combination is very good.

Some other day metallurgy if you want to see, what is SS? Chemicals, we use both kinds of organic and inorganic chemicals often in the cleaning process as well as during the other processes. For example, if you see organic, we use trichloroethylene, trichloroethane, acetone, benzene and all kinds of resist, photoresist, EBIB resist and these are all organic materials. Then we also use inorganic acids and bases.

For example, we use (chloric) hydrochloric acid, hydrofluoric acid, (hydro) sulfuric acid, nitride, nitric acid, ammonium hydroxide, H_2O_2, H3, orthophosphoric acid and ammonium chloride. All these are inorganics materials and they are used. One important thing which I wrote just below that, all these chemicals should be MOS electronic grade. This is essentially, minimum electronic grade material should have 6 nines purity. That is 99.9999 purity, percentage.

Whereas the MOS grade is not only it is better than normal electron, it is 8 nines purities plus it has some way no sodium inside. MOS is most affected by sodium, I have shown you other day and therefore it does not have any alkaline. It is particularly sodium or potassium. So therefore these are called MOS grade. Unfortunately in India no one makes MOS grade chemicals. So if you go to other lab, everything looks to be imported.

That is the worst part in all these technology because there is no fab IC here, big ones. And therefore there is no sale, you have to make such things. So we all import. Of course please as I told you the electronic import in 2025 may exceed oil export. So please, oil import, so please think of it. Any small amount you say today is at least 1 percent saving in 2025. Gases, we use all kinds of gases: oxygen, ozone, nitrogen, hydrogen, hydrochloric acid gas, TCA gas, N2O, NH3, argon, phosphine, arsine, diborane, silane, silicon tetrachloride gas, of course you have to boil it.

And silicon trichlorosilane, monochlorosilane, dichlorosilane, fluorine, CF4 and sulfur fluoride, S2F6. All these gases are required for some things, some of them are cleaning, some for etchings, some for reactions and some for putting better oxide growths. So all these gases are required and many or most of them are again as I say better than electronic grade. There should be very very ultra-ultra-high pure gases. Some of them are very poisonous, extremely poisonous.

For example, phosphine, arsine, they are extremely poisonous. Silicon tetrachloride fumes are poisonous. CF4 is, Freon is very poisonous. Do you know why, where does, where was this used earlier and now we stopped it? In air-conditioners or fridges. We have changed this CF4 from there. We use S2F6 sometimes, some other, we also removed dichlorosilanes from there. They are very toxic ones. Also some of them are flammables. Like silane is extremely flammable like hydrogen.

It just at room temperature, under pressure it just blast. So we have to be worried about the tubing which you keep, the exhaust you keep. All these have to be taken care when you are working in the lab when the cylinders are there where the gas is stored. No leak should occur there, there should be leak detectors, there is should scrubbers which immediately removes those gas into non-toxic material, converts them. All these are required when you actually enter this.

So then why do I enter? Itna sab problem hai, nahi but that is the fun part. I make devices or I make circuits. As I say so a clean room making is a tough job and maintaining it is even worse because humans will be there and they will never care but the system does not believe that way. So it spoils. So devices, read was very anyway 1 out of 100, it will be 0 out of 100. So that is where you should start looking for, that your cleanliness has to be there. Of course there is a fire extinguisher, there are gas extinguishers, there are some mask, everything is available when you are working with any toxic and flammable gases.

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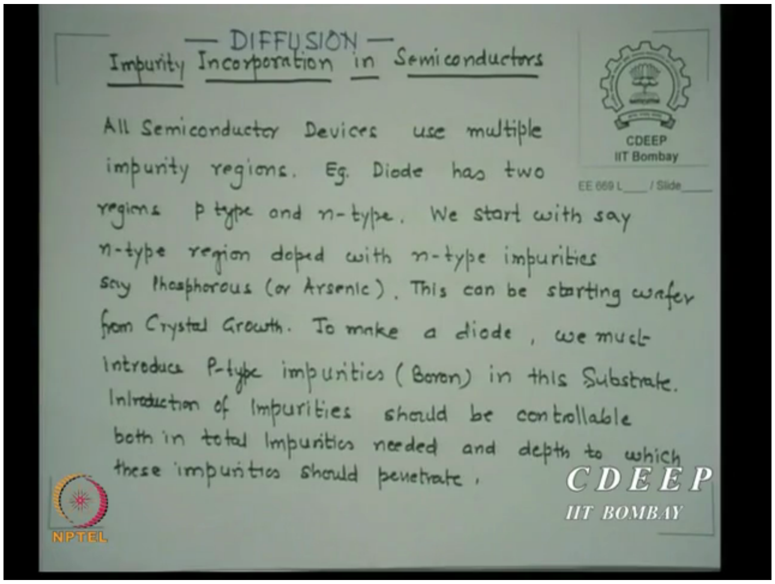

— DIFFUSION —

Impurity Incorporation in Semiconductors

All Semiconductor Devices use multiple impurity regions. Eg. Diode has two regions p type and n-type. We start with say n-type region doped with n-type impurities say Phosphorous (or Arsenic). This can be starting wafer from Crystal Growth. To make a diode, we must introduce P-type impurities (Boron) in this Substrate. Introduction of Impurities should be controllable both in total Impurities needed and depth to which these impurities should penetrate.

I will start with the new, this was all about the last lecture, these two slide I could not finish yesterday. So I start with now the new topic which is diffusion. The diffusion process is the most important process in semiconductor device fabrication or IC fabrication. All semiconductor devices use multiple impurity regions. Diode has two regions, p and n. Transistor, bipolar is 3, p and p. MOS has substrate source drain, plus thin oxide plus gate. So we can see there are different kinds of areas have different kinds of doping and different kinds of concentrations of impurities.

That is the major part, like source drain are really heavily doped materials areas. So most of the time we start with a wafer which is, it is from the crystal grown and we can add impurities directly when the crystal is grown. So that time we can make substrate either p-type or n-type whichever way you, whichever impurities I add during crystal growth, so wafers are available, p-type, n-type for given dope and concentration.

So we call that a substrate. So wafer is we call substrate. And as I say thickness can be as large as 1 millimeter or maybe more now with 16-inch wafers. And we will use only large, better the technology we are going, smaller is the surface area we are using, smaller surface depth we are using. In 5 micron processes we at least have junction depth of around 1.5 to 2 microns. Now with 14 nanometer, the concentration there of source and drain is even around 50 nanometers only.

So everything is killing other. So what is happening? There wafer is thickening but the volume which you are using of silicon is very thin, very small. So rest is only physical support. As I say of course silicon is far better than other material which is very popular in other areas called 35 compound materials. Gallium arsenide, (())(19:15), I do not know, host of them. Said in gallium arsenide that if you see, it may break. So how do I work? That is the fun.

So gallium arsenide is extremely fragile, silicon is not that fragile as gallium arsenide but it is fragile. Is that okay? So we want to control impurities. Let us say at this, so during the crystal growth we are controlling one kind of impurities. But when I make a diode, I will integrate the other kind of impurities for given concentration to a certain depth and that will make my diode. That controllability is essentially what is most important in making any semiconductor device.

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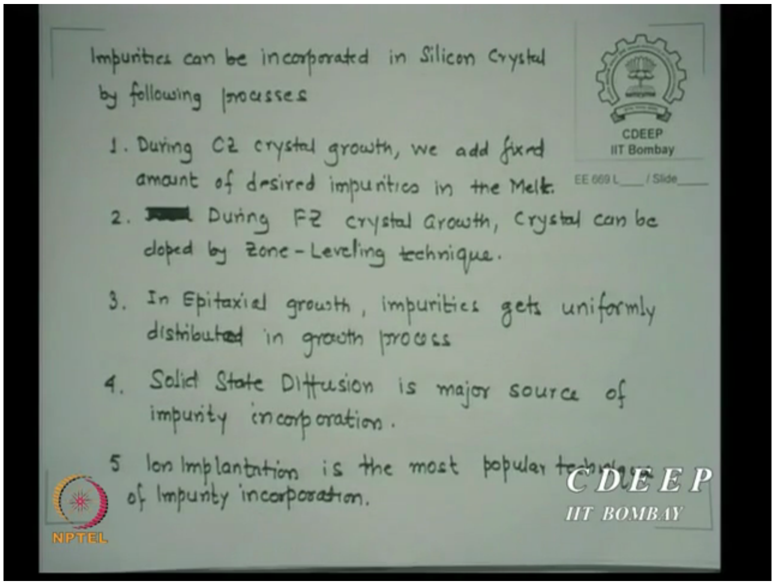

Impurities can be incorporated in Silicon Crystal by following processes

1. During CZ crystal growth, we add fixed amount of desired impurities in the Melt.
2. During FZ crystal Growth, Crystal can be doped by Zone-Leveling technique.
3. In Epitaxial growth, impurities gets uniformly distributed in growth process
4. Solid State Diffusion is major source of impurity incorporation.
5. Ion Implantation is the most popular techniques of Impurity incorporation.

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So impurities in silicon, right now as I say if I do not say anything, material is silicon for us. We are only for silicon ICs, so unless said otherwise 35, 26, no other semiconductor will be thought of in this process. Though gallium arsenide technology is maturing and it is a technology of future, and as I said future never comes, 50 years it has not come. However move himself is suggesting that yeah, it will come. So maybe it will come.

During CZ crystal growth we add fixed amount of desired impurities in the melt. So one method is this, the other is during float zone we can add a dope crystal and actually give a number of passes to give uniform doping from that dope crystal to the undope crystal. That is called zone leveling. So we have shown in the float zone we can actually uniformly dope from a given standard silicon which is doped, known value and you keep passing the float zone and it all impurities will get distributed along axis.

And therefore this in FZ it is using zone leveling but it is uniform doping. What is important in crystal growth? The doping is fixed or at least uniform. I do not say fixed. Of course number can be decided by amount of impurities you add, an amount of in case of zone leveling how many passes you give and what is the Na concentration in the crystal you start with. There is another process which we will look into is called epitaxial growth. Now this epitaxial word, epitaxial growth impurities gets uniformly distributed during the growth process itself.

It is more like crystal growth but it is slightly different. Solid state diffusion is the major source of impurity incorporation. How? From a solid source like in the case of phosphorus it is phosphorus pentoxide, P2O5. In case of arsenic it is As2O3, arsenic oxide. In case of boron, it is B2O3 which is diborane. So we have solid sources which contains impurities and from solid into silicon solid, we pass the impurities.

So therefore this diffusion is called solid state diffusion. However nothing can move unless the temperature is increased. We will see how much it will be. This is the major force where impurities are earlier used to be incorporated, flake we do not but this is, there are some, I have to learn this much more because even after any process I do, impurity motion is decided by process of diffusion. So we will see that again.

The most important process of incorporating impurity these days is ion implantation and we will have full 3-4 hours of talk on the implants because these are the major. We at least have to go through 6 to 8 implants processes, steps before we make an IC. So implants is a major process of incorporation of impurities. Basically what we are doing is whichever impurity I want to introduce, I somehow get it purified form of that by some method and then by electromagnet I only get that element getting into a particular tube because it will follow certain Lorentz law.

And it will bend only in one particular angle. So I pick it out and I put a lot of electrostatic field on that so that it picks energy and these high energy ions of impurities actually go and bombard the silicon. So this is wafer and this is beam, it just bombards. So if I want everywhere, I just scan it like this. So I actually push the impurities by force. I am having lot of kinetic energy, I am bombarding static silicon. So they will hit the silicon atom and get in by force, robbery, just get in.

However you need huge energy, 300 kv or something like that, we will see in implants. However these are the major, this is the major step in which we can incorporate impurities. There is a version of this which is more like a CVD, which we call, it is called plasma implants. So when I teach implantation though it is not part of implantation specifically, I will tell you what is the difference we did.

The reason why we went to plasma was low temperature process compared to normal implants process. So we will see, we will do on plasma implants. Of course there is energetic ions is created, therefore still plasma, still ions but created out of plasma, therefore is plasma implants. We will see this when we come to that.

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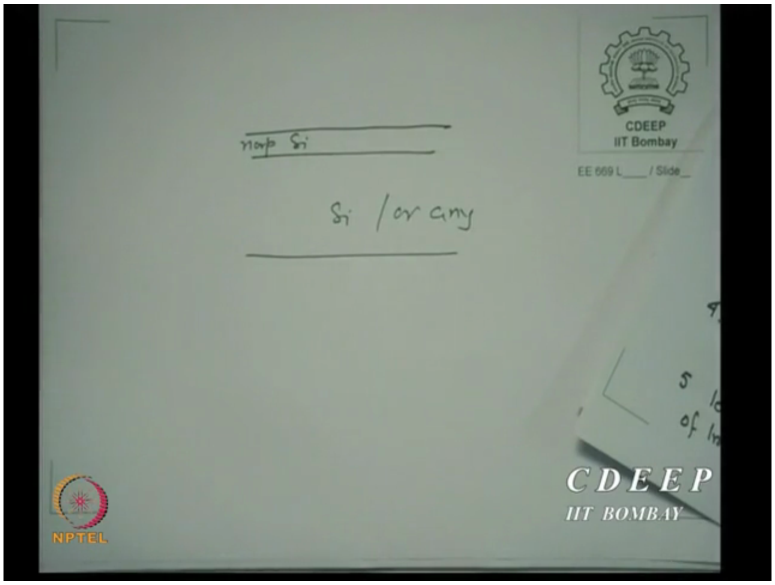

The epitaxial growth is like a growth on any substrate, it can be silicon or any other substrate. It can be glass, quartzware or even gallium arsenide, any substrate, gallium nitride, any material you can put. And the top of this I will create silicon by wafer depositions. And during wafer deposition I can make n or p. This is called epitaxial, word essentially starts, come from the growth as below. So whatever crystalline part is below is replicated above, is called epitaxi, as it is grown.

So epitaxial is the process where we want very thin silicon layer on silicon dioxide shape, I do not want silicon. Then I have to deposit it on any other surface and that is called epitaxi. So that process is slightly different from normal crystal growth base. So the silicon is brought in the contact, it will heat it, it will sit there. All this process will be discussed in epi growths.

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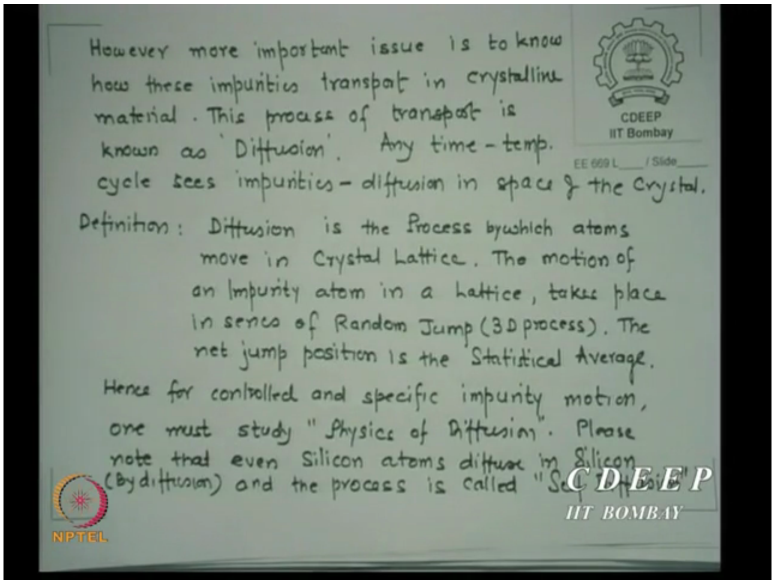

However more important issue is to know how these impurities transport in crystalline material. This process of transport is known as 'Diffusion'. Any time-temp. cycle sees impurities-diffusion in space of the Crystal.

Definition: Diffusion is the Process by which atoms move in Crystal Lattice. The motion of an Impurity atom in a Lattice, takes place in series of Random Jump (3D process). The net jump position is the 'Statistical Average'.

Hence for controlled and specific impurity motion, one must study "Physics of Diffusion". Please note that even Silicon atoms diffuse in Silicon (By diffusion) and the process is called "Self Diffusion"

However more important issue, then all that I said so far is to know how these impurity transport in crystalline silicon or material. This process of transport is known as diffusion. Any time-temperature cycle to silicon or any substrate or wafer which may have any other process done earlier, whenever it sees time-temperature cycle, what does that mean? Wafer sees certain temperature for a given time is called time-temperature cycle.

And if wafer sees any of these larger time, small temperature, larger temperature, smaller time, larger temperature, larger time, whatever it is, then the impurities which are already inside will get energized and will start moving. These impurities will start moving. This process is called diffusion. We will see this. This is what whole next our, other time I will do. So what is the definition we will say?

Diffusion is the process by which atoms move in crystal lattice. The motion of impurity atom in a lattice takes place in series of random jumps. Now this word is important because diffusion process is a random jump process or random work as it is called. What is random work? It is a statistical process, random word itself says it is statistical. So a person is standing here, maybe our CR is standing here and he has probability that let us say one axis he decides.

He can either come to my side or he can go the other side. So there is a 50 percent chance. This person may come this side, 50 percent chance, he may go backside. Similarly 50 percent chance, he may go to left, 50 may be right, maybe any angle. So there is a 50 percent probably across, left or right or whichever it is. So it is a random process. However after long time this, he is not found there which means he has moved from his original position even in random jumps.

So the distance which it travels is essentially because of process of diffusion. The simplest example of diffusion given in many elementary books is if you have water, add ink drop, on the top there is a bluish surface and suddenly it becomes blue all around. So the ink atoms actually diffuse through to equalize, this word is most important. The diffusion want to equalize. So let us say I smoke which I do not and I hope none of you should.

So for example, if I show the snow particles are largest concentration here where I start, are incense like agarbatti. You use, burn it, so for right only it is particles are around but after sometime everyone smells. It means these have gone back and forth, back and forth but at the end equalize everywhere. This is the process of diffusion. However in case of silicon I do not want impurities to go everywhere, I want in a particular direction and that is the game we are trying to play.

I want it to get in where I want. If they go randomly, it is isotropic system, they go everywhere. Then I am under not control. So I want to see they actually channelized, they come to where I want, to a depth I want, number I want. This is something what we will do in the technique, how to control everything. The process-wise it is a random work system.

So as I said you how hands were controlled and specified impurity motion, one must study some physics of the diffusion because we have to finally control. All my life I have been preaching you all that every subject has some influence on others. Why learn physics? Learn because if I have to do something at the end to control, then I cannot say someone should have written a software directly. Yeah, these days many softwares are available.

So let us stick, please note that even silicon, interesting part is very important in this. Not only the impurities, the silicon itself can move. Atoms during temperature cycles can move from one position to the other, is called self-diffusion. However as I see this will be much smaller than impurity transport but there is a self-diffusion also possible. So anything in heat cycle you will see some kind of motion and that is essentially process of diffusion.

Have you noted down? Anyone? Of course these are given every book, not necessarily in the language, not necessarily in the order but given in most book because these have nothing to do with any specific person. This is process, I may state in one way, you may state in another way but you have to state the same at the end. So please remember this most important part, the self-diffusion because now I am, sooner I will come to this, how much is self-diffusion and how much impurities because in real life both can happen. So how much I will be tolerating the other ones? Or will that add or will that obstruct, we will see that.

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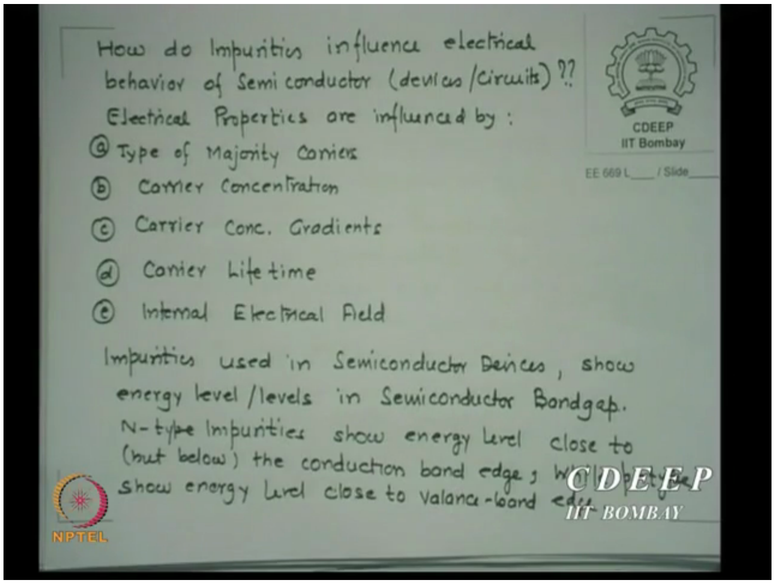
How do Impurities influence electrical behavior of Semiconductor (devices / Circuits) ??

Electrical Properties are influenced by :

ⓐ Type of Majority Carriers

ⓑ Carrier Concentration

ⓒ Carrier Conc. Gradients

ⓓ Carrier Life time

ⓔ Internal Electrical Field

Impurities used in Semiconductor Devices, show energy level / levels in Semiconductor Bandgap.

N-type Impurities show energy level close to (but below) the conduction band edge ; while p-type show energy level close to Valance-band edge

How do impurities influence electrical behavior in semiconductor devices and circuits? They are essentially concentration decides the majority, how much types of majority can reduce p-type or n-type, that will decide the property. How much numbers, carrier concentration you have is also going to decide the property of the semiconductor or circuit rather. Carrier concentration, gradients decide how fast or how distant they will go.

Then carrier lifetime, how long they can survive, is called lifetime. Most devices are affected by this word lifetime. VJT, they are maximally affected. The minority carrier lifetime in the base decide the gain of a transistor. So lifetime is very crucial in most processes. So in many technologies if I am working for power rectifier industry or I am working for micro industry where they use what called PI and diode, I have to control the lifetime in the I region very strongly for faster or slower whatever I want. I will have to control the lifetime, so this process is very important in deciding the property of a device and which is technologically has to be controlled actually.

Then of course there are internal electric fields, you are looking of charge. Any charge is essentially affecting each other because this is the space charge and there will be always a Poisson's equation sitting right there. So there will be electric field and therefore voltage drops. So any charge system will always be associated with, this is essentially statement of Gauss's law. So one of the Max's equation and please I do not know if anyone of you who appeared in, I do not take these days MTech or PhD entries often.

But once a while if I sit, I ask such trivial. Why should charge should give electric field, so that is I am asking natural equation. So you also start thinking Max's equation is the crux of all electrical engineering. If you do not know 4, at least learn 2 by heart. And know about other 2 otherwise. Is that okay? Majority type concentration, gradient, lifetime and internal fields decide the device property.

Impurities used in semiconductor devices show energy levels or level in semiconductor band gap. n-type show energy level very close to the conduction band and p-type show energy level close to the valence band. If an impurity gives a level at the mid gap, that is Eg by 2, what are those called? Recombination centers, both hole and electron can come and recombine. These are called recombination. They are away from the edges, that means they are called traps.

Any impurity will give energy level in the band gap. If it is near conduction band, it is n-type. Near valence band, p-type this. In the center, recombination center and anywhere else, it is essentially electron or volt trap. And that also is very important way of controlling device property. Yesterday I said leakage current in MOS transistor is essentially governed by Shockley-Read-Hall recombination theory. Theory is not relevant, actually we see it. So theory is only because Shockley did it, everyone has to see Shockley did it, so we also should say.

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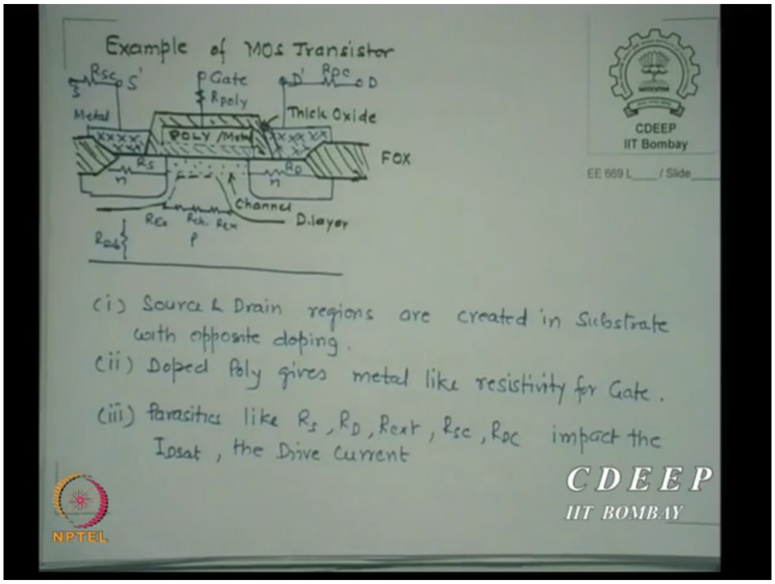

Example of MOS Transistor

(i) Source & Drain regions are created in Substrate with opposite doping.

(ii) Doped Poly gives metal like resistivity for Gate.

(iii) Parasitics like R_S, R_D, R_{ext}, R_{SC}, R_{DC} impact the I_{Dsat}, the Drive current

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The another example of electrical behavior is shown here. This is a MOS transistor in channel kind. Of course the statement is always made that channeled MOSFETs are better than p channel. This is little false statement. In a CMOS both are required, so why do you say this is better or worse? And p has its own advantage, n has its own advantage. But let us say because mobility of electrons is some numbers higher than the holes, we keep believing NMOS is the best device. Please do not go by that correct statement in every book, everywhere they write.

This is Milman's thinking, this has to be like this. He was in 1800 times, so he still think this in 2000 it is correct. For example, we used to teach in 87, CMOS process is the low power process. In 2010, it is no low power process, it is as much consuming as I told, I thought earlier. We did not think that time. So all statements have to be modified as years come. Here is oxide which is called fork, this is essentially what I am going to fabricate.

So all the process, some they are shown here, not every one of them, many of them. So this is a p substrate, n regions are created which are source and drain. There is a metal contact to source and drain. These cross ones are metals. Just above the source drain area, please take it area, this is 2-dimensional but in actual device transistors are 3-dimensional device, WL and thickness is third dimension. So this thin oxide setting here can be insulator of any other, earlier it was SiO2 and even now many devices use SiO2. But now the new names, lanthanum oxide, hafnium oxide, hafnium oxynitride or tantalum oxide, titanium oxide, zirconium oxide, all are trying to replace silicon dioxide.

The top of this can be either metal or polysilicon and this if it is poly, it has to be doped because poly doped can be have, will have a concentration around close to metal, not any way very close but close to metal. So I want a metal like structure there. So I use dope poly, it is always covered by oxides. These are called spacers, we have problem there. So if you see, you go on different materials here, n is why, n plus doping is here, so np is doping in the substrate. Then there is a polydoping. There is metals here which make a contact with silicon.

Please metal into semiconductor is called schottky contact, that is rectifying contact. It can be made ohmic by doping heavily below. But it is still rectifying, rectifying contact kaa, what is the difference between ohmic and rectifying? What is the difference? The resistance in the other case is 0 in ohmic, in rectifying they will be finite resistance of the contact, it is called contact resistance.

So we can see there is a contact resistance due to this metal and there is a semiconductor setting here, source and drain, they themselves will have source-drain resistances. Then there will be a channel, some part will be depleted out in the below. So there will be some contact here as well. There is a junction resistance here, there is the junction here. Below is depletion layer. So there is a pure channel resistance, some external additional resistance, extra resistances on the edges.

And there is as I say, poly is not as good as metal, so it has some resistivity and therefore it will have some resistance, so it is called gate resistance. Many people believe that gate resistance does not play huge role because there is oxide setting, no DC current pass. But the AC we are passing, shaping, RC time constant is there. That means the input clock will never go with the same frequency if R is larger. It will get attenuated right there.

So please remember gate resistance many people do not even think it but as I increase frequencies, I did realize that time constant is also very relevant. So in 2000 onwards we are going back from polysilicon gate to metal gates. So then question arises, 70s mein bhi metal gate tha, tab kyon nahi, abhi continue kyun nahi kiya? We will come to this technology. Of course we are not using same metal. There we use aluminum earlier, now using molybdenum, titanium, tungsten, many other materials and they are silicides as word goes.

So that means there are parasitics which are RS, RD, R external, RSC, RDC and they will adjust. Let us look at current going from source to drain, simple one calculation. If there is a very small R here or sigma is very large, the current is essentially called death current, field death current. So J is sigma E. If sigma is large, current is large at smaller E, sigma is large. If there is a resistance there, I will have a drop on this parasitics.

So I now applied VD but actual VDS may not be exactly what VDD I apply because there will be a drop in the this parasitic. Essentially means I require additional current to come either by increasing power supply voltage or by increasing the size of the transistor. Because otherwise the speed will go down because your R is getting, current will reduce which is called IDsat current, the current of a transistor is defined in IDsat. That current, drive current will go down because of simply drops in the parasitics.

Resistance we shall see soon, is a function of rho L by A. So some way if you are thinning something, your resistance will increase in newer technologies. We thought it will be decreasing, actually it will increase. So more worry started when you scale down the new technologies. 14 nanometer have worst problem. So we are now seeing why dope, we will make schottky contact, metal-metal, no in between. There are issues with that, we will see that technology later.

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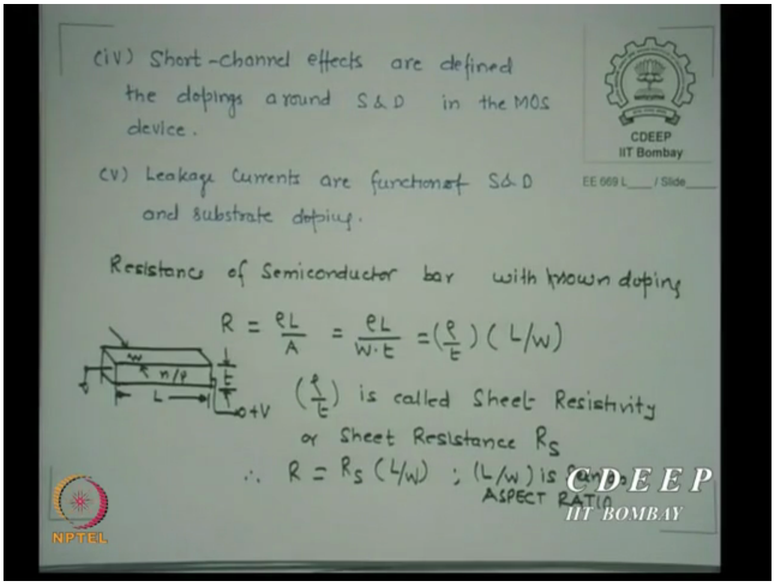

(iv) Short-channel effects are defined the dopings around S & D in the MOS device.

(v) Leakage currents are function of S & D and substrate doping.

Resistance of Semiconductor bar with known doping

$$R = \frac{\rho L}{A} = \frac{\rho L}{W \cdot t} = \left(\frac{\rho}{t}\right)(L/W)$$

$\left(\frac{\rho}{t}\right)$ is called Sheet Resistivity or Sheet Resistance R_S

$\therefore\ R = R_S (L/W)$; (L/W) is called ASPECT RATIO

If you scale down the technologies from say 1 micron, 90 nanometer, 45-65-45-32, this is the channel start reducing and it gives lot many effects. Professor Vasi is the best person to explain them. Short-channel effects, it deteriorates the performance of transistor. If I would have been teaching that, I would have taught but since he is the best person around, so you learn from him. This is very important worry for all designers, short-channel effects.

And of course they are decided by doping’s size, so around source and drain. The fields you create, they are very crucial. Leakage currents as I just said you, the substrate doping decide the leakage current, so is the because of the junction formed. So all these you can say technology is some way controlling the circuit performance or device performance. Larger current means higher speeds but larger current means higher power to keep matching what do you want.

So our worry, what is our ideal thinking? We must make a chip or device which has 0 power consumption, infinite speed and 0 area. That is the ultimate but that is only 0. So please do not believe it will happen but just that is the ultimate way of looking for. Typically such things which are used in my theory, my measurements as well as theories, the resistance of any bar of a semiconductor n or p is given by rho L by A. L is the length, e is the thickness, w is the width.

If I replace it as A by w into t, then I can rewrite rho by t into L by w. One can see from here rho by t, if rho is constant, when rho will be constant? When the doping is constant, rho will be constant. But if the doping is varying, rho will also be a function of x or y or z whatever. So rho by t if it is constant and even if rho is a function of x or y, that term is called sheet resistivity or sheet resistance Rs.

So we define R as Rs into L by w. Now you can see this L by w is also called aspect ratio. If you see this semiconductor bar and if you say L by w is equal, is smaller than L, so you have say three parts. This is also one w, ww, so one can see one cube of L, L and w is same, so one cube, two cube, three cube. L by w is 3, 3 cubes or length is three times the width, so it is L by w is 3. So it is called aspect ratio. So if I want to increase or decrease resistance, one of the method is adjust sheet resistance or adjust aspect ratio.

This has, in a design this is important. How much resistance you want, you must decide whether I should use aspect ratio as, if the dopings are fixed which you cannot modify, then the only way R can be varied is by different L by w. If you are allowed to vary dopings, different regions, what is the problem if I dope different regions differently? So many mask will be, every small process I have to mask rest of this and dope only that part.

So mask numbers will increase but they will be more accurate. I control rho much better and therefore resistance in a circuit is normally avoided in most circuits because this R control is very difficult. Larger the R means larger the aspect ratio. Who will put, if one chip contains only one resistance, what do I put up? Therefore bipolar technology lost race many times simply because without R it cannot work easily or where is better way?

And Rs are the, there is emitter resistance, collectively everywhere resistance, resistance. Now I cannot put too many R, such things on a chip. Instead I put MOS transistor itself everywhere. So I have better way of doing. However as I say bipolar still could be faster, could be MOS are getting on. So please remember R, this Rs word is very crucial, called sheet resistance. You will actually monitor in a lab, whenever I do diffusion, the first thing I monitor is the sheet resistance, how much sheet resistance I got. And that gives me an idea how much doping I have done. So this is my major parameter which I control or which I monitor actually.

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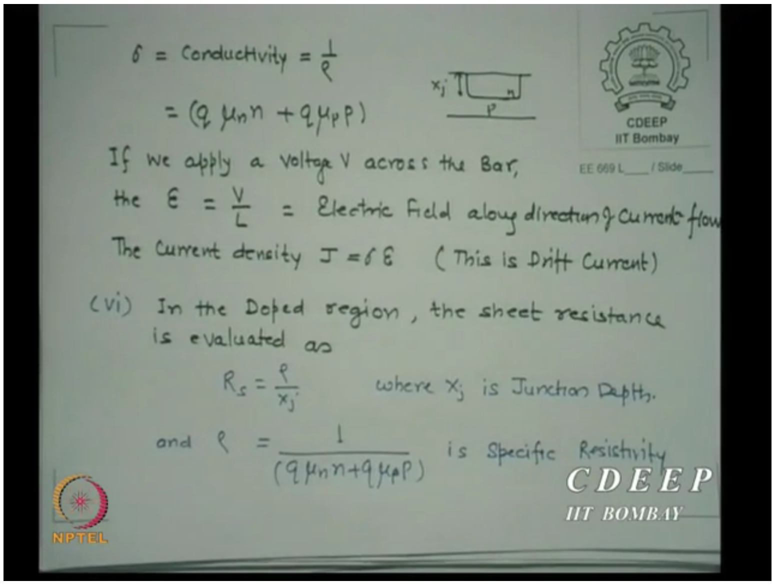

σ = Conductivity = $\frac{1}{\rho}$

$= (q \mu_n n + q \mu_p p)$

If we apply a voltage V across the Bar,

the $\mathcal{E} = \frac{V}{L}$ = Electric Field along direction of current flow

The current density $J = \sigma \mathcal{E}$ (This is Drift Current)

(vi) In the Doped region, the sheet resistance is evaluated as

$R_s = \frac{\rho}{x_j}$ where x_j is Junction Depth.

and $\rho = \frac{1}{(q \mu_n n + q \mu_p p)}$ is Specific Resistivity

Extending same thing we know conductivities q mu n plus q mu p. If it is n type, then it is n is larger than p, so we can have either q mu n or q mu p or if it is p type. The current from say x direction where the voltage they are applied, for example, let us say this is x direction along L. Then the electric field is voltage divided by the length, applied voltage divided by the length is the electric field along the x direction.

And the current and sigma is given by the carrier concentrations you have. So J into sigma E is the current which is called drift current density. If you want current multiplied by area, so you get current density, J, I by A is J. So I is A times sigma E. In the dope resistance if I have a junction, maybe I will show you here. This is let us say p and n, so the impurities have only gone to a distance and where junction is formed between p and n. This depth up to, from where the junction lies is called junction depth.

That means impurities from the surface are introduced and they go up to xj and the material is n-type only till then. Below this there is a p-type. And what happens at the junction, how many impurities? 0 because they must, that is how junction is made. They are compensating each other. This is what essentially I say. Rs is rho by xj in case of diffused regions and rho of course is 1 upon q mu n, q mu p is a specific resistivity.

So rho by t instead xj is, in real diffused regions it is instead of t we write xj. Let us say if n is not uniform in the dopings, normally the diffusion process does not give uniform doping, only crystal growth, epi growth gives it. But diffusion process is gradient based. Please. Diffusion processes are gradient based, so their concentration is not uniform everywhere. So they give some profile nx downside and surface concentration is the maximum and impurities start diffusing down due to the gradient.

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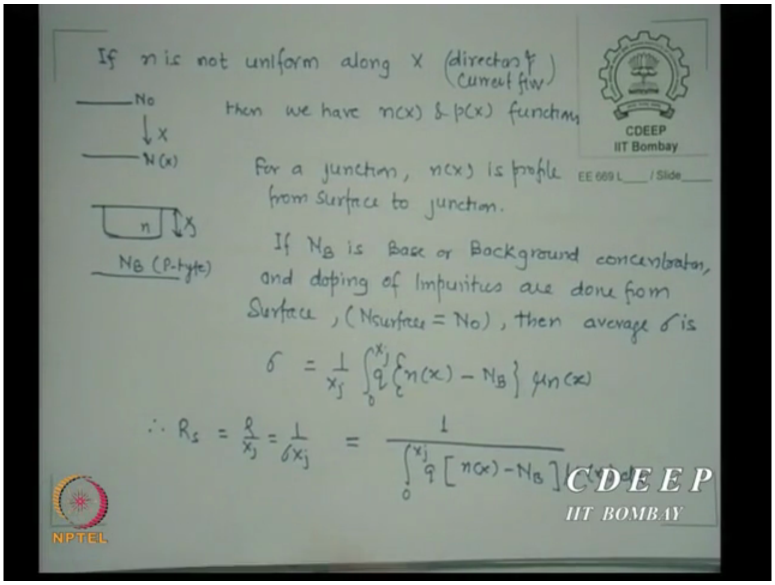

If n is not uniform along x (direction of current flow)

then we have $n(x)$ & $p(x)$ functions

For a junction, $n(x)$ is profile from Surface to junction.

If N_B is Base or Background concentration, and doping of Impurities are done from Surface, ($N_{surface} = N_0$), then average σ is

$$\sigma = \frac{1}{x_j} \int_0^{x_j} q \{ n(x) - N_B \} \mu_n(x)$$

$$\therefore R_s = \frac{\rho}{x_j} = \frac{1}{\sigma x_j} = \frac{1}{\int_0^{x_j} q \, [n(x) - N_B]}$$

And somewhere down where this impurity concentration same as p-type, it will form a junction. We will show you the, this is what all that process will work into. So if I use this as my junction depth, I can then write sigma, average sigma, that is called universal averaging. What is averaging? Some of our terms divided by the distance you take or integral of that. So sigma is 1 upon xj, 0 to xj q nx minus NB. NB is the base concentration because these impurities minus these impurities are only available in this.

So Nx minus NB into mu nx. mu n also is a function of x because mobilities are also function of the dopings. Larger the doping, mobilities are smaller. So if you really want, this needs to be solved numerically not easy to solve analytically. However we define Rs as rho by xj or 1 upon sigma xj. So this 1 upon this integral is essentially sheet resistance. So I will tell you later, I can, if I monitor number of Rs at different points in xj, then I can find Rs or nx actually.

That is how the profiling is done. I repeat if I have Rs1, I find nx1. Rs2, I etch out something, measure again, then this, the next point, next point, next point. So actually I can plot n versus x as I keep etching and measuring Rs values. That is the one person we will see later. Otherwise you can do secondly on spectroscopy and can, since as the word goes we can always get a profile. But even there we etch, all that we do is etching.

So basically any diffused profile, the monitoring is only by sheet resistance. This is the whole crux of all that was that whether it is uniformly doped or gradient doped, this will always be, Rs can be always monitored at the surface. So x is equal to 0 at the surface, we know the concentration which we start with which is essentially called, the word we shall use later is called solids solubility. What is the word solid solubility? We always talked of solutions.

The maximum number of atoms which can introduce into other material without dislocating it or without disturbing its lattice structure is called solid solubility at a given temperature. Solubility is a function of temperature. Largest number of, like in silicon we have 5 into 10 to power 22 atoms per cc, is the concentration of pure silicon. So obviously no impurity can be, 5 into 10 to power 22 per cc, why? If they replace all of them, then there is no silicon. So obviously silicon concentration will be higher than impurities.

So the best of doping can be done with arsenic which is around 4 into 10 to power 21 per cc, one order less. 10 atoms of silicon, 1 arsenic. That itself will put some value of sheet resistance because larger the, even larger when I reduce the resistance. So I want to see how much higher I can go. Is that Rs clear? Rs can be figured out even in the dope regions as well as universe, uniform ones. So it is not that only you know uniform doping, I can have profiling and I can find what is the way impurities getting in.

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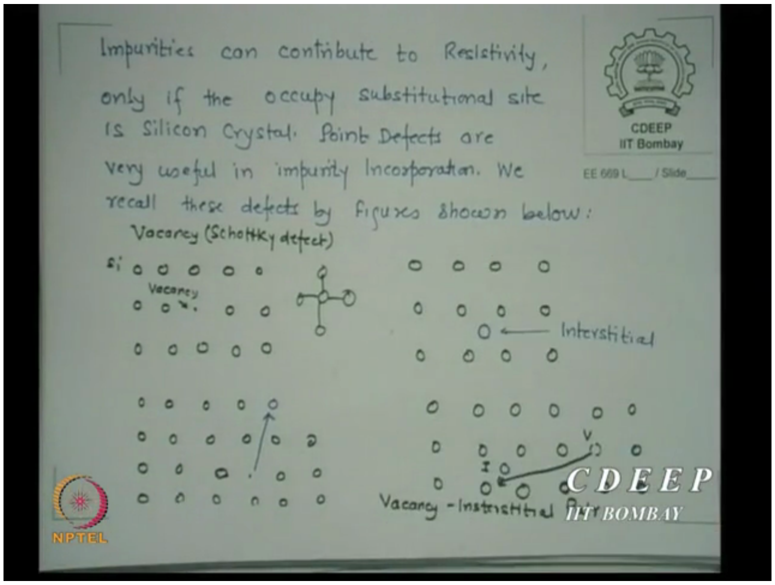

Impurities can contribute to Resistivity, only if the occupy substitutional site is Silicon Crystal. Point Defects are very useful in impurity Incorporation. We recall these defects by figures shown below:

Vacancy (Schottky defect)

Impurities can contribute to resistivity only and only if these occupy substitutional sides. If they are on interstitial sides, they do not want itself to any silicon. Here is an example. This is the silicon lattice. These are atoms and there is a vacancy here, no atom. And as I already discussed with you, vacancies are naturally created because of the crystal growths when we dope. Some atoms just do not go there where they should.

But when we say it is a defect, methane it is a defect but if it is not there, there is no doping. So it is good that there are defects. These are also first found by schottky and therefore they were given in schottky effect. Now if you have a vacancy, it can be also created by something. You have a lattice, good lattice and during this crystal growth freezing because of energy release, one atom may leave the space and can sit other places, may go to interstitial also but then creating a vacancy there.

If this atom moves from here to here, it will create a vacancy. So vacancies can move, is that word clear? Atoms jump, self-diffusion. Atom jump create vacancies. From here something else will come, vacancy will move somewhere else. So we say vacancy also can move. This is important. This is the other diffusion we can see. If silicon any impurity atoms sits between this lattice points, not bonded to anything, please remember silicon is essentially tetrayl and bonded. So every silicon is, has one silicon on all sides. This is how silicon lattice works, 4 sides each.

Similarly for these 4-4-4. But there is a place in between and those, this essentially is called primitive lattice, 3 these is called primitive lattice, it is not in itself. This is called primitive lattice. So I have figured out if I take a surface picture of this primitive lattice, these are four atoms. There is a void in between which is actually larger, do you think so? Even if whatever is their size, this space, diagonal space is larger and because of that voids are very easy to be available for us.

So actually impurities will like to go where? To the void space because they are, they have enough number everywhere available and they will try to go there. So interstitial diffusion as such looks to be much more dominant but if all atoms impurities sit into interstitial side, they do not get bonded to silicon atom and therefore no change in resistivity. At the end they may give defects. So but it can also form something else as I just now talked about this, a vacancy from here and atom can move from a good lattice to interstitial side and create a vacancy.

Some other, this will come here, occupy this. So this pair itself will move ahead. It is a Frenkel pair, interstitial substitutional pair is called Frenkel pair. Unlikely event but can occur. Together jumping is unlikely event but can occur. So there are three major defects which we see in crystal, vacancies, interstitials and Frenkel. Sorry, interstitial and Frenkel. So the diffusion can happen to either at vacancy sides this or vacancy this pair itself can move. We will see this is also important actually. Is that okay? So this is something how impurities diffuse inside a silicon crystal.

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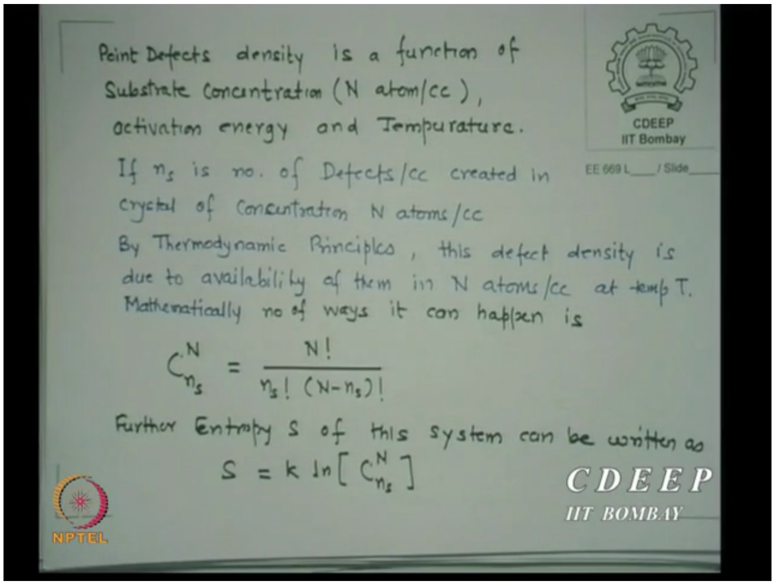

Point Defects density is a function of Substrate Concentration (N atom/cc), activation energy and Tempurature.

If n_s is no. of Defects/cc created in crystal of Concentration N atoms/cc

By Thermodynamic Principles, this defect density is due to availability of them in N atoms/cc at temp T.

Mathematically no of ways it can happen is

$$C^{N}_{n_s} = \frac{N!}{n_s!\,(N-n_s)!}$$

Further Entropy S of this system can be written as

$$S = k \ln\left[C^{N}_{n_s} \right]$$

Please remember the point defect density is a function of substrate concentration, number of atoms of silicon for example per cc. The activation A because if they have to know, they need some energy, so it is called activation energy. And of course at a given temperature only that much additional energy, it is a thermodynamic process, so thermal part will actually enhance the kinetic energy. So let us calculate at least this, how much, how many defects per cc we create. If Ns is the number of defects per cc created in a crystal of concentration N atoms per cc, if Ns is the number of defects per cc created in a crystal of concentration N atoms per cc.

The thermodynamic principle, the defect density due to availability of them in N atoms at a given temperature can be given mathematically. This is possible combination, permutation and combination towards the, one out of so much can go, so Ns is the defect, N is the number of how many ways actually they can have possible moving there. It can be given by C and Ns which can be given by N factorial, Ns factorial in minus. This is, I suppose you know this much maths anyway.

However thermodynamic system say the entropy of this system can be written as k, k is Boltzmann's constant, 1.23 10 to power minus 23 joule per second. Please remember number. Of course I will give data whenever I need, you do not have to remember. 30-odd year, 40-odd years I am doing so much of that, I remember all numbers but you need not. You will give the data.

Data is from our side. All that I am asking is this and handwork. So S is k ln, this probability see Ns to N, this is how it is defined.

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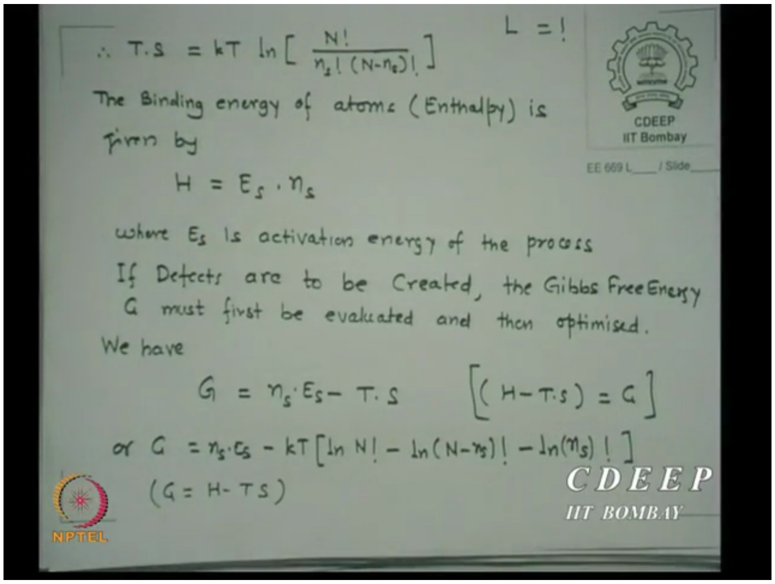

$\therefore T.S = kT \ln\left[\frac{N!}{n_s!\,(N-n_s)!}\right]$ L = !

The Binding energy of atoms (Enthalpy) is given by

$$H = E_s \cdot n_s$$

where E_s is activation energy of the process

If Defects are to be Created, the Gibbs Free Energy G must first be evaluated and then optimised.

We have

$$G = n_s \cdot E_s - T.S \qquad \left[(H - T.S) = G\right]$$

or $G = n_s \cdot E_s - kT\left[\ln N! - \ln(N-n_s)! - \ln(n_s)!\right]$

$(G = H - TS)$

Then I multiply both side t, so T dot S is kT ln N by upon Ns in this. The binding energy of atom which is also called enthalpy H as it is called can be written as activation energy into multiplied by, this is per unit volume into numbers. So how many defects? This is for creation. What is Es? Is the energy required to create a defect. If the Ns defect, the enthalpy, total enthalpy is Es times Ns. If defects have to be created, there is a thermodynamic slog which says maybe I should say somewhere below, G is equal to, or maybe delta G but right now I may say G is enthalpy minus TS where S is the entropy, T is the temperature, H is the enthalpy.

If H is larger than TS, Gibbs energy is positive. If H is smaller than TS, the Gibbs energy is negative. In any reaction A plus B equal to C plus D, a forward reaction is to be held, G should be positive. If reverse reaction has to be there, C plus D coming back to A plus B minus you should dissociation and formation. This process both, thermodynamic says life is not simple, it forms these forms, come keep cutting all the time. And equilibrium something is available to you.

So if I write G, then G is Ns Es minus TS. Already I have written sorry. Then I substitute TS from here, and H from here, so G is Ns dot Es minus kT bracketed ln N bar, N factorial. These are, this some people write this, I am writing this factorial. Is that okay? I just put this TS here and H here, so H minus TS is G. So G is Ns Cs minus kT, ln N factorial minus ln N minus N factorial minus ln. This is log, so ln A minus ln B. So this is the function, is that okay? We must evaluate the Gibbs energy which is H minus TS.

In fact the way it is, it is written delta G is equal to delta H minus T delta S, is the change in from the room temperature. But I right now did not want to take it too much in thermodynamics, I directly wrote. As to create a defect, how much energy is required? There is, for any process there is activation energy. So to create one interstitial defect or a vacancy defect, you need Es energy.

If there are N such atoms defects to be created, I need N times Es the net energy. Each ke liye S, N ke liye A. Because you are asking is why it should be multiplied. The multiplied part is something each defect will require that much energy. It is somehow Es plus 2S, this is N Es. Each atom will require that much energy, same energy cannot be used. Lattice will spend that much energy from the thermal area. So each will require Es energy to create one defect. Ns will require N times Es defects energy for total Ns defects.

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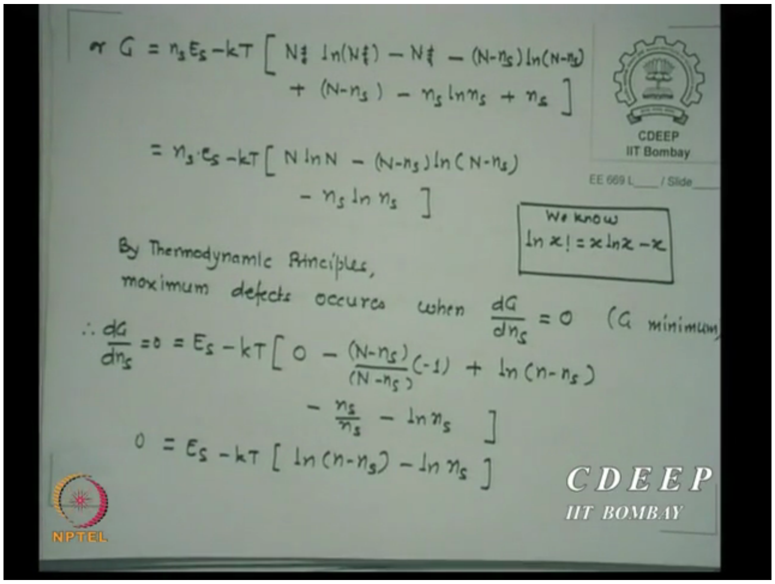

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$$\text{or } G = n_s E_s - kT\left[N\cancel{!}\,\ln(N\cancel{!}) - N\cancel{!} - (N-n_s)\ln(N-n_s) + (N-n_s) - n_s\ln n_s + n_s \right]$$

$$= n_s \cdot E_s - kT\left[N\ln N - (N-n_s)\ln(N-n_s) - n_s\ln n_s \right]$$

We know
$\ln x! = x\ln x - x$

By Thermodynamic Principles,
maximum defects occures when $\frac{dG}{dn_s} = 0$ (G minimum

$$\therefore \frac{dG}{dn_s} = 0 = E_s - kT\left[0 - \frac{(N-n_s)}{(N-n_s)}(-1) + \ln(n-n_s) - \frac{n_s}{n_s} - \ln n_s \right]$$

$$0 = E_s - kT\left[\ln(n-n_s) - \ln n_s\right]$$

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If I write, expand this, we have a maths formula which is well-known. ln x factorial is x ln nx minus x. This is a very important maths formula given in every book, maths book, tables, Google, go anywhere and books of this silicon VLSI as well. This is a formula. ln x factorial is x ln x minus x, this is known maths. So I use this to remove these factorials, solve these three terms which are going. For example, this N, N, minus N, plus N will go. Ns, Ns will go. Something some I have done this. This N and this N will go, this Ns, this Ns will go.

So I get this as my G. You can write down, I am just saying. The thermodynamic principle says the maximum defects can occur when dG by dNs is or G is minimum. All thermodynamic system wants to go the minimum energy state, so G has to be, dG by dS has to be minimum. If that happens, I differentiate this, equate it to 0. And I remove the term whichever can go.

“Professor-student conversation starts.”

Student: After that N?

Professor: Where? Oh, kaat diya meinei. Woh N factorial wahaa aaya tha, isliye. N log N minus N, okay? N log N minus N, minus N minus Ns ln N minus Ns plus N minus Ns minus Ns ln Ns plus Ns.

“Professor-student conversation ends.”

So if I differentiate this and then equate it to 0, I get Es minus kT, ln N minus Ns minus ln Ns. The other terms this is minus 1, this is plus 1, so that goes away. Only these two terms remained. So these are the two terms. What is that I am trying to do so far? What is this relation is going to look at you? I want to find Ns as a function of Es and T. I want to know how many defects I can create at a given temperature. That is the relation I am trying. I could have written day 1, this is how it is.

But I just told you how do we really do in thermodynamics. This is the way I do it. This is the way books do not want to do it. I Just want because how interesting it is to see, how actually happened. Maybe some for them, someone maybe view, I am wasting time and theirs. Maybe more theirs than mine. Since I do not have this solution from anywhere or maybe it is there, I do not see I solve myself. So I have to write all steps.

You can write this and maybe this. For me to know what is this last step, I will have to do the substitution, cutting, putting equal to 0 and then see which term goes. I gave this expression after some maths, you need not do it. You can assume that this is done. But to prove tomorrow if I would have written directly, this is equal to 0, you would have asked me how come it has. So I just thought okay, this is how it comes. Of course these are available in many old books.

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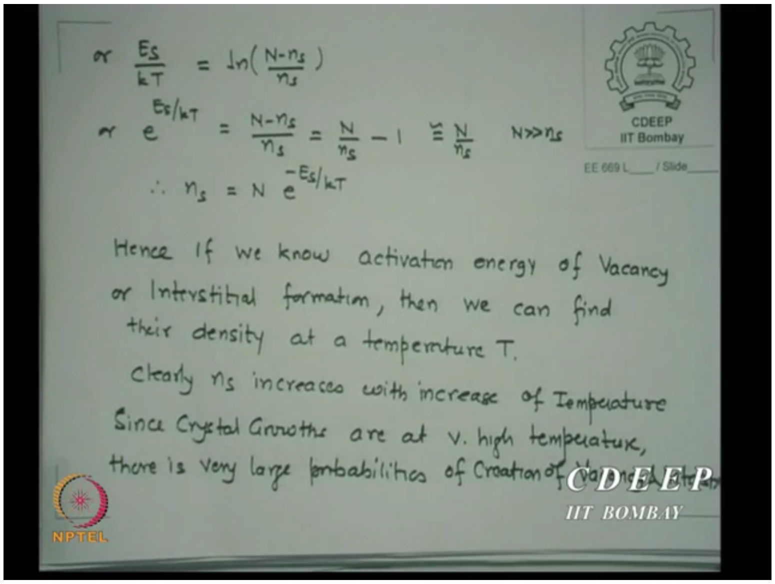


$$\text{or } \frac{E_s}{kT} = \ln\left(\frac{N-n_s}{n_s}\right)$$

$$\text{or } e^{E_s/kT} = \frac{N-n_s}{n_s} = \frac{N}{n_s} - 1 \cong \frac{N}{n_s} \quad N \gg n_s$$

$$\therefore n_s = N e^{-E_s/kT}$$

Hence if we know activation energy of Vacancy or Interstitial formation, then we can find their density at a temperature T.

Clearly ns increaces with increase of Temperature Since Crystal Growths are at v. high temperature, there is very large probabilities of Creation of [illegible]

Okay, so if I reorganize Es by kT is ln N minus Ns. I assume that the number of silicon atoms are atoms in which these defects are going to be, are larger than the defects I am creating. If I have more defect, then as I say they will not be silicon at all. So I assume any larger than Ns. If I expand this N by Ns minus 1, I neglect 1 because N by Ns is larger than 1. So it is close to N by Ns. So I write Ns is N, e to the power minus Es by kT.

So defect is one can see from this expression, available atoms N, in silicon it is 5 into 10 to power 22 for example. Es is the activation energy of vacancy or substitutional, I mean interstitial or Frenkel. Whatever is Es required to do that. So one can see what is the crux of all this. Ns will be larger if temperature is larger. e to the power minus 0 is 0 and therefore sorry, it is 1 and therefore N. All of them are as if replaced.

So T is equal to infinity. This is e to the power 0 which is 1. So at very large temperature, silicon will be replaced by impurities which what we do not. So we do not go to the that much temperature. So obviously larger the temperature, incorporation will be larger vacancies or interstitial may be available, it is interstitial vacancy will be larger. Larger the vacancy, what does that mean?

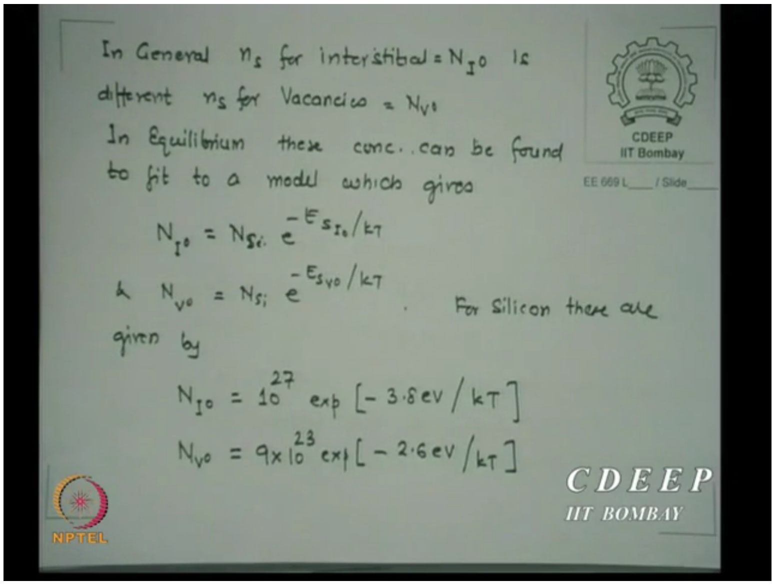
I can replace with so many impurity atom, so I can dope. So is that now clear why high temperature process required? Because I need atom space to replace, so I must create. That is why I decide. I learnt, oh, thermodynamically it must be happening. Clearly Ns increases to the increase of temperature. Since crystal growths are at very temperatures, there is a very large probability of creation of vacancies and interstitials.

And because of that there is an impurity incorporation possible. So one question always asked that, how can, how you know that they will get in so much. So at a given temperature only those many amount of impurities can be introduced. So is that fact clear to you? So why you have to increase temperatures? If I want higher doping, I must push higher temperature. Lower the temperature, lower will be doping but I do not want that.

I want lower temperature and all controlled. So I search for non-diffusive or non-solid state diffusion process where temperatures are not necessarily thermal temperatures. Thermal temperature is how much energy? kT is the energy associated. So I say, okay I will give kT energy in some other form. Why do you want only from heating? Which is the method? Plasmas. So I can create plasma which has as much energy which is equivalently high electron temperature but not system temperature. System may be 200 degree but the electron, the ion will have high energy. And therefore higher temperature. I use the same maths later and say okay, all that you wanted I did it at low temperature.

So there are processes which are trying to choose the same anyway. Because this is the only theory, how impurities can get inside. Whichever way you are providing temperature, it is yours. This is last maybe few minutes. Ek last slide, ek number dikha deta hoon.

(Refer Slide Time: 71:13)



In General n_s for interstitial $= N_{I0}$ is different n_s for Vacancies $= N_{V0}$

In Equilibrium these conc. can be found to fit to a model which gives

$$N_{I0} = N_{Si} \, e^{-E_{SI0}/kT}$$

& $N_{V0} = N_{Si} \, e^{-E_{SV0}/kT}$. For Silicon these are given by

$$N_{I0} = 10^{27} \exp\left[-3.8\,\text{ev}/kT\right]$$

$$N_{V0} = 9\times 10^{23} \exp\left[-2.6\,\text{ev}/kT\right]$$

In general Ns for interstitial sides is called NI0, I to the power 0, is different from Ns for vacancies which is Nv to the power 0. This 0 is intentionally put, it is starting vacancy concentration, starting interstitial concentrations. And there is something we will later learn. There is no just v0 but v minus, v minus minus, v plus, v plus plus. So some game I am going to play, so I right now put 0.

Some books write x, so the interstitial concentration to N silicon at that temperature, e to the power Si0 by kT, Nv0 or Nv to the power 0. Or later vacancies as they recall, Nsi e to the power Sv0 by kT. And for silicon if I substitute this N numbers, and activation energies, I get Ni0 is 10 to the power 27 exponential minus 3.8ev per kT. Nv0 is N into 10 to power 23, exponential minus 2.6ev by kT.

So which numbers seems to be larger? So interstitial sides are always larger than vacancy sides. So is that clear to you? For a given crystal or given concentration, silicon of course are used but any other specie, any other impurity, the defect and interstitials can be found. If you know the activation energy for those impurities in that material on a given temperature, I can find number of defects both interstitial and vacancies.

If I know the number, I know how many I can push in for given concentration value I am looking for. Someone want 10 to power 20. If you do process the 700, nothing will go there. So I must increase to 1,100 so that those impurities can go there. So why process has to be have temperature strong dependence is decided by availability. Is that okay?

“Professor-student conversation starts.”

Student: As a style you seems to have portrayed?

Professor: Because the activation energies are not same for both. They will not be same. This number is not very clear, this is a fit function as I call. I adjusted this number to suit some equal, otherwise this value will be smaller and this value will be correspondingly adjusted. So what I did is I readjusted to fit to a curve. So this is not mine, means many others have done it. So this is a fitting curve.

“Professor-student conversation ends.”

Please remember most modeling people what do they do? They only do this, see a curve and put A, A0 plus A1x plus A2x square. Par ye magar kisibhi chij mein fit hota hai. Hundredth order lagaoge toh all surface volume, anything can be fitted. Randomness, everything can be taken care. Large amount of program running you have to do it but it will fit finally. 1,00,0000 ton mein toh sabkuch fit ho jata hai. Shorter term mein fit karana hai toh kuch tricks lagana padataa hai. That is the way it is. Okay.