Fabrication of Silicon VLSI Circuits using the MOS technology
Professor. A N Chandorkar
Department of Electrical Engineering
Indian Institute of Technology Bombay
Lecture 05
IC Fab Labs and Fabrication of IC

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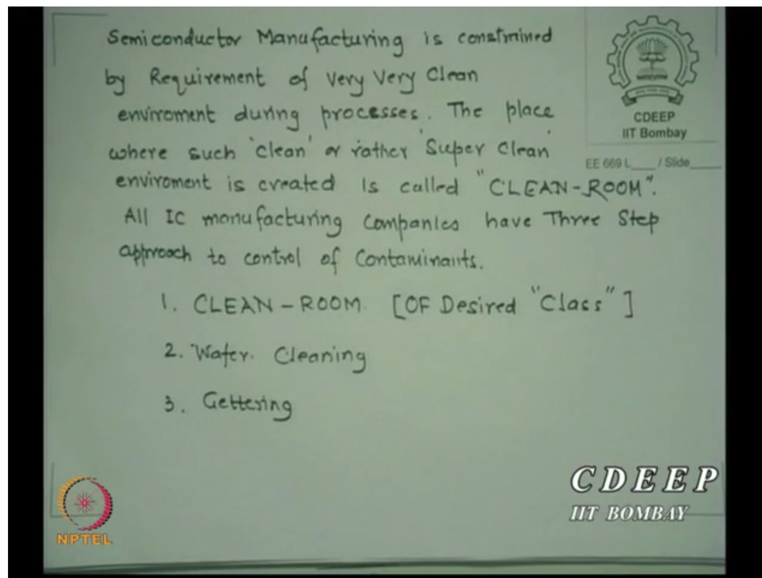

Finished other day the silicon wafers to get from company but however they manufactured and their properties. Today we start with the next something about where we actually fabricate the chips and these are called IC Fab Labs. And there is lot of constraints one gets in fabrication of ICs. Few of the things which are listed here, semiconductor manufacturing is constrained by requirement of very very clean rooms.

The environment has to be very very clean and I will give you some examples if they are not what can happen. They need not be just clean, as I said it should be super-clean. And such an environment you have to create to make an IC Fab. And today we will talk about the clean rooms and then whatever goes inside the clean room we will talk and then something about before we prepare our next processes wafers need to be cleaned and there is a standard procedure of cleaning.

And finally we will also talk if time permitting about getterings. The word getter as I say will come later but let us wait for that. So I repeat I am looking for very high class of clean area

where as we shall see what are the properties of clean rooms, how do we manufacture certain things, some things we have to be away from the normal routine in the case of whenever you are clean room. For example, typically in a clean room no more than 2 to 3 people are allowed to be in at a given time.

The reason of course is we will see later or something related to particle motion due to Brownian system. So let us talk further if you have noted down. This is not exactly given in the either any of the books. As partly it is given as I discussed but not everything. I designed first clean room of India way back in 83 to 86 or 85. So I was aware in those days what is requirement of a clean room and you want to get those items in India was very difficult.

So anyway somehow we made our first clean room in 85 and of course I do not say it was first in India by me. So things the industry had, BA had some Fab Lab, so semiconductor complex started in Chandigarh but they were industries. No university boosted any IC Lab till that time and we were the first to actually create IC Fab area. So something which I have learned over the years may be of interest.

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So what is problem in a normal room? Normal room has lot many contaminants and they may be classified as particles, surface contaminants and molecular contaminants. So there are three kinds of contaminants are seen in area any volume of space. And as I say if we want to fab a chip, then

we need to somehow control all of them. Here are some list of contaminations given. Particle contamination is major source, are the people working in the IC Lab, I just now said.

So if you want to go inside the lab and you also want to work, then that goes against the clean room requirement. So that is why many people do not want to work because then the clean room will be cleaned. But that is not the purpose. So limited people should be inside. The second, part of the people who, part of the things which come from people are skin's perspirations. We perspire a lot many times, not everyone but many, almost everyone but larger or smaller.

And it contains lot of sodium. So one of the major contaminant which human body gives is sodium. Second are here, here are the (())(04:58) particles. So if you even go to a normal good looking hotel, these days people wear caps. Simple reason, the largest amount of contaminants come from hair. Then there are whatever we wear, clothings, they have some small looms early on and they float when the air comes.

So clothing lints, these are the major source of contaminant from person. Even wood, we cannot live without wood or particle bores or maybe polish boards or everything in making of a lab. But in that case they are the source of contaminants or particles. Actually machine which saws or sand bursting or drilling can cause particle flow and these are the other contaminants. So first thing we will have to look into making a clean room is how to actually reduce this particle contamination.

And we see that there are ways of doing it and that is what the word is clean room. So first thing is clear that I want to reduce somehow particles which are floating around and as I say other day typically this room is slightly air-conditioned, slightly closed. So it may be 1 billion class of room which essentially is trying to say it is 1 billion 0.5 micron particle floating per FCFT per cubic feet. We will come to numbers.

So we are talking of billion particle per cubic feet and the class of room which I am looking for is class I or better and M1 as it is called or even M2s. So we are looking for particle removals in large numbers and we will see how do we do that. So first is particles.

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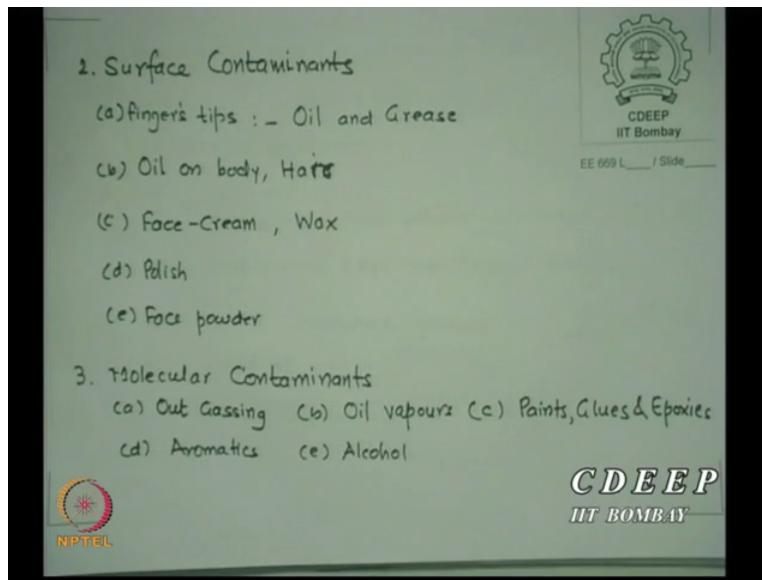

The second is surface contaminants. Finger tips, we all have where we use fingers by design or otherwise we get some oil or grease on our finger tips. Then from the body itself there will be oil or from here there will be oil. This actually stick to surface of a wafer or around it gets into over it by floating in the air but gets attached to silicon. Polish, polish is something (())(07:41) and facial powder as I say.

The fairer sex are not allowed to use any nail polish or any face powder or any facial during the work inside the camp, inside the clean rooms because they are the contaminants which sits on the silicon surface. The third of course is molecular contaminants. Lot many gassing, gases coming out inside the system, near the system. For example, there is some kind of evaporation system for electron beam or sputtering system.

They have pumps, which are firstly, first pump be diffusion pump and below that is rotary pump. All uses some kind of oil and they heat and the oil vapors are available even inside a clean room. We try to reduce or balkanize certain area so that those vapors do not come to other areas. But there is vapor flow all along due to the system itself. Then there are wall paintings, paints on the walls, so it leaves epoxies. Aromatics, alcohols, all these things are molecular contaminants. They are available in larger amount in many places and one has to take care that these are minimized during the creation of a clean room as well as during the fab of the chip. So I repeat first is particle contaminant, the second is surface contaminant, third are molecular contaminant.

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4. Inorganic & Organic Contamination due to equipments and Reagents in Lab.

(a) Heavy Metals – Stainless Steel Pipes, Furnace front ends, other metallic impurities from Reagents

(b) From Water, Human prespiration and air, one gets Alkali Ions who occupy Silicon surface. Na^+ and K^+ are likely alkali ions in the lab.

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The same number, the same name and now little different name I gave you because though they are part of any other, but there are two kinds of contaminants we see mostly in equipments and reagents. These are either inorganic or organic. Now there are heavy metals. We use stainless steel everywhere though it is best possible material which does not give enough particle contamination but it does give you some contamination which is oxides.

Then there are pipe we use. Furnace front ends are there. Other metallic impurities present in reagents, all create some metals inside your solutions or inside your furnaces and these are sometimes as we shall see may be killing actually your device performance. From water, human perspiration, air as I just now said or inorganic materials like alkali ions which can occupy silicon surface. And most likely alkali ions which are seen on inside a clean room even if it is clean, the sodium and potassium, mostly sodium, partly potassium.

So one question is arising that is that really affecting so much that you are worried about making a clean room which may cost a billion dollars, total area of say large fab, not small lab. Our maybe around 50 crores to 100 crores, our new fab lab which is nano-lab now it is called.

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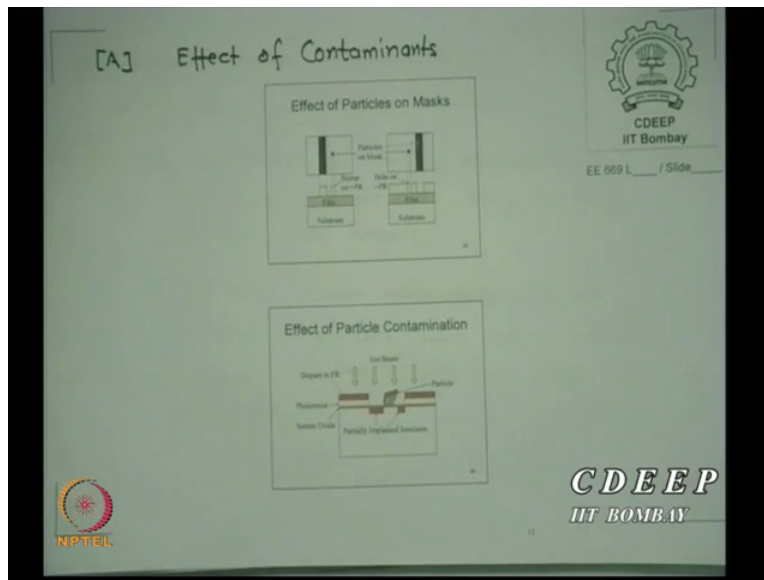

Now the question arises why are we so worried about contaminants. So there are two foils. Of course I do not know whether it is, yeah, I do not know because it is taken from a book or rather paper, so it is not very good but maybe I will explain you. There is something called a mask which we have not yet discussed, either a gas plate or some other form on which pattern is created, is like a photo plate on which patterns are. Some is white region, some are black regions.

So what happens? Here is a mask plate which has this region black. So if I have a film over which photoresist is coated, I said the last time some photoresist when receive light actually either become hard or soft depending on PPR or NPR kind they are. However if there is a black portion, the light will not pass through. So the expectation is that if there is a particle next door or next to that black portion, particle is also opaque in most cases.

So light will also not pass through that. So the pattern which is getting printed on a resist now because hard and soft areas will be additional and the spot will come there. Either it will be etched out or retained whichever resist is used. Similarly there is a possibility that the particle may slip on the dark area and that portion may actually be opaque. They are particles, quartz particle for example, they are translucent.

Some light may pass through it. So the below there may be some portion cut out, some portion, additional portion may be blocked or cut out. And this means whatever pattern I was transferring does not get transferred when I go from mask plate, when I expose it on resist, everything what is

on the mask does not really go because of contaminant. It can also have a problem that the contaminant may sit on the resist itself and even then it could create the same problems.

So contaminant particle size, now question is how small this particle size will be. In say, 14 nanometer node or maybe 11 nanometer or maybe 0 nanometer later. The particle size is at least around 0.5 micron alone, maybe 0.05 smallest particle known. And if dimension are of the same size, so it may happen maybe here itself.

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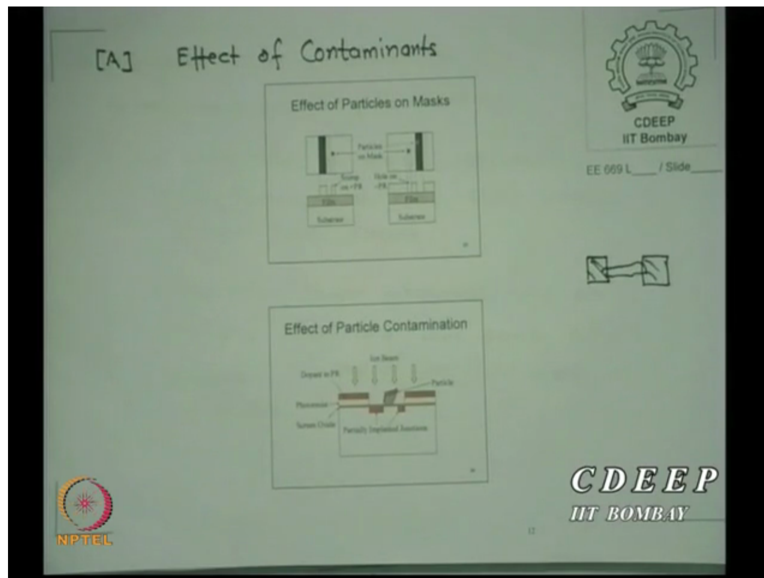

I have two metal areas which I was having but and this gap is also of same order and a particle sits like this during resist. Now when I metalize, the two metal plates get shorted simply because metal also goes along with that. So you thought that two lines are separated by you but in fact they are shortened. This comes more at edges as we shall see in real life. So there is a problem with the actual reliability issue.

If number of particles are floating too high, there is more chances of shorting or opening of the areas without you knowing unless you see finally wafer is not, chips are not working. So these, this is one major worry which we say particle contaminations. For example, the way impurities are incorporated in the silicon these days is by process called ion implantation, high energy ion beams are bombarded on the wafer.

The resist normally acts like a good mask, so no resist, implant can go through this. However this was the window where I was trying to implant certain impurities. Let us say this was P type semiconductor and I am doing phosphorus implant or arsenic implant. However there is a particle sitting in that so called window. Implant cannot then go through this, it may actually scatter from there and may even give something called strontium as radioactive material sometimes if the metals are of that kind, molybdenum for example.

Now what happens, that this particle has actually, we have total end region to be created and you found certainly two end regions and open between the two which you thought that I did everything correct but there is nothing working. The mask and this channel is broken down let us say somewhere. There is N type you had, there is implanted N type in between the P, so there is some kind of depletion channel things have appeared before even you started doing invasions. So there are issues which are very crucial in actual device performance. So these are particle contaminants which lead to failure of circuits or failure of device.

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There is another worry particularly for people in the (mem), as I earlier said the technologies are normally specified three ways these days. One is processor market or processor technology, then the other is T-RAM or memory technology and third of course is a flash. So most of the research is in these three areas, flash, memories of DRAM, SRAM, CAMS and the rest of course is in logic which is normal what we discuss.

So if you look at DRAM performance, I hope some of you know or your next course in design I should talk about. A typical DRAM has 1 excess transistor and a capacitor which stores the charge which stores 1 or 0. If there is a charge on this capacitor, we say 1, if there is no charge, we say 0. So this is the word line, x line and this is my Bit line. So if I am accessing it, then this turned on because I turn on this word line. So this capacitor shares charge with Bit line capacitants.

And depending on this voltage on the Bit line, I can sense it was 1 or 0. Now the problem is when I am not accessing. Even if I am not accessing, I find there are two ways charge is lost and that is why DRAMs required refresh cycle. Every now and then whether you read it or you do not read it, whether you access or do not access it, the charge is lost from the capacitor and because of that your 1 may not become, 1 may not remain 1. It for a long that bit is never exercised.

Now this is a very serious problem and that is why there is a refresh has to go through which means during the refresh cycle you are not writing or reading anything. That means there is a slower down of the total cycle of DRAM because every certain number of this you have to come back and refresh all of it again. If it is 256 G memory, we can think how much large time it will take to refresh all of bits.

Of course there are faster way of writing. But all said and done you need refresh on that. And refresh cannot be selected, refresh has to be through, through and through. So there is a time required. Typically it may require around 1 millisecond, every millisecond you should have to come and refresh. There is excess time maybe in tens of nanoseconds or 30 nanoseconds. Now why this happens?

As I say there is a leakage in the capacitor and there is a leakage in the so called transistor because of the junction sitting in mass transistor they actually leak. Whether you like or you do not, there is a reverse-wise current. Also the threshold which you thought is very correct threshold, is not very correct. There is a sub-threshold current also flows in the device. So there is a leakage due to junction, there is (())(19:47) currents.

There is a leakage in the capacitor. All and all finally charge is lost and therefore you say you need re-refresh away. Now replenish this charge you require to generate for example, in a

capacitants large amount of carrier should be generated back so that it comes back to the level you want. So there is a time associated with refresh cycle or even access cycle also, is called generation time which is equally normally the recombination time.

In the case of transistors, it is recombination which generates this junction currents. So this called shockley-read-hall mechanisms which leads to junction leakages. Now these are major worries, so you are worried about the recombination time and equivalently the generation time. Larger the generation time, that means charge is retained this much more because you have much more time to adjust the charge. And therefore you will have much smaller other times or this. Now from there this SRH mechanisms or leakage mechanism occurs, is essentially because of what we call as traps.

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The SRH mechanism is dominated due to Presence of Traps in Silicon. We know

$$\tau_R = \tau_G = \frac{1}{\sigma v_{th} \cdot N_t}$$

E_c

E_t

E_v

where N_t is Trap Density

for $\tau_R = \tau_G \geq 100\ \mu s \sim 1$ (or even higher) msec

Min $\tau_R = \tau_G$ as per SIA standards should be $\geq 25\ \mu sec$

For $v_{th} = 10^7$ cm/sec in Silicon, with Capture Cross Section σ of the order of 10^{-15}, the Trap density N_t be $\simeq 10^{12}$/cc. (0.02 ppb). Typical traps availability are due to Na^+, K^+, Au and Fe as well as Cu. First two Na^+ & K^+ are mobile ions on the Surface

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SRH mechanism, there say shockley-read-hall mechanism is dominated due to presence of traps in silicon. Trap essentially gives energy level in the band gap of any material, particularly in silicon it may be close to half Eg y or Eg y2. Closer to the Ei, larger is the trap current. Both whole electrons can have probability to reach Et faster and therefore recombine. So if you look at recombination times, it is essentially given by sigma Vth Nt, inverse of that where Nt is the number of, or is trap density or number per centimeter square.

And by semiconductor industry standards tau R, tau G should be greater than 25 microsecond. And if I know capture cross-section of the most materials, most systems which I, what is capture

transmission? The area which a carrier actually sees before getting trapped is called capture cross-section, some other day in physics course or Professor Vasi will be more happy and much more serious about telling the trap problems.

So the capture cross-section is typically 10 to the power minus 15 and if I calculate back the minimum required tau G or tau R, then each trap should be around 10 to the power 12 per centimeter square or per cc. Now typical silicon doping is 10 to the power 14 above and traps are around 10 to the power 12 which is around 0.02 part per billion. Now traps are because of what? There are many materials like iron, copper, gold, they are present there and there are other two, sodium and kalium.

They are essentially not so much in the band gap, in the mid gap, they are closer to the surface either mostly towards conduction band and these are ions. So these are the possible impurities and as I say when I showed you the list of contaminants, I did show you all of them are contaminants for us. And if they are present there, Nt may increase and if Nt increases, tau G or tau R also goes down.

That means your refresh has to be not milliseconds but maybe 100 microsecond and in worst case maybe every microsecond. Before you excessive read, first write. Then why do, if you have to every time write and then read, then as well directly you can read the data. And why memory? Memory is kept because you do not want to write every now and then, store something. So the very purpose of memory will be lost if you require refresh cycle every microsecond or every nanosecond, tens of nanosecond.

Excess time is 30 nanosecond and you write also every 30 nanosecond, then why write? Read directly from wherever you were transferring data. So the game is that this refresh cycle has to have larger time, therefore trap should be very very small numbers, less than 10 to the power 12 possible which means the processing has to see that these are not present in the silicon area anywhere around so that they just get in touch and sit there in any reason.

These may come even from the solutions or gases we produce, so they also should be pure enough that they do not introduce these many impurities. So these are very crucial problems which many people are worried about and particularly with 4G and above 256 GB RAMs this is

becoming a very serious issue. Of course there are very interesting new technologies that come in DRAMs, so we do not right now want to use single transistor DRAMs.

We are going back to 3 transistor DRAMs for variety of reasons. Some other course, some other day. This third part as I say sodium, potassium which I did not want to club there but I wrote. Alkali ions and they particularly are part of silicon dioxide (())(25:29). Now if you see the gate oxide of a mask transistor which is the major material which makes mask transistor go, it is essentially we say gate oxide threshold if you write either N or P type, it is work function difference.

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[C] Alkali ions (Mobile Ions) can get incorporated in Gate-Oxide of MOS structure. This may give variable V_T

$$V_{T_{n,p}} = \pm\phi_{ms} \pm 2\phi_F - \frac{Q_B + Q_{ox} + Q_m + Q_{it}}{C_{ox}}$$

Q_M is Mobile Ion (like Na^+) density in col/cm^2

Clearly if Q_M varies due to mobile ion movement, then V_T also varies proporationately.

PBTI and NBTI are known worries in MOS Flash ROMs.

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For the potential twice, there from potential Q any Ni by, Ne by Ni or Nd by Ni. KT by Qln, Ne by Ni or Nd by Ni, plus or minus will sign come accordingly. Then there is a bulk charges because those doping in the silicon substrate concentration, QB, QA, Na, Xd. Xd is depletion layer, so this is related to dopings. These are charges which are available, fixed charges which are already available.

They in other term which one can add and maybe Professor Vasi is the, he will be so very happy to see this number. In the best states they also contribute very well charged. Why I keep saying Professor Vasi? Because for 40 years he is with mass surfaces. Recently two years ago he changed to photovoltaic. But otherwise his research interest and his personal problem matched here.

He has been working on mass surface systems for 35-40 years. So I think he may be the number one person all over world maybe, I do not know, many I shifted now. I left it in 90s but I think he continued. So Qm is the mobile charge. What is mobile? Sodium and potassium, then enter into the oxide area or volume. They actually are not fully bonded to SiO2 lattice. Since they are not bonded or even if they are what is called electrovalent linkage, bond is very weak and sodium is released very fast.

Little temperature and sodium will come out. So sodium even at room temperature or at least 30-40 or 50 degree centigrade is extremely mobile. It has large mobility. So depending on mass structure, this is your oxide, this is your silicon, this is your metal and let us say this is Na plus. Let us say I have a negative terminal here and positive to this, minus VJS I am applying let us say. So most of the sodium may come towards metal.

But if I put plus here and minus here, which is plus VJS, in this case sodium will be close to the silicon surface and when I calculate a threshold whatever charges are available at the interface of oxide and silicon was taken care and that is the numbers these charges are actually, very close to the surface. Since the metal then will be very, these alkali ions will be very close to the surface, they are charged species and because of that BT will actually be affected by Qm by C of sum. This is the calculation some course can do that.

Since the temperature varies, VJS varies because they turning on-off device. So it is not that fixed temperature or fixed voltages will appear. So this sodium will be actually moving in the oxide. If they move, the Qm value at a given surface point is time dependent which means threshold is time dependent which essentially means I was doing some logic, suddenly I find the time of charging of that output load is (())(29:27) sudden.

Where is an ion any, nothing, I think I applied same bias, it did not work. Then I figured out old metal heated, so they must have really pushed in or pushed out. So this is called instability. And there are two words which we use in most cases. Positive biased temperature instability and negative biased temperature instability, particularly for flash ROMs this is becoming a major worry and BTI specifically.

And because in the case of ROMs what is the way we do it? We have a Bit line which is charged to a voltage, we have a EPROM cell or E square PROM cell and we are putting some gate

voltage to actually ride. And we assume that the threshold of this transistor is either enhanced or decreased. And if it is enhanced, then nothing, not access to the output. If it is smaller, it has an access to the Bit line.

This is how 10 are read there. Now the BT varies. One does not know whether Bit line gets connected or does not get connected even if it wants or it does not want. So there is a issue in a flash ROM that particularly because flash voltages are coming down, this may actually dominate. The sodium contamination may actually dominate. So we are extremely worried in case of flash to get this so called temperature instability reduced and that is why contaminants like sodium, potassium and other kinds should be minimized.

Why I always give this? Actually I think even Plummer talks about, he is also electrical person. So we all believe that we have reasons to think why we are doing something because electrically it will affect us at the end. If it does not affect, who cares? Even if it is dusty area, who cares if my chips are working well without any problem, I will not dare to do anything on that. But I figured out nothing works, then I will have to solve problem. That is how we do. So this is you must have understood that why we are so much worried.

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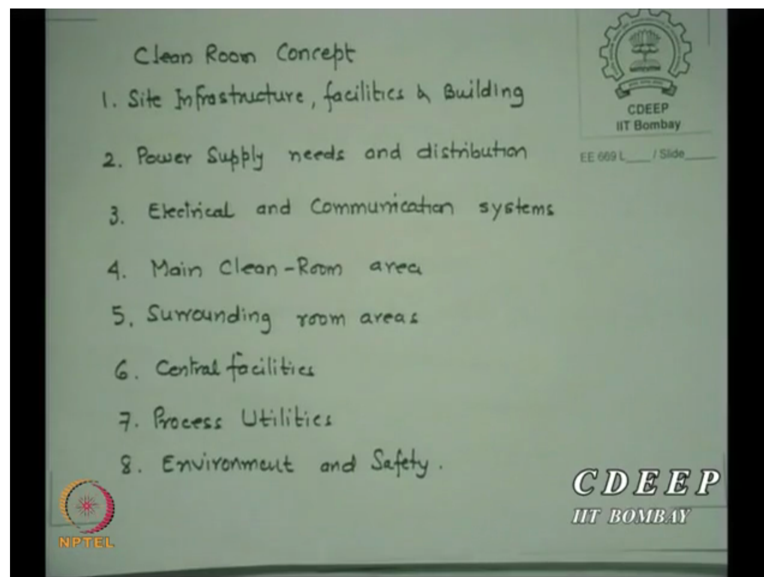

There is a clean room concept. Site infrastructure, facilities and building are, has to be taken care designing a clean room. You also need to think about power supplies and their distribution. Some are, standard power supplies can be 230 lines you need, 60 volt line you need. Many equipment

need 60 volt. So stabilized or non-stabilized, both kinds of sources are required. Distribution is very important. Prior we have to decide where power is to be required. So which equipment will be there, how much power will be required, that kind of lines have to be put.

So power supply design is the major design in case of a clean room. Because once clean room is created, nothing can be changed. It is very expensive to change anything. And there is also a system which needs communication from outside. Of course is telephone is probably but even telephones box itself is a contaminant. So we like to avoid it as much but we also want a system in which I can talk.

So there is a membrane kind of throughput which is sealed from both side but membrane vibrates. So I talk and answer person can listen it. So these are membrane blocks which essentially can allow you actual talking without any connections. But of course telephones are still used, blocked very way so (())(33:17). Then we have to worry about, there will be large area where you think you are going to artifact but there will be some area which will be ultra-clean which is called main clean room area.

Also we have to worry about side areas which is feeding this main thing. For example, this gallery outside, how much it will affect us is very strong dependent because if that is two particle content, then the diffusion may actually come inside. Then we need lot of central facilities, gas supplies, liner, many other hundreds of things we have to supply in. Then we need process utilities. You may have furnaces, welding machines, so many machines with a vapid room. So many facilities inside a clean room. That is why the purpose of making a chip, if they are not there, how do you make a chip?

So we need to then, so must take care how much thermal load they will create, how much area contaminant they are going to give and which area they should be kept so that their dirty things do not go too far. And of course one will be always worried about environments. Because if I release gases in the air, I may survive inside but someone outside this building or outside this IIT may also get affected, may die in one case, some cases.

Arsine for example if it is released, 30 percent of the people in first 50 meters will die before they know that what is happening. So that is very important in making designs. This is just to

give idea because this is what I took care when 30 years ago. Of course over the years same things have changed but not much.

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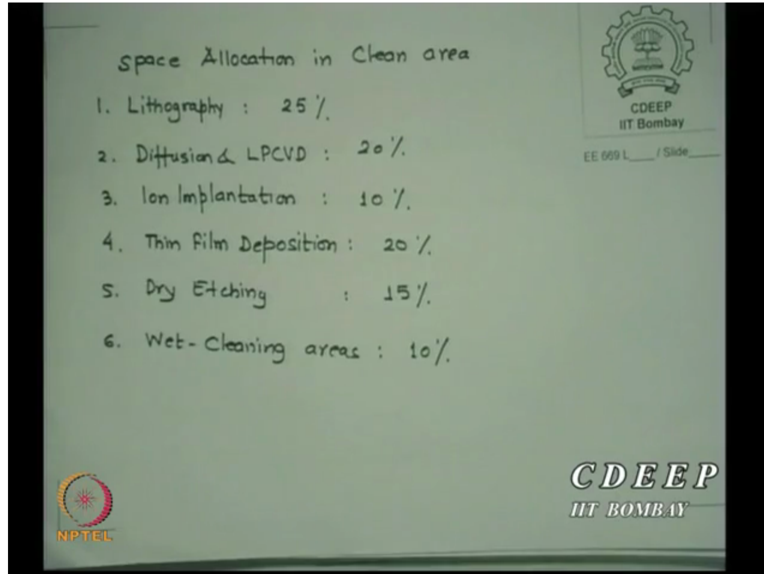

We also have to decide how much area each will have. lithography should be around 25 percent, diffusion LPCVD should be 20 percent, implantation may be 10 percent, thin film that is EBIB depositions, etching and sputtering it should have occupied 20 percent. Dry etching area may be 15 percent, wet cleaning areas may be 10 percent. So we actually distribute areas also where which areas what we are going to keep and we are going to see that these too much area because each has contaminant giving problems.

So you must mark your areas where you will keep where and how much is the area you will allocate. As I say these numbers are mine and may vary from Intel Lab to TI lab to other labs, even our own lab. But this is typical numbers which one, Ciasons have designed it. I thought I will inform you that person has to take care even if you are electrical person. And you are making a lab for which you are going to work there. Do not believe that chemical engineers will do as good a job unless you are around. So someone has to keep telling him, this is what I want. This is typical area, they say these have no meaning but it is just to say you that we divide certain areas for certain work.

“Professor-student conversation starts.”

Student: Sir, how do you decide the percentage like……?

Professor: Yeah. Firstly the sizes of the equipments.

Student: But does not that there is no abort?

Professor: No, other is like for example, diffusion furnaces actually reduce too much of gases. They do exhaust and but there is a thermal currents which keep flowing there. So if that area is too small, then there is a possibility that it will diffuse, go faster other end. So I want to remove heat right there. So I keep little larger area so that power density, thermal density reduces. So each has some reason.

"Professor-student conversation ends."

I may, as I say these are not specifically accurate here. But typically given by the sizes and the outgassing or out-products they give, one has to decide area. It is okay. Many times these have to be thrown out because this is the lab given by institute, this is the area. Now you put your brains how does you can achieve in this what. But if you have given a space, I will like to divide it properly.

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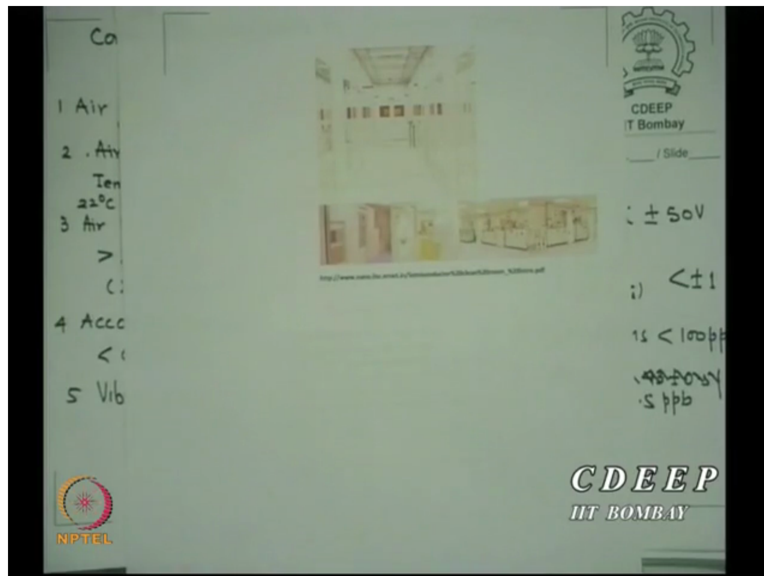

Before I quit, I mean finish this, there is a side given to them. This is the center of excellence in nano-water we have. 50 percent of that center is in IISc Bangalore. We shared the money, we

shared the work as well. So this is taken from there. I think (doct) Professor Anil and Professor Vijayraghavan have actually created a video, I have not seen it but hopefully it is there. Or I give you, this is http www.nano.iisc.admin.in/semiconductor clean rooms intro pdf. This is the Vijayraghvan, PM Vijayraghvan.

www.nano.iisc.admin.in/semiconductor clean rooms entropy.pdf. That PDF has this problem. You cannot copy it, so I could not. Otherwise I would have copied partly from this site itself but this is just some word printout and it is not coming good in colors. But you can still see some way, this is the corridor. Both side you have rooms which are gas paneled everywhere. These are the furnaces, other systems kept there. This is the clean area for lithography. So we do have areas which are marked for each activity. Is that clear? Yes. So this site, as I say please receive it.

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Hopefully they have better, maybe today I may also see it but I ask Anil, so he thinks that, he told me he has put it. Of course this is not his slide. This is from some other paper. You can see from here the central area is the most clean area, class 1 as the word written there, class 1. There are central area which is the cleanest area and you can see outside that central area is called equipment area and which is class 1000.

Now this class word we will define soon. Then there are process tools, pumps, this, everything. The major thing which you should look into is the three top areas. This, this, this, now these are essentially you can see filters kept there. Even here there are filters. Of course they are side

filters but on the top there are filters. So when the air comes, they are filtered down and goes down actually.

These filters essentially decides the class of clean room you actually make. So we need air filters, what particles you can allow from the air to get in. After you can lose out air, so you have to survive. So you said block all air, then contaminant will be 0, so you will be not there. If you have to be there, you need air. So survival also needs, as you need survival, so we do that. For example, this you can see the process tools and one person is standing on this.

So the front of the furnace or which of this is only visible inside the main clean area where wafer would be actually opened. The back portion goes into class 1000 area because that area may, is not very much used for silicon opening. So that is how we say, so gradient at least should be 1000 to 1. 1000, just outside the furnaces are sitting. The front end of the furnace actually goes inside the clean room, the rest is closed from around.

So only furnace end is seen now. Now these HEPA filters as we shall see soon. So what are the contaminant control we need? We need to have, look for filters. We need to have air-conditioning because we need temperature and humidity control. Typically in a clean room 22 degree centigrade is the temperature maintained. 40 percent relative humidity is, and some areas may have 45 percent, some may 40. Lithography should have as low, possibly 40 or even lower if possible.

Please remember temperature and humidity goes against each other. Larger the temperature, humidity is much less, relative humidity. So if you increase the temperature to 30 degree, obviously humidity may go 10 percent. But then you cannot, particles will start floating because Brownian motion will be very high. So you have to cool and you cannot cool too low because again you will feel chilled and you may not be able to work.

So 20 to 22 is the range up to which we normally survive and that is the temperature at which most of the clean rooms are maintained. There is air pressure inside, forward pressure is maintained which is 30 Pascal. I think some other day I will give, there are number of units for vacuum as well as pressure as I say. Foot per square inch is one but there are others, star, bars, Pascals, many others, five of them.

But they give some relationship and we will talk about system where pars pressure. So this is the up to part or (())(42:59) or something. So if you have air pressure, should be larger than 30 Pascals or 1 to 5 torque. Sudden 60 torque is atmosphere. So acoustic noise in another area, it should be less than 60 db. This is what Supreme Court also says, less than 60 db. So the same number should be inside clean room. So no speeches, no loudspeakers.

Of course you can play what are some, I do not know but that was not there in my time. So I do not know how much vibration and noise pollution it gives. Typical vibration system should be very stable. As I say we are looking for platforms because the wafer is going to shift and if it vibrates with some numbers, then it can never align with anything. So either the relative vibration should be same, 0 or we should have vibrations as small as possible. 3 microns per second is all that we are looking for.

There is electrostatic discharge, there is because of the nature whenever we touch, we provide some voltage, electrostatic voltage. Typically it can be human body can be, 1500 volts. Whereas we are expecting ESD is less than 50 volt. We also do not want any magnetic fields, it should be less than 1 milligauss. Because many of their materials are affected by magnetic fields. We need, do not want to any hydrocarbons less than 100 ppb, preferably 10 ppb.

And there are many other contaminants whatever it is should be less than 0.5 ppb. So this is kind of clean room requirements and you get in. And this is the kind of main area, these are the filter areas through which air is coming down. Air is coming from air-conditioner and there are many filters, micro filters and HEPA filters. So air, now this is an issue which is important because if I have 3 levels of filtering before the air is pushed in, the pressure which I am building from the system side, from the pressure side has to be such that the air has either sufficient flow or not very large amount of flow.

If you have a large amount of flow, then the particles will also come with that. They move with that. If you have too little, this is coming in, it also it creates a problem that air is, some globules of air is formed. So that is not allowed, it is called sucking systems, it is in-between.

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The major thing which we look into is essentially called, if the air is coming from here, it should flow exactly vertically down without any of the layers of air actually interacting with it. This is called laminar flow. So there is some, if you are aeronautics person, this is the standard Reynold number which decide the some kind of flow system. It should be small enough so that they are not distributing themselves, air do not interact, so the air particles do not flow out.

They remain vertically down and also if this is my edge, air comes and comes out and it does not go towards silicon side. So these are some requirements. We also look at it that the class 1000 as which through this has lower cost, there are no walls. Then the boards are put, better than class and environment and process tools are inside and there should be then the problem starts. Your other equipment is outside this clean area but you will have to carry your wafers inside the clean area.

So either they should be, you should carry but then you are the dirtiest around. So you are carrying with all your dirt around. So you must pass inside. So there are called pass boxes which are air sealed as class 1, you have seen, as they are called. You release the pressure, the box internally opens. You put the box in, close it, then I will open it, take the box out. So this is all transferred boxes areas are also possible.

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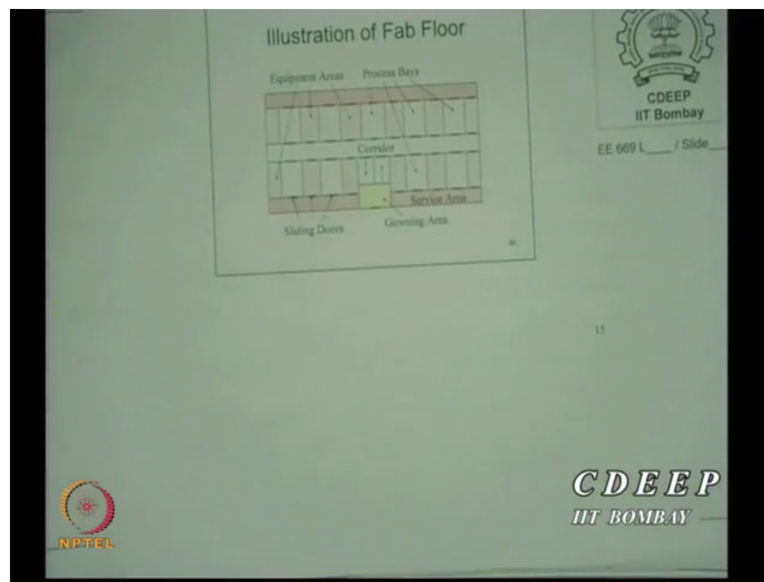

The HEPA stand for high efficiency particulate air filter, they are typically of the sizes of 0.01 micron, 0.05 and even 0.5. Particle sizes are not 0.5, and 5 microns. They can be large particles. When I say it is 0.05 HEPA, I am actually talking, these nines you should now learn. In the semiconductor technology or any technology we always talk about nines. 8 nines, 8 nines means 99.69 nines, 99.999999 is called 8 nines.

So you need 8 nine percent or 0.08 micron be removed when I say it is 0.05 HEPA. These many of this kind should get out. Then there is another HEPA which is 0.01 which is 6 nine percentage of 0.04 particle removed. So that is the HEPA part. Many clean room nowadays on the wall HEPAs because of much more air you want and much more laminar system you want to create certainly.

You want horizontal laminar, you may have filter. When the air comes from down, upward and goes down, you must understand there must be something a return air path from where air will go. So there must be some kind of system where air is pushed, pulled in and taken out. These are called return air paths. So air is coming down and you actually suck it from the bottom and that is path return.

Every AC cycle should have 30 percent fresh air. Every fresh, this 30 percent fresh air is pushed in, 30 percentage because otherwise heat becomes higher and higher. The compressor may not work, compressor may not work. These are called return paths which is very important. A typical

cross-section, I mean the planned area one can see from here. These are racks, grown racks. These are the actual benches on which systems are kept.

Then there are shelf of gloves, shelf of this. Before you enter inside, you must wear what is called as bungie. This is made of terylene, bungie suit which is completely covering yourself. And as I say humans are the worst, so first thing you cover yourself, tie it up yourself. Use goggles, sometimes in many companies you need triple goggles as they call or hair should be completely invisible. So you do not know who is inside actually when you see the person.

Only by height roughly you know, otherwise you do not know who is he or she. So there is an entrance where you go through a shower, a small area, you first enter there, one gate is closed, one gate is open. You enter here, there the gate goes and there is a huge HEPA filter all around you and a large amount of air is pushed on you. So all the part, and then there is a grill below. So if the grill below, all the particles sit below the grills and you actually get completely dry washed. So that is how you enter the lab.

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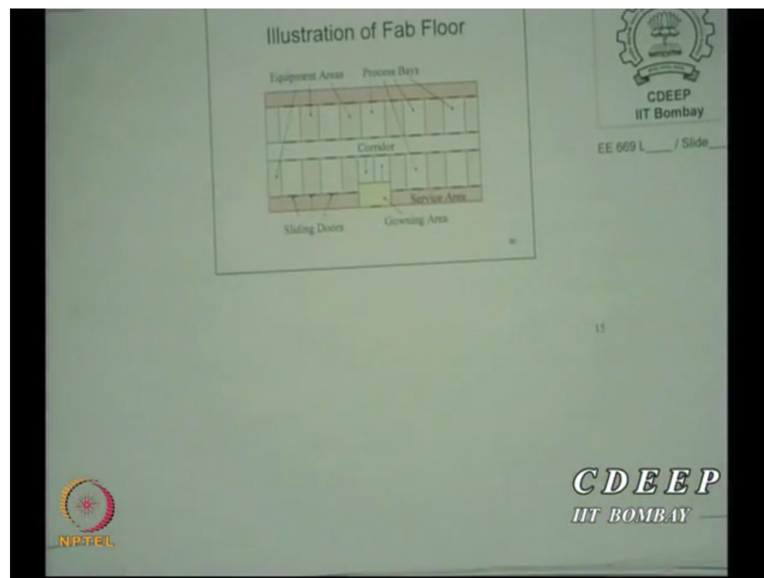

The same area which I have shown you as larger this.

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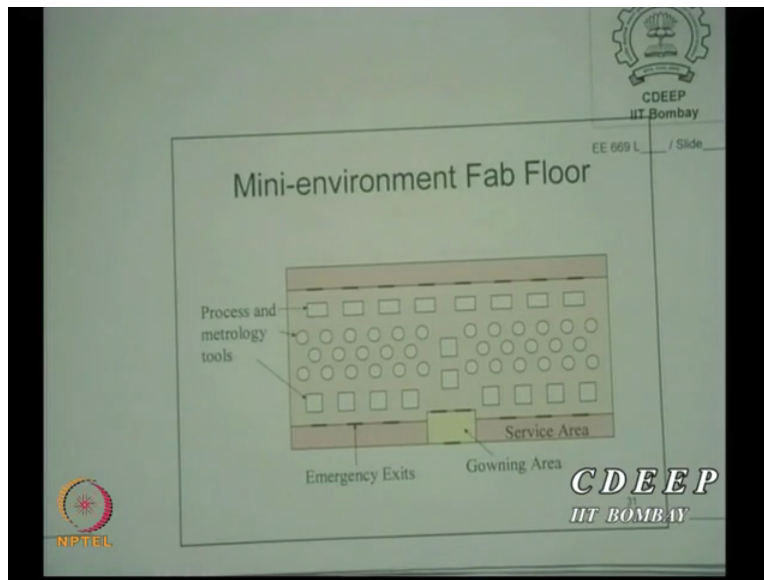

This is something more important. The lower part of the labs normally has small holes or grills as they called and the air actually is pushed down. You actually walk around 6 inches grills, so you walk thak-thak-thak on that. There is as I say, these are only, and the areas around this are called service areas where cylinders, every other things are kept backside. That itself should be at least, cross 10,000.

So this is mini-environment for fab floor. These are the tools which you are working at. There are also emergency exits. Many time there will be 6 in larger areas, at least 2 in a normal. If you see in other lab, there will be only 1.

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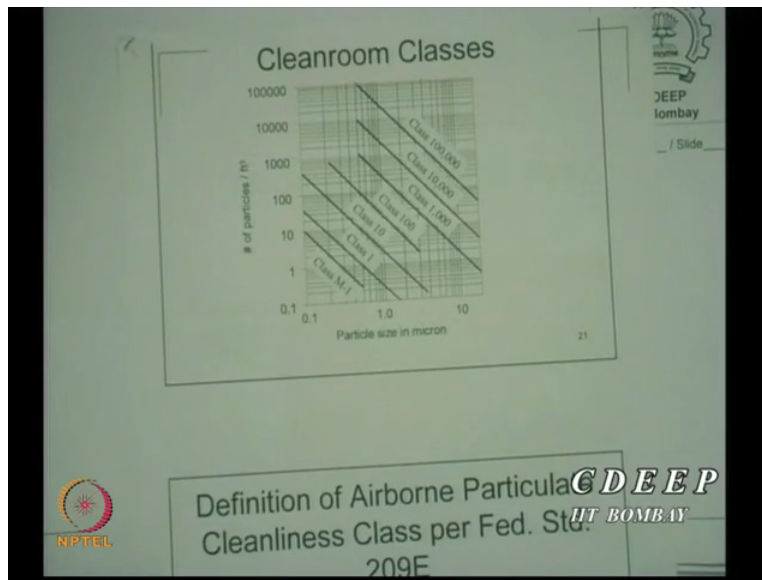

This is the class of rooms which I discussed for all along. Typically this class is specified by a number of ways. One is 209 East Federal standards which is American standard and there is a British standard and there is a non-British, non-American standard which is what most people agree. This is called class of room. Typical this number which we are talking, class 1000, 10,000 is the number of 0.5 micron particles per cubic feet.

This is, should be understood per cubic feet. VLSI technology is the only area where we work on both FPS and MKS system together or CGS system together. We specify something in micron and the area sometime in mills, milli-inches, so classwise. So CFT is volume by feet, 1 feet, 1 feet, 1 feet and how many particles? So class 10,000, 0.5 micron particle has 10,000 such particles. Class 1 has 0.5 particles, is around 1 particle. And there is a class M1 which is lower than that and can go even lower than 0.1 microns.

This is, actually M10 is the latest one now which essentially is even better, is used for below 16 nanometer tech-nodes actually. So we can see we are the people and right now as I say this may be class billion, so you are talking of 0.5 micron particle have billion numbers per CFT floating here with air-conditioners. If you remove air-conditioner, it become trillions. So also you must know, when I move my hand from say 1 feet, I move at least 10 lakhs or 1 million particles.

1 feet I move hand, 1 million particles I move. So your motion in the lab also has to be restricted or number of particle itself should be small enough, so they do not move. All tricks of the trade.

So typically as I say we are looking for class or sub-class 1 clean rooms. The reason why we are looking for this less than 0.05 now, because these are the feature sizes we are working on and anything particle which is of same size and same numbers, then the nothing will come out. So features has to be taken into considerations. However all said and done, as I keep saying nature sometimes works for you. Some unknown which you do not know actually helps you out. So something happen good, so company survives unknowingly.

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This is Federal standard 209. In electron, there are too many standards. For example, military have standard 801, 803, 833, so many specifications they will give you. Space has its own standards, clean rooms are with own standards, Americans have different standard, Germans have different standard. Communication, actually communication only probably works on standards, nothing else. I do not know anything they do more than standards. Or there should be another standard, so another 20 people will meet and create third standard. So every now and then we are finding standards.

Good travel and good nice time you see. So typically what we are saying, M1 is, has 10 particles of 0.1 micron and higher of course will be smaller. Class 1 has 35 particles. So I need M1 which should be less than 0.1 micron particle. So I should actually work on higher than M1 in many cases so that, of course 0.05 according to this will be even higher than 10 and we are expecting better than 1 inside that region.

So M1 also has been, now there are M1 to M9 standards have appeared. Intel is using M10, I do not know why that 0 appeared but that is their lab number. So I do not mean when I am clear, the other particles are, there will be all size of particles. Even if you have a HEPA, I myself may release, machines may release. So there are all sizes but then numbers should be correspondingly smaller if you go for a smaller or higher, smaller class of clean rooms.

And I already said what particles can actually trouble you when your circuit performance, I am least interested if these particles come and go. If it does not hurt my silicon, thank you very much but it does and I am buried. So please remember all other theories we have to talk about has some at the end the relationship with the performance of the chip and that is where we are actually bound to work for.

So all the courses in any department, in microelectronics probably they design earlier to say how ICs are done. Things have improved too many this way, so I do not know it is the only thing. Spin transistor for example, whether it will come or not but it is very interesting and its functionality is very, very good. It seems as if it will do everything what you want but whether it will do it at the end of the day and will go into chip, is only God knows. And I will certainly not because till 2050 it will not come. As I say I am not going to be there, maybe another few years also but at least then.

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Last part of this is as I say many of the wafers when they come, even if they are virgin wafers, virgin wafers means coming from the company itself in a box which are very highly tied. And actually there is a silica gel kept there so that no moisture is retained. Everything comes good as they clean. There are mirror polish, better than normal mirrors because there you have mercury oxide and other materials to shine. Here it is only silicon polish.

However there are, whenever you open a wafer in any clean area, there are called clean benches. There is, inside the clean room there is benches. On the top which is HEPA filters are there. Air is passed through this and the area below is laminar system. So you open a wafer that is better than the actual clean room area. And therefore much less particle contamination is expected on silicon. So better than class 1 as I said.

However silicon is extremely fond of oxygen, and therefore as soon as you open it, it will oxidize. And that can be seen by its polish. Suddenly your face may not be as bright. There are also organics which are, whatever way you touch it, whichever way, some grease, carbon, oils do comes on that. So even if we are getting fresh wafers but that is only first time but once you are, you started using, you are passing these wafers to number of chemical, number of gases. So they are getting this every next step anyway.

So some way, before the next process step starts, we must do something that the wafer is cleaned as earlier. So there is the cleaning procedure which was decided that we should have. Of course we also need pre-clean and post-clean things. Like for every process step, diffusion, oxidation, CVD, metals, many look CMOS process. Pressure creation, contact, wears in CMOS. For every process step you do, you need pre-cleaning to do this process and post-cleaning after the process has been completed.

So this pre and post is a part of the game. All processes which you work to make a chip, pre-clean followed by process followed by post-clean is standard practice. So silicon cleaning is an essential part in refabrication step and it follows every step in fact. So it is very important. These process steps, anyway this is the course. We will do all these processes now. The first process after our clean room system is diffusion or incorporation of impurities.

That is how device is made. P and N unless they are together, no junction. So first thing, how to incorporate impurities is the next core part of this course. As I say these are standards, they need

not have been written exactly in the same format as I wrote in the Plummer's book. But I think everything must be available. This course I do write myself, so I many times do not know from where it is and how it is but must be from some book, some journal, some idea of mine whichever I actually did. 30 years I was in process line, so I know what problems I faced.

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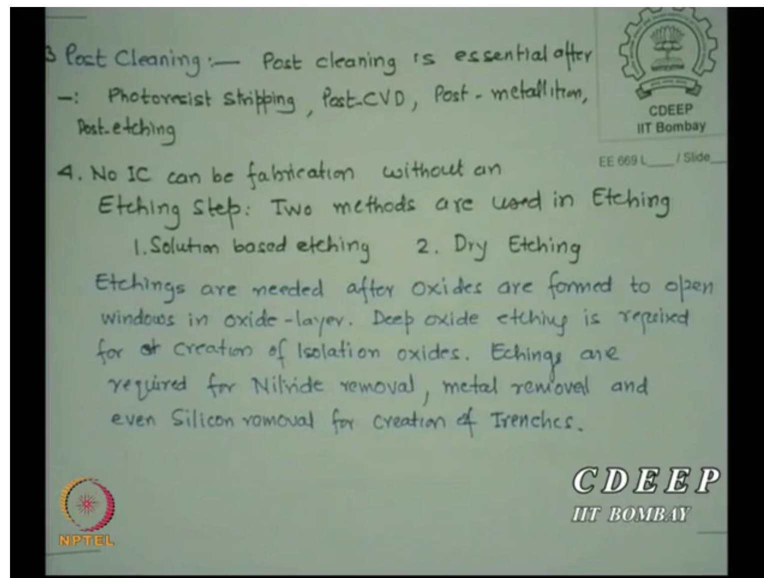

So as I say every process step should be followed by cleaning. Now most important thing is internal circuit cannot be fabricated without etching step. After you are selectively doing certain thing, that means certain area you want to remove, so etching is most important step other than lithograph as we shall discuss. And they actually form the major dose for any IC fab. Now there are two kinds of etchings we use.

One are called solution based in which you actually did the wafer into a solution. And other is dry etchings in which only gases are used to etch the things. Solutions, liquids and dry. In the dry etching also nowadays there is another etching which has started coming and that is called photon based. You bombard with photons. Something new has appeared. But anything you bombard, photon is practically no mask, so one expect no damage but it is seen there is a damage.

So we need to remove nitrides, remove metals, we want to remove silicon to create trenches. Oxide is the major thing we keep etching every now and then. We also need silicon etching because to create wears down. So the procedure which most people believe is correct, slightly

modified by different companies, there is a CMOS process, there is IMEC process, there is RCA cleaning cycle which is worst accepted by many companies with modifications which they never tell.

Like Intel follows only 80 percent of RCA clean. So what is that 20 percent, no one knows. Piranha cleaning, they have another process in which three steps are different from RCA. Why do they do it? But their wafer processing is good actually. So each company has its own cleaning cycles. And this is what very standard cleaning which is most people believe it is good and also work partly at least 80 percent to 90 percent is here. If you have written down, I may start looking for RCA, that is the major cleaning system which almost everyone uses. There is a small difference in some play steps which way back in 83 I have introduced which now, and they claim IMEC has, is doing it possibly.

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There are number of steps. When you take the silicon, first you boil the silicon or rather heat. Maybe 120 to 150, you can also call it boil in H_2SO_4, H_2O_2 solution. Typically some people use 1 is to 1, some use 1 is to 4. That is the difference. Every person has his own standard procedure in mind and he keeps doing it. 1 is to 1 is mine, maybe others I do not know. It goes up to 1 is to 4 if you look at the books or journals.

Typically 10 minutes boil is sufficient. Please remember do not put water around when you are boiling H_2SO_4. H_2SO_4 actually splits and may hurt your face. So do not add water any time in

boiling H2SO4. Why I know? Because once I did, my whole hand got burnt. So I tell you now. What is the purpose? To remove organic materials, grease and resist. Please remember H2O2 actually in the solution system immediately reduces to H2O plus nascent oxygen.

And nascent oxygen is extremely reactive. So what happens? Any material which by removal of their oxides or soluble, this nascent oxygen will oxidize them into solvents, soluble this into the liquid. So they will be removed from the surface. Same way carbons or carbon containing compounds get oxidized faster and are solubles or at least separatable from the silicon. The major reason why we also have H2O, H2SO4 of course can remove many materials because of sulfates which are solubles but we actually have H2O for one more reason.

Because it creates silicon dioxide, H2O2. So this oxygen reacts silicon faster and then makes SiO2 and this thin SiO2 layer actually contains impurities. Because the surface area is same. So some of the impurities are well within this thin oxide. So if I next time remove this oxide, even those impurities will be taken care. Those will not form sulfates nor form oxides, can still be retained in this top silicon dioxide layer which I am naturally creating.

And they can be then removed out. The every process step of any kind must followed by DI water rinse, we will discuss what is DI water. And after DI water rinse, the third step is we etch the wafer, HF plus H2. HF is agent for SiO2. Fluorine is a very strong oxidizing and reducing agent for SiO2. So it removes as silicon fluoride. Silicon fluoride is soluble material. So SiO2 plus 4HF is SiO4 plus H2O is the reaction.

Typically this is called dilute HF. 1 is to 10, 1 HF, then this, and some people do even as low as 100 H2O, H2O2 which means it dilutes the HF even lower. The reason why they dilute because thickness of silicon dioxide is very low during the last process. So this is sufficient for removing this much. But there are other people believe that HF also tends to actually create, I mean why larger because they may give some pits.

So they are people who have different times and temperatures. Typically 1 to 2 minute at room temperature is sufficient. Again every process step must follow DI water rinse. So 3 to 5 minute you rinse to remove all HF traces. Then this is the most two steps which are coming now, are the most important step. This is how RCA is more strenuous for.

To remove organic metals and like hydroxides or oxides, we put the wafers in NH4OH:H2O2:H2O bath. Typical ratios can be 1 is to 1 is to 5. 1 NHOH, 1H2O2, 5 water. Or in some cases 0.05 NH4OH, 1 H2O2, 5 H2O. This is called SC1 cleaner. Company names this as SC1. You boil the wafers for 10 minutes around 80 to 90 degree centigrade bath or by films whichever this heating plate.

Nowadays we have rarely used plates because plate themselves are particle containing disk. So we actually use baths. They remove as I said and since there is H2O2, it will again give a trace of silicon dioxide when you remove the wafer from the solution. Again rinse it for 5 to 10 minutes because this NH4OH ions has to be removed much more from them. So we rinse it longer at room temperature.

For example, IMEC not only adds in this first step either H2SO4 and ozone or followed by H2O plus ozone. So they are ozone technology. Ozone again is similar like H2O2 because ozone breaks faster into O2 and O and it does the oxidation. So instead of H2O2, IMEC is the micro-center at the Belgium where from Anil has his PhD. So it is from his recital, he is using ozone. Ozone has an advantage that you can actually push through gas phase but then it bubbles and it actually does not allow proper rinsing of silicon. So there are issues. If you ever ask me, I would also, I does want the best way but does not matter.

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Reagent	Temp. & Time	Purpose
7. $HCl:H_2O_2:H_2O$ 1 : 1 : 6	80° to 90°C 10 min Boil	i Chlorides removed Alkali Ions Metals as Chlorides are removed; ii Oxidised Si
8. DIW Rinse		
9. 1% HF treatment followed by DIW Rinse	Room Temp 10-20min.	Oxide is removed
10 Drying N_2 gas flow. OR IPA vapours (INTEL)		

After this we want remove remainder of metal ions or alkali ions as chlorides. So we have, we boiled this into HCL:H2O2 plus H2O in a ratio of 1 is to 1 is to 6. Again boil for 10 minutes and 80 to 90 degree centigrade. Chlorides are removed as alkali ions, metal ions as chlorides and again whenever you put H2O2, you will leave a thin layer of silicon dioxide. Now many people believe and that is the difference between say our RCA clean and many real RCA clean which started way back in 70s, they do not have the step 9.

They do not etch the last oxide. They believe this 20 Armstrong oxide is a good passivator, it is punchable by most impurities. So it is better to preserve it for the processing. We believe that 20 Armstrongs of oxide may create interphase states. Those interphase states may actually reduce mobility in a short channel device. So however we believe for slightly different, so we normally used to etch. And many companies now I find do etch this HF actually.

So we give 1 percent HF treatment, that is 1 to 100 in water. Boil it, and again rinse it very heavily now for 20 minutes or removing all kinds of fluorine traces, all kinds of whatever in the material and the surface should go away. Normally in a running water, spray water as we say so that most of the physically removed particles can be moved out. And many cases you can try these wafers into N2O gas flow system or there is another which Intel uses is isopropyl alcohol wafers, IPA.

So people do not think N2O, N2 is very pure compared to IPA. This is there because it can be multiple distilled IPA. So Intel still uses IPA compared to nitrogen flow. Please remember the process steps which I am talking are generic, company to company, Siemens have slightly 30 percent different from this, Micron has even different, Google foundries have even another small variation in their last steps. So each company has its own processing cycles and we keep doing. Before we leave, just a minute.

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In IC processing most used reagent is water. Water is the major reagent we need. As I said other day we need roughly for a good foundry 54,000 gallons of water per day. So it is the company has to provide, get this much water from state government. Okay, 54,000 gallons per day is used by a company. So we decide the quality of water which is called ultra-high pure water. Something nowadays most people are having Aquaguard or water purity and whatever it is, it is essentially purifiers. Similar system is used.

There are three quality markers of water. One is the resistivity, other is particulate size in the water and third is bacterial content. Now typical tap water if you look at, actually there is a statement made by some good doctors these days: start actually drinking tap water. And now do not believe me, I am just telling you. They say it is much more good, it is much better for human body when it produces what is called as cells which will actually protect you. So maybe but essentially tap water has dissolved inorganic compounds of sodium, calcium, strontium also.

Even some mercury traces are found in human body. Dissolved organic compounds like living matter, then there is a particulates like silica, sands particles, dust particles, paper pieces. Then there is a microbiological life like fungi, algae is there. And there are of course bacterias, both can be viral or non-viral. Now the first thing on most, mostly we do is to figure out resistivity and typically water resistivity to be used is something, quickly to one more slide and we will finish.

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H2O, please, H2O goes H plus OH in any equation in equilibrium. H and OH ion concentration is equal and it is typically of the order of 6 into 10 to power 13 per cc. Diffusivity of ion is essentially given, we have discussed this kT by q mu, where actually the mu or mobility of ions is given by z qD by kT and this relation is not pure Einstein because there is a charge z, ion charge z is associated.

So it is called Nernst-Einstein relation. So we calculate for mobility for mu H plus and mu H by using this if I know the diffusivity. Diffusivity of OH and H ion are known from chemical people. This is 9.3 into 10 power minus 5 centimeter per second. This is 5.3 into this. So I get mobilities. If I know mobility, then I know the concentration. What do I calculate? Resistivity. I know the mobility, I know the number, I know the charge, so I know the resistivity. And resistivity of water is therefore a measure of quality. I will just show you the numbers.

H2O breaks into H plus OH, equilibrium both are same concentrations. Diffusivity is given by z qD by kT, mu is called Nernst relation, Nernst-Einstein relation. So I calculate mobility for hydrogen ions, mobility for OH ions which is 3.59 and 2.04 centimeter square volt second. These numbers, so if you can somehow do better, then we will see what can be done better. Is it okay?

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So if I calculate resistivity which is q mu n plus q mu p, like similar like H and OH, so I calculate mus, I know concentrations, I substitute them here and I find that the pure water has 18.5 mega ohm centimeter resistivity which is extremely high. You need not put all this, you can write row as this and directly write this. I just did maths. If I compare with DI, tap water with deionized water, then the resistivity is tap water is 200 ohm centimeter.

You can see how bad it is, so many ions. But as I say they may be useful, some of them. 200 ohm centimeter is tap water and DI water is greater than 18 mega ohm centimeter. Electronic, electrolytes available inside tap water is 10 to power 5 part per billion and it should be less than 10 part per billion in case of DI water. Particulates, 10 to power 5 numbers per cc in tap waters, less than 10 numbers per cc in DI water.

Organics, 10 to power 2 to 10 to 5 numbers per cc in tap waters. Of course these are not necessarily Bombay water, it can be worse or better in certain areas. Borivali may have worst, we may have the best. You know why? The first water released come from the cleaning this in Bhandup to IIT without actually getting further contaminated by the pipe lines. So we get probably the best water in whole Mumbai luckily.

So these are the numbers which we get and maybe quickly next time we will show you some systems and they are not very important. And we will show you that once the process is now

ready, we can start actually the first process in corporation of impurity. Maybe I will show you DI plant or something for few minutes and then start. See you then.