Fabrication of Silicon VLSI Circuits Professor. AN Chandorkar Department of Electrical Engineering IIT Bombay Lecture No. 3 Crystal Properties and Silicon group

We have seen already importance of technology in making realisation of integrate circuit is and now systems the course really now starts. The way I organized a something like this, since the starting material for all integrate circuit is silicon chips mostly they are working at and therefore with starting material silicon and so we will see first how silicon is obtained, okay.

Once we know how silicon can be achieved, best silicon of your silicon is available and particular form of (()) (0:55) I want then I will say okay take this so-called silicon wafers inside the clean room or inside the lab where actually fab is going to be done then we discuss therefore something about the conditions in the fab lab's which are called clean rooms. So we will then discuss something more about cleaner rooms.

Then we will also see there is that you know when the silicon comes packaged from elsewhere many times there it seems very clean, it is very polished surface and everything but it still has many other impurities particularly organic ones, so the first thing before any processing start we have to clean the wafers and there is a standard procedure of cleaning and we will see what are those procedures and how silicon is ready for the actual processing.

In most cases the first process is normally oxidation but maybe we will do something more about diffusion because some part of the diffusion characteristics are required in oxidation. So we will start first start studying about the incorporation of impurities which is called diffusion of impurities in silicon followed by we will talk about oxidation's variety of kinds and once we did oxidation we look for lithography, we look for metalled other depositions, metal deposition, etching all this will follow as if we are actually working inside the lab and we are trying to realize and then I show how many mask as we will latter are required to realize some kind of CMOS chip or even MOS chip.

Typically you may require around as I said 400 steps, 400 to 450 steps and asking may be as low as 16 mask processes can be as high as 34 or 36 mask process.

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Crystal Structures Solid Material are of Three kind CAMERA 2. Polycrystalline 3. Crystalline 1. Amorphous depending upon Seriodicity of Lattice Amorphous :- Non Periodic Poly crystalline :- Partially Periodic Periodic Crystalline :used in Fabrication

So I am going to one by one is Crystal per se is a solid material of 3 kinds every solids are available in 3 kinds, one of course is the state is called Amorphous, the second is called poly crystalline and third is called crystalline. The difference between the 3 is something like this, please remember all atoms in a solid are arranged in a particular manner and their arrangement itself decides the kind of material whether it is amorphous, polycrystalline or crystalline.

I may start with the lowest one, crystalline first, crystalline materials are those whose atomic arrangement is such that they are periodic in nature that is fixed atomic arrangement repeats all sides, so this is called periodic structure for crystalline material. So there is a periodicity every lattice we will work this word soon every such smaller cell which is repeated is called lattice and there is a lattice periodicity which creates a solid.

So you can see from here those are atoms in particular order are fixed and they are bonded exactly as they are nearest possible bonding is possible, so this is called crystalline materials, so this is called (()) (4:14) materials. If there is no other of atomic arrangement then we say such materials are amorphous in nature, okay. Most things which you use many a times other than metals are mostly amorphous in nature.

Most compounds are amorphous in nature for example silicon dioxide which is the most important material for us in IC processing is generally available only in the amorphous tile.

"Professor -Student conversation starts"

Professor: However if I crystallise it what is it called, yes?

Student: Quartz.

"Professor-Student conversation ends"

Quartz, in between also there is something but we will come to it later, okay. So quartz, quartz is the crystalline SiO2 whereas we are looking for right our amorphous material which is silicon dioxide as amorphous this is used often, okay. And in between this there is a partial order that is the direction of lattice at different...

There are number of such crystals in one area then we say it is poly crystalline even this material is required in IC processing. So all 3 is remember these though most of the time we talk about crystalline materials, the other 2 also play a lot of role in our fabrication, in particular if you look for solar cell these days we were working most of the time on crystalline silicon there to make a solar cell.

The cost of making crystal is very high as we shall see it today and to reduce the cost, if the process which allows the films to be deposited which are amorphous in nature is much cheaper and solar cells people major activity or major work is what they called as watts per cent or cents per watt it is how many cents per watt it cost or how many watts per cent you can create is the feature figure of merit for them cheaper the one that is larger watt since smaller cents as smaller cents in larger watts is essentially what is the feature of a good solar cell.

Since the amorphous films are much cheaper to make and much repairing cost otherwise they may be the best candidate as far as the low cost solar cells are concerned. However if anything is good there will be something wrong, so they are very poor in efficiency and therefore if you look for higher efficiency solar cell conversion of optical energy into electrical then the crystalline is the best and there is a microcrystalline also which is close to poly crystalline better than amorphous little (()) (6:52) then poly crystalline it is called this and this also are these days work for reducing I mean increase in little cost with greater efficiency.

So if we look into the solar cell area latter if time permitting this year I do not know then we will see that there also material choices are very crucial. Silicon IC is per se starting material is always crystalline silicon and we will like to see how that is created in actual way.

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Arrangement of Atoms in Solid is called arrangement of hattices. Most Semiconductors like Silicon , Germanium and II-I compound Semi conductors show crystal amongement called Cubic Lattice. 1. Simple Cubic - Polonium 2. Body centered Cubic - Tungsten, Molybdenum & Tatalum 3. Face-centered Cubic _ coloper, Cold, Silver, Platinum 4. Zinc-Blend Cubic. - Silicon and Gras CDEEP

As I just now said arrangement of atoms in solid is called arrangement of lattices, one single arrangement which is periodic in nature is called one lattice. Most semiconductors like silicon, Germanium, 3 5 compound semiconductors like Gallium Arsenide Indium Arsenite, Indium phosphite, Gallium phosphite these are compound semiconductors, 3 5 materials as they are famously called, they also crystalline arrangement and normally they have what they called the kind of lattice which they show is cubic in nature, okay.

Of course in the cubic itself I will show you other lattices little later. The simple cubic there is only one material which is popularly known there are maybe few at least I could only gather one polonium which is more radioactive material is essentially have a simple cubic structure. Okay, I will show you this lattices little later.

Then there is an arrangement called body centered cubic, the materials which are known in this kind of lattices is tungsten, molybdenum and Tantalum. There is a third possible arrangement which is face centered cubic copper, gold, silver and platinum and of course this zinc blend has one more possibility which is called Diamond. Diamond essentially is a slight variation of a zinc

blend but it is classified in the same. Silicon lattice is diamond lattice where is Gallium Arsenide is zinc blend lattice, okay.

So what is the purpose of these lattices? Since these are the arrangement possible in atoms we are interested in particular kinds of lattice exist and if I want to create a material of different kind for example for electrical conductivity expect that the material should be either N type or P type that is it should have excess electrons or excess holes, so that the current can actually transport.

Now this idea that only semiconductors allow you this 2 bipolar transport is very important, metals only show electron transport, insulators do not show any transport if at all they show they will show electron transport but very difficult transport. So the materials which are used in everything in this, it is a circuit area is P type semiconductor or N type semiconductor and therefore how these semiconductors can be doped to make it P type N type is also part of this crystal growth. Initial wafer or initial substrate should be doped to a given value, this given value and type of Dopant is very very crucial in actually making the device.

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 $V_{T_n} = \phi_{m_s} + 2\phi_F$ - Qox - QBulk $2\phi_F = \frac{2kT}{2} \ln \frac{N_{a,d}}{n_i}$ QB = 1 2 Nord Xdmax Xdmax = 2K560 DEEP

So this fact has to be understood by you that why we are so worried about this is the fact if you look at the electrical characteristic MOS transistor you can see the threshold voltage of a mass transistor is given by for N channel device VTn Phi ms Plus 2phi F minus Qox by cox I will

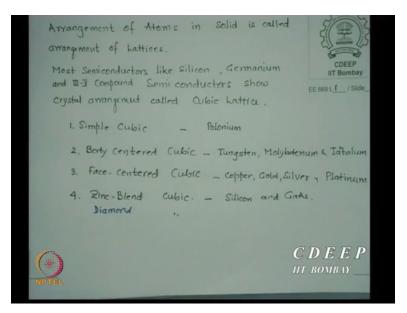
name the term minus Q bulk divided by cox, 2phi is 2kT by q Ln Na or Nd by ni depends on what you have except (()) (11:17).

Q bulk essentially is q Na, d Xd, Xd the depletion layer maybe max, XD max is equal to twice Ks Epsilon not upon some phi F, okay, 2phi F upon q Na or d, so you can see from here if I want to control the threshold voltage of (()) (11:54) device as shown here or P channel either of them then I must be able to have fixed value of acceptors or donor concentration in the substrate because these Na or Nd are constant only then phi F is constant, the bulk charges are constant and therefore to fix Vt I must have a process which will fix my initial concentration in the wafer, okay.

So one technique which will allow the substrate to have a known concentration is to dope the crystal during its growth itself, okay. Otherwise of course you will go to other process called (()) (12:36) growths but we will see this later. So essentially I say dope concentration of wafer is a very very important parameter many a times in deciding the electrical property of transistors.

In the case of bipolar the base width and the base doping again decides the gain of a bipolar transistor. So again the doping in the base in specific is very very crucial to design the beta of a transistor. So in some sense starting material resistivity or charging material donors accept our concentration is very crucial to us and therefore how do we dope the crystal, okay. So these are the issues which we like to solve in the coming hour, okay.

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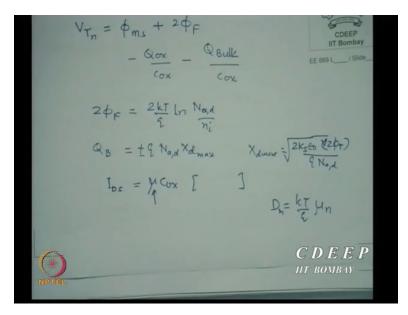


So the lattices, why I am worried about lattices? Because lattices have a minimum amount of volume in which so many atoms are residing. Now if I want to introduce an impurity there is no volume there, okay. So where with you will go, okay. So there will be something where this so called impurity atoms like phosphorus, arsenic, Antimony beyond Aluminium which are the dopants for P or N type, N or P type can get in.

And how do they get in and they uniformly distribute everywhere? Because crystal will have large volumes or large areas in many cases and so we want her uniform doping everywhere that is our major worry, how uniform are you really uniform? So understanding a lattice has some advantage because then we know how much of the possible external atoms can come in without actually disturbing the periodicity of the lattice.

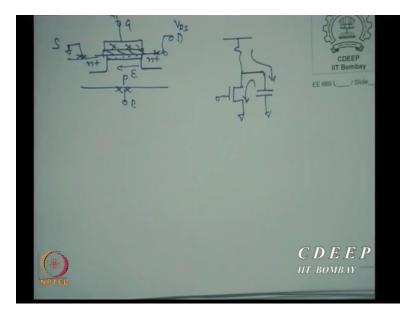
If crystal bakes or it dissociates then it will go to polycrystal or even amorphous, the problem with amorphous semiconductor to crystalline is because in the most electrical characteristics of any device if you see very carefully.

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If it is a MOS transistor the (()) (14:46) into source current is mui into Cox into voltages, so there is a molality term appearing. If you look at bipolar transistors the diffusion coefficient of the careers minority carriers in the base there the D is related to mobility by Einstein relation say let's say Dn. So the mobility of the carriers essentially are going to decide the available current in the both bipolar and MOS transistors and therefore we would like to see the material should have a known mobility or at least controllable mobility, okay. And only then I can fix a current, why I am interested so much in mobility control because if I am working at a circuit, let's say what is that?

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Let us say it is a simple MOS circuit I take. Typical MOS transistor looks something like this; I am giving you a cross section worth this is a n channel device, okay. This is gate oxide, this is my gate, this is my drain, this crosses our metal connection sources and this is bulb. The current is actually electrons are moving under when I apply VDs apply VGs, I create an inversion channel hopefully if VG succeed threshold then source is grounded VDs is positive electrons move from source to drain because of the (()) (16:29) field. There is a electric field in this direction and the electron move towards drain, okay.

Now this electron through the channel they are moving and I want this current to be known to me because I will decide if I had a capacitor as my load, okay. This is my resistor, when I say I want a circuit to be faster I want charging to be faster and I want discharge to be faster, obviously the current made available to you from the power supply and the one which is grounded down from the capacitor discharge both are important to improve the speed of the circuit.

So current control is our major aim, so we do not think that is so called metallurgy chemistry, material science which I teach has no relevance because we are actually looking at my circuit which is what is driving me to do all this till maybe 90, most of the electrical engineers should also doing fabrication. Of last 20years chemical engineer have taken our role though we are still the ones who probably manage them and tell them what we want and how you should do.

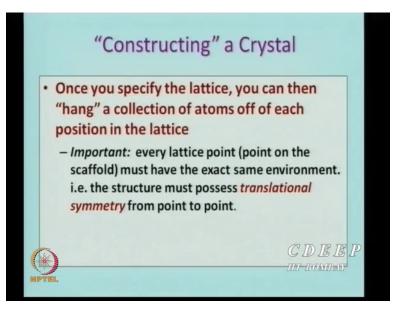
But off late I figured out for example Intel's last chief was also a chemical engineer, okay. So it's not true that only electrical can do but the idea is that study of a circuit essentially forces me to study devices, devices I want to finally make from somewhere and I must know all technology to make it so that the so called circuit performance or resistance performance is guaranteed, is that clear?

I will like to make my technology independent of design as much as I try, so that this designer should actually ask me what did you do? Okay, he say these are my parameters I gave you use them and design your chip but things are not becoming so simple we need to know what is happening in technology designers must know and what designer can do also technology must take care and therefore now understanding of technology where designers is as much relevant in 22 nanometres no one would have believed as much it was earlier in 0.5 for 1micron nodes technology people were told you do what you like tell us what is your limits?

Designer will say I will use that do not worry, okay. Now it is not so much true, so in study of technology is still relevant now or rather it has become more relevant now which was earlier in 70s or 60s much more stronger separate disciplines, okay. So please remember that all our thinking has something to do with this circuit and it is not just material which I am studying but as an electrical engineer I will like to know if I have to achieve this what should I make a choice for, okay.

And that choice is something you must understand, so many people get bored with this courses many times too much chemistry, chemical and things goes on but they are part of the system you know and in a system you cannot say I will only use this part of the system, system is a system, okay.

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Okay, so first thing let me first go to lattices, so how to construct a crystal? Once you specify the lattice you can then hang a collection of atoms of each position in the lattice and that is how we can always create a crystal and this the lattice points are essentially like a, you know when you build a house or build a building that is scaffolding all around from which the building is created after that. So this is atomic structure which is bonding is essentially scaffolding and it has this transitional symmetry that means you repeat and the crystal repeats.

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Generally there are only 14 ways in which atoms in solids can be arranged these are all shown here this is called Triclinic, when it is like all 3 sides are not equal and their angles are also not equal this is called Triclinic then there is a monoclinic, Alpha is not 90 but the other 2 angles are fixed or Beta gamma is 90 and alpha is not 90 with a slight variation in sizes and there is an atomic additional atoms at the surface, 2 surfaces then it is called monoclinic then there is a standard cubic structures which are slightly modified to look as Orthorhombic.

None of the sides are equal by their angle can be 90 then none of the sides can be this but there can be atom in the centre, we will come back this figure again and then can be this when you can have atoms at the surfaces and then there is another arrangement which A not equal to B not equal to C but there are additional atoms connected and we will see this structures are called Orthorhombic.

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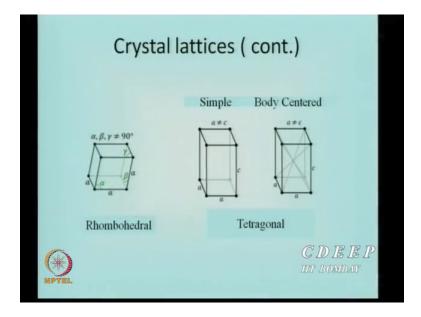
These are available, okay I will just tell you this is the book which either a sum of you should jointly buy or Xerox it, Xerox is officially not allowed, unofficially I don't know, I just check up if it is available in library and if there are fewer copies I may order some more otherwise those who are going to remain in the nanolab, they keep saying they want very high level research going on there they should at least buy this, okay. This may be a good bible for them, okay.

So if both (()) (22:31) I suggest of course this is second edition, this is (()) (22:36) this edition, Indian edition may be in the (()) (22:40) also I have no idea this was purchased 7years ago. So maybe 3rd or 4th edition may be there, I am not aware but I have this book I don't lend anyone please take from me, I would not lend this book to anyone 250dollars, okay. So do not come and say, Sir I need it just for a day, I would not give it for a day, for an hour and not even for 30 seconds. So please either buy whatever you can do, okay. Do not steal from me.

So this book almost gives everything which I am talking not necessarily in the order, no necessarily the way I am saying something which I say is, by the way professor Plummer who is the first author is the Dean of engineering at Stanford university and he was the professor I mean he is still a professor in the E department. His friend is my friend or his colleague is my friend Krishna Saraswat. He is also around same age as mine.

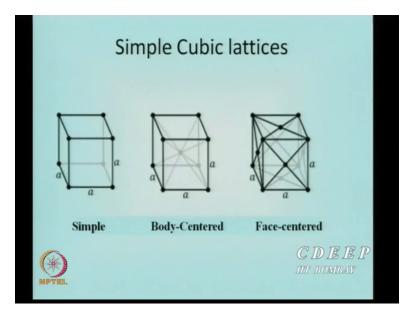
We both are from Birla institute together he was junior to me and my son who was doing PHD at Sanford did a course with Plummer. So I have met 3 times Jim, so I can tell you the way he thinks, he has being the strongest consultant in technology in bay area. Any problem finally comes they say pass on to Jim, okay. That he may solve it finally may be some student of his will solve it, okay. There are many IItians who would do PHD with Plummer and with Saraswat, okay. This is just to give an idea why I am saying you; Plummer is one of the most famous person.

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Now here is something Rhombohedral in which none of the angles are equal, sides may be equal but shape is slightly tilted then there will be Tetragonal A and C are not equal other 3 sides are like this then there can be an atom in the centre which is essentially called Tetragonal is called Body centered, so there are 14 possible ways in which atomic arrangement can be done and that is the basic thing we know about.

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However as I said already there is the one which is the Cubic lattice which I was just talking. In this cubic lattice Cubic means A B C are equal each angle for this is 90 degree, so it is a Cube the length of each side is A is called lattice age, each material has a different lattice age for example Silicon has 5.43 angstrom, Gallium Arsenide is 5.68 angstroms. So it depends on the material this lattice age will be different even for cubic or other lattices then if you see this second one you can see from here there is an atom in the centre of the lattice and each is then bonded to corners every other (()) (25:48) this is called Body centered and if there are atoms not at the body but every surface then there are 6 surfaces, so each atom is there.

But very interesting thing you should remember, since it is periodic in nature how many atoms this cell has someone said one is correct, why? Because it is a periodic there is a possibility of another lattice sitting left, right, top, bottom, so 8 such corners can meet at a point, so each corner will give you 1 8th atom, 8 corner will give only 1 atom. So ages of the cubic lattice only contributes to 1.

"Professor -Student conversation starts"

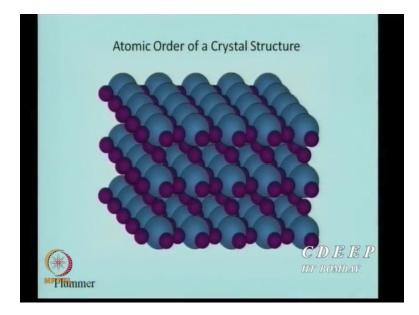
Professor: In body centered there are 2 because 481 from the corners and one in the centre and the surface, how many?

Students: 4.

"Professor-Student conversation ends"

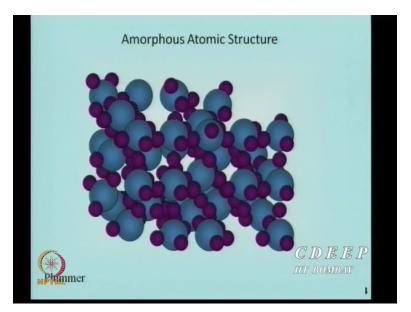
4 because 6 means they will share with the other one, so 3 plus 1, 4. However the one actual structure which we are interested in is Silicon which is neither of them, okay. Then why are we showing because from the phase centre we will create a structure which is silicon structure and it has number of atoms are 8, okay. So let us see how do we get to it?

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This is just to show you atomic arrangement (()) (27:11) structure, 2 different material show Gallium Arsenide for example okay, this Plummer slide that is why I said you all introduction, this slide we have taken from him personally. So all Plummer slides due regards to him that he allowed me to have them. Only thing he said don't sell it to in a book I said fine I will not.

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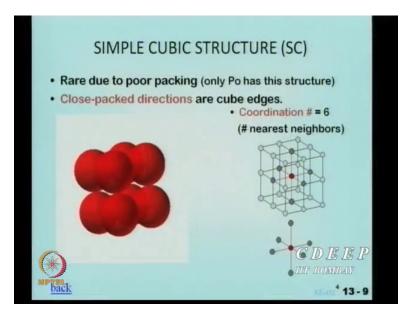


Here is an arrangement which is non-periodic random and since you can see they are random there is no periodicity and therefore material is Amorphous. Crystalline I forgot there the mobility's of crystalline structure is the highest Amorphous is the least. Now mobility why it is proportional to this atomic arrangement is the following whenever let us say electron is given by an atom like an N type material or otherwise and you apply electric field to a solid electrons will try to go towards the positive polarity.

However there will be large number of electrons in the crystal, okay and each will actually interact with these moving electrons, okay. This energy sharing is called relaxation or scattering. So whenever electrons start moving it hits something and then it loses the path because once hit this it may shift way there are many other space charts, there are number of scattering events happens and not all electrons in the Amorphous are possible to reach to the positive terminal that means the (()) (28:43) mobility of a carrier in Amorphous material is very very low, okay.

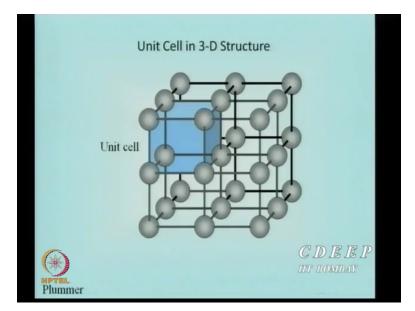
Whereas in case of single crystal since they are all atomic arrangement if electron is moving between atoms they hardly scatter except the space charge as it is. Of course therefore it is not infinite otherwise all of them would have gone some will not go even now and this scattering events reduces the possibility of all reaching there with a given velocity and this is essentially why crystalline material show highest mobilities, okay. Compared to polycrystalline and compared to Amorphous, Amorphous of course is more like an insulator many a times you may have a resistivity of the order of 10 to power 8 ohms centimetre semiconductors may have order of say 0.01 ohm centimetre to maybe as high as 10,000 ohm centimetres, so this is Amorphous.

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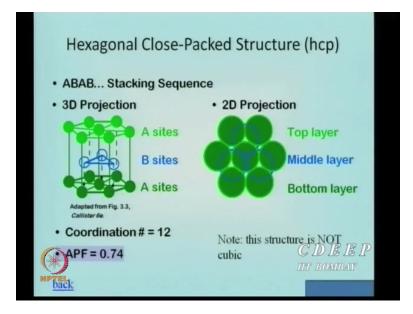
Now there is a word what is it called? Packing, now this packing is a very interesting word which you will be surprise to know but before let me come to silicon first.

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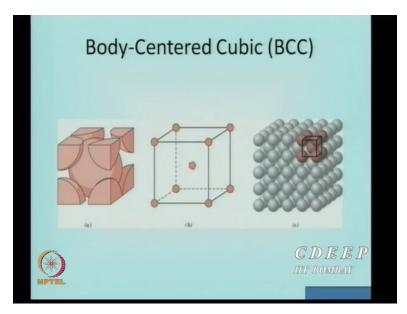
This is called a unit cell smaller structure of atomic arrangement lattice as it is which allows you to repeat itself and create a crystal is called unit cell, okay is called unit cell. Please remember this is unit cell but not a primitive cell, now this word is very interesting this is a unit cell but not a primitive cell we would like to see what is a primitive cell for silicon or for any other material? This blue colour volume, there are how many atoms? 8, it's the cubic lattice, so there are 8 atoms and you can see they can be repeated now all sides to create the large size of crystals.

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There is also an possibility which is called hexagonal close packing some materials do show this for example diamond has similar structure hexagonal, Quartz have similar structure, so hexagonal closed packed structure is frequency on the top there are 6 edges and they are called hexagons.

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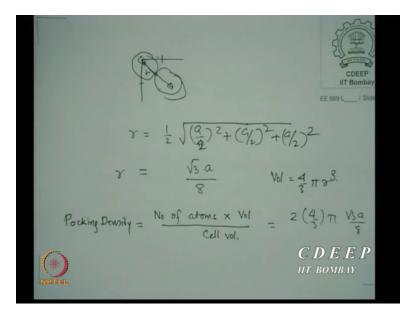


Now why I draw this? Is to show you what is this word packing density? The way packing density was say that let say in the body centre you can see from here, the centre one is the slightly enlarged version, the actual lattice is shown in the right. So we create a model which is called heart's sphere model, okay.

So each atom we blow it by size, okay equal sizes. If they are Silicon all the atoms are of equal sizes, so we start increasing from the ages blowing the size of the atom, whenever they will touch each other we say that's the distance between these 2. So you can see from here this sphere corner this is only shown half quarter of this but the upper inside part is not shown where the centre one is fully shown, okay.

So if I want to calculate distance between the corner atoms and the so called body centered atom, how do I calculate? This is the lattice age they are at the centre, so it is diagonal from any atom, okay. So how will you calculate a by 4 square plus a by 4 square plus a by 4 square under root of this essentially is the distance between the 2 and since we are trying to make 2 atoms stretch in this distance, this body centre and let's say this, so what is the radius of each atom? Half of this, that radius is called tetrahedral radius R maybe we will discuss, so a by 2 a by 2 and somewhere here, so if I want this diagonal.

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So if this is your body centre and if I start increasing the (()) (33:07) for this then I want to calculate this radius r, is not it? This radius r, since each is a by 2 a by 2 and say diagonal, so that tetrahedral radius is half of a by 2 square plus a by 2 square plus a by 2 square, so essentially it is a square by 4 a square by 4, so root 3 a upon 8, is it okay? So this is the tetrahedral radius of this, so what is the volume of this sphere then?

4 3rd pi r cubes is the volume, is that okay? In the body centre how many atoms are there? 2 atoms, so what we will do is, number of atoms into volume divided by cell volume, what is the cell volume? A cube, this is called packing density, so we can say 2 times 4 3rd pi root 3 a by 8.

"Professor -Student conversation starts"

Student: Sir which is for Silicon?

Professor: This is not silicon, a is only age any is this, body centre is not silicon.

Student: Body centre is r is equal to (()) (34:57) by 4.

Student: 2 a by 2 whole squares.

Professor: a by 2 a by 2 and a by 2 it is a diagonal.

Student: calculation.

Student: calculation.

Professor: okay calculation you can do that.

"Professor-Student conversation ends"

So the problem which I am saying is, if I now calculate this by a cube we are right, okay, whatever I get packing density is typically 78 percent is a packing density of a body centered lattice. If I do the same analysis for face centered, how many atoms there? 4? Okay

"Professor -Student conversation starts"

Student: 16.

Professor: Sorry, I think I did not have the number, so 52 percent for body centered, face centered 72 percent but if I do for silicon which is very interesting that comes out to be ready for percent and the number of atoms in silicon are 8, okay. So which looks very funny that there are 8 atoms in a lattice and the packing is only 34 percent which means the lattice is very loose, impurities can easily come inside the silicon compared to any other material therefore platinum cannot be easily doped, okay whereas silicon can be, okay.

"Professor-Student conversation ends"

So the trick about calculation whether impurities can get into material is decided by the impurity you are talking, size of that impurity as well as how much available space for you to enter inside a lattice where it can still bond with the atoms and does not create any strain, the most important word is it does not create any strain. So without straining how many atoms can get in is essentially per CC if I calculate is called concentration.

So I am interested to know how much concentration I can (()) (37:10) impurities in a silicon crystal, so that I can say, okay this much imperative atoms are available and once I know if any RNDs are known to me then I can do all kinds of calculation for my device parameters and

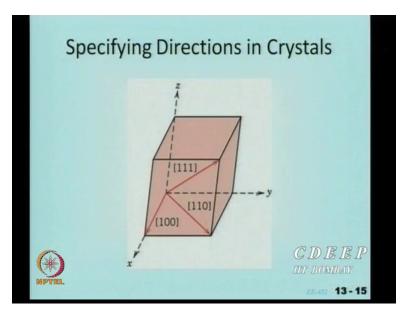
therefore my circuit performance. So to essentially know how much I am trying to understand what is happening actually.

Though many a times you may be right or I may be right, anyway no one manufactures wafers in the world other than some few manufacturers, okay. Maybe refer cam is 1, money sentry is one (()) (37:46) is one, (()) (37:47) is one; Japan is likewise one because the process of making silicon wafer is very very costly. Typically silicon wafer plant from polysilicon to silicon is around 1 billion dollar typically and they cannot do more than 8 inches. If you have more sizes you need even costlier (()) (38:08).

And even to make large number of wafers the users are only fixed, okay. So if every company has its own crystal growth system they will be just putting their use of their crystal (()) (38:22) 10 percent of the available capacity, so that is a big loss and an industry anything which is ideal including humans are thrown out, okay. So ideally is the worry for everyone and therefore the capacity remaining ideal also is not encouraged.

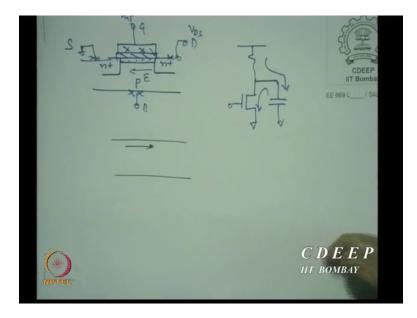
So just think of it why no one makes silicon as a material they get it buy it from somewhere at relatively higher cost because someone makes for you. However if he can, he or she company whichever CEO seek an early can supply you of any kind of dopings, any size of wafers with different density as to what will come as much as you specify, okay this is something very very important.

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So here is a phase centered and here is, okay hexagon. Before we go to other packing density our silicon I will come back there is something you need to know of the crystals, the directions because if you look at...

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If this way it is shown here this is the surface of the wafer and this direction is 1 0 0 the crystal because the mobility of electrons in silicon is highest along 1 0 0 direction, the. Now as I said for

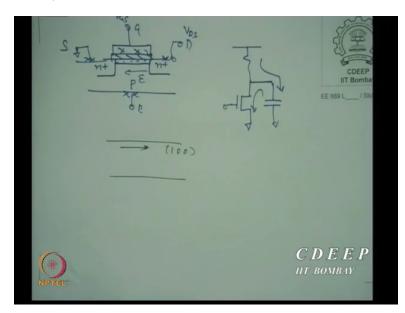
a circuit I am looking for higher mobility and if I see 1 0 0 highest space, so I must have a crystal which is called, has 1 0 0 plain and the direction is such that it is orthor...

Direction means? If this is your plane this is direction because you can create crystal like this, so if this is your plane this is your direction, so we want to create a known plane of the wafer which we will use in the case of MOS transistors as well as bipolar. Bipolar transistors normally are 1 1 1 oriented, MOS transistors are always or not necessarily always now they are changing.

They are going for 1 1 0 but most cases it was 1 0 0, for FinFET's 1 1 0 at least some characteristics but for a normal MOS transistor 1 0 0 planes are most preferred planes, okay. So we would like to see why we are looking into this because I keep referring you back to circuit because that is where my ultimate performance is, I am looking for circuit performance I am not interested in all these jumble if that does not help me to improve what I am really looking for.

What are we really looking for? High-speed circuits, large density circuits, okay. Low-power dissipation, since I have parameters in my mind if I look the technology back I will start looking if I do this where it hurts where and I improve here? If I improve can I do that there? Some way we are trying to match best of technology to the best of requirement of designers or system users.

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So please take it that this whole course was planned in 80s when I joined IIT Bombay was because I thought that most of the Indians including myself maybe we are very much shy of

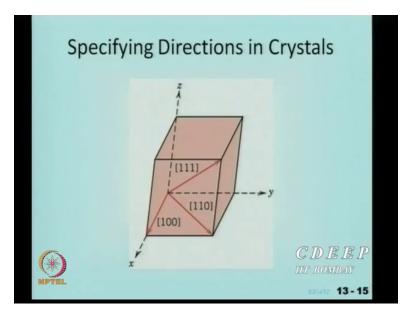
doing technology and more say in 2014 now with so much of laptops and what iPad's and pads whatever it is, the tendency is only to work on everything on CAD tool everything can be seen.

So why do it, okay. Unless you do it like for example other day I made a joke also you can do everything on CAD tools, (()) (42:15) tools, design tools you can create almost a reality which is called Virtual the only catch is can anyone inside scream give me a cup of coffee which I can bring if that so that day I will say CAD is very good, okay. Till that happens someone has to hand me something which is real that all other things remain virtual.

If you go to Japan 90 percent of their scientists or even professors actually work on technologies of course they are not doing recently but otherwise why they did so well? Because they have the best of technology, why US do so well? Because they have the technology we do not have technology, we always have CAD tools, Infosys is our ideal I can fill up some data for LIC I have to do something, change the date I say Y2K and I say I know a lot of computer science, God forbid, okay.

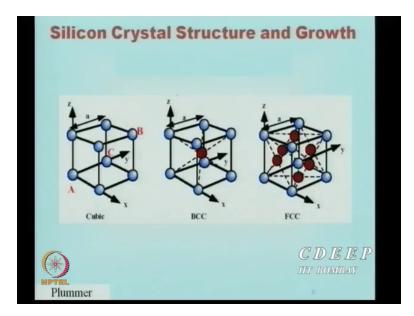
All sort and done the course is therefore were written then that at least introduce our students to a hard job which is actually realisation, okay. (()) (43:25) now in 2010 or onwards some maybe 2008 onwards we had a good facility now to make the devices circuits also, no one makes circuits but at least devices, at least study of materials, technology is being worked out its good to work on technology and see what is going on.

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Because unravelling a mystery is the noble prize winning work, okay. The directions of the crystals...

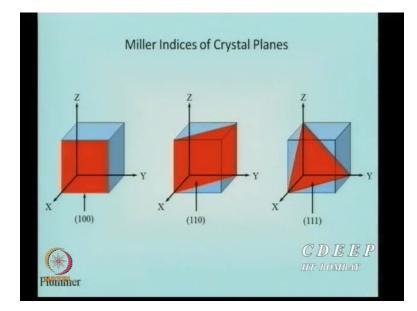
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The way it can be shown in a cubic is the following, you can see from here, you can start from any point, so ACB are the corners they say then you can either take x here y here, so this is your origin than the x, y and the top one is z each have a lattice edge a,. So you can see if I have or each BCC FCC I have actually shown the same directions and then we define planes, okay.

Once you see xyz you can at least make one lattice, one cubic and you say xy and z but these are arbitrary can call zxy there is nothing very specific it is only a matter of my decision or people whose copy I am making their decision. So once I decide this is my axis, okay and this axis is easy because it is an orthogonal system.

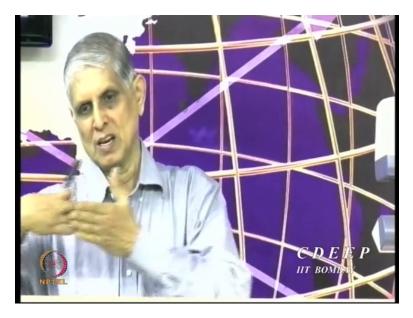
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So plane which has for example which is changing in this case, this is my origin, so X is on this side, Y on this side, so what we define a plane is, we find if there is an intercept on whichever axis, okay that will call one, since this red colored one does not have any intercept on Y because for this plane Y remains constant Z remains constant but X is (()) (45:35), if I move like this X will be (()) (45:37).

So I say it is 1 0 0 plain there is no intercept on Y and Z, so 0 0 is intercept on X you can see here, since there is a variation of this crystal (()) (45:52) like this, so this plane is moving therefore this has a variation in X, so it has 1 0 0 plain. If I want to make then I must take a diagonal of that and put a plane across and then there is Y and X both has intercepts where as Z is constant.

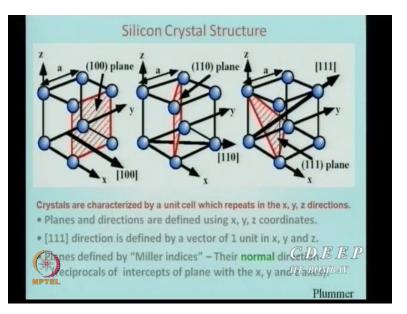
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So this is moving like this and therefore it is 1 1 0 and if all 3 are weaving then it is like a triangular shape plane 1 1 1, okay. So as I said in most cases the MOS transistors used 1 1 0 plane wafers and as I said recently we are looking for 1 1 0 particularly for FinFET, multi-FinFETs just now we are looking for maybe this may be a better idea, okay.

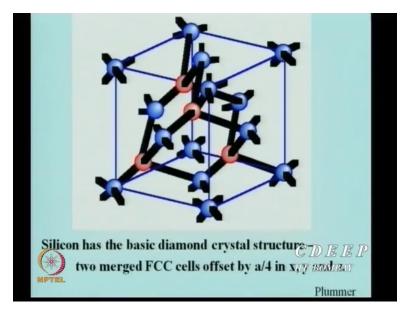
So why I am looking for plane? Because plane has something to do with mobility and since my aim at the end of the day is to get the highest mobility I will try to get, of course this is not the only way I can improve mobility but this is one possible way at least starting should be good then worst is going to happen and I will again try to improve on that and before that worst happens start should be as good as possible.

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Now here is a silicon structure you can see by the way we have not shown.

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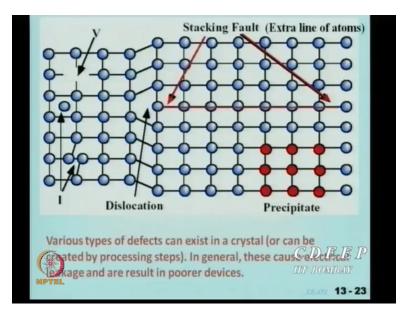
Here is a silicon structure which is most important, what is done in silicon is, it is a phase centered lattice, 2 phase centered lattice are interspersed post in, okay. 1 by 4, 1 by 4 and 1 by 4, I repeat 2 FCC lattice you take it, put inside get from one corner 1 by 4, 1 by 4 and 1 by 4. So if you shift 1 by 4, 1 by 4 the one edge of lattice from there will enter the first FCC near the corner.

For example this one, all these red ones these are the 4 which are 1 by 4, 1 by 4, 1 by 4 from the lattice age, okay. That is one of the atom, so from 4 sides the other atoms will be the above one, similar lattice will be above, so the other combination will go above, part of this will then go in the topmost portion, this 1 has come from one lattice which has gone in, this one has come from this lattice, the other is coming into the next lattice adjoining.

So if you now see it is a by 4, a by 4, a by 4 inside, okay. So there is how many atoms now I said? 4 from which are directly gone in, one from the corner and 3 from the surface, so there are 8 atoms in silicon lattice and what is the radii now? Because it is half off, please remember a by 4 is the distance, diagonal distance but actually radius will be half of that. So this is a by 4 only, so a by 4 square plus a by 4 square plus a by 4 square under root of that then calculate number of atoms divide by a cube get this number as 34 percent backing density but you see the lattice how much packed it looks, okay.

Now they are saying it is the most loosely packed lattice, it has only packing density of 34 percent, okay. Whereas FCC has 52 and BCC has even higher, what does that mean? That is packed lattice, so you cannot introduce impurities there. Whereas here seems to be little funny but that is what whole game is, a silicon lattice allows because it has the lowest packing density more impurities to come inside and therefore it can dope itself to N kind or P kind or any other impurity can be introduced. This is very very crucial in our decision to make any material useful for the device.

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Okay, before I go to the crystal growth there is another fault, you know there are some interesting fault occurred during growth. For example this lattice was being grown and suddenly we figured out that one atom is missing, between that the atom is missing, missing atom is called vacancy. Please remember though it seems fault as I keep saying it is a fault or a defect, if there are no defects particularly vacancies there cannot be any doping at all, is that correct?

Doping essentially is decided by available vacancies. So even if during the growth of the material you create a defect which you really thought it is a defect it has actually helped us to incorporate impurities. There is a possibility between the lattice there is 4 portions there is additional space between the lattice in between atoms that is called interstitial between the space available to you there is a space where atom can go and sit. So these atoms for example can be called interstitial. So this is another different which essentially is available.

Further if you start moving from left to right suddenly you find there is an additional plane of atoms appeared the red line, red line is additional atomic plane has appeared. The earlier ones let us say we have only 7 atoms in height, now there are 8. This additional atom you can see now the bonding is upper 3 are (()) (52:25) lower 4 but the one where the additional plane has no bounding with the earlier left part of it and this is additional plane, this essentially is called the area where it starts is called dislocations, okay.

You have dislocated the material and the plane through which this location is continuously seen is called stacking fault, okay. Stacking fault can be one dimensional, 3 dimensional, okay. And there is a possibility that this silicon atom may get some other atoms bonding there like Oxygen in specific case it is called precipitation. So the defects which during crystal growth one sees are the following one is the vacancy, interstitial and then dislocation starting for precipitates.

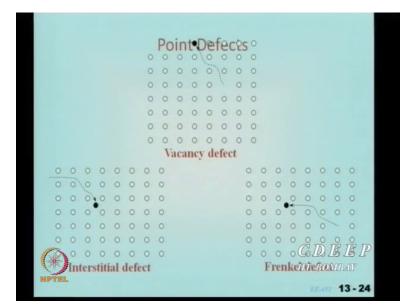
We do not want precipitates, we do not want stacking fault and we do not want dislocations but we certainly want vacancies, okay. So to create any device we need to dope and we need vacancies to be created, so we will see how they can be generated in actual crystal (()) (53:44), okay.

This is very interesting because these defects are material property during growth because you are going from high temperature to low temperature we will see this, this will appear irrespective whether you want or you do not want, you can make some correct gain to minimize this number, okay but cannot actually avoid it but certain techniques do (()) (54:09) most of the dislocation to move towards the age, okay outside the wafer or age of the wafer.

So the centre of the wafer is very good age is very bad, so we are (()) (54:22) he said remove them, okay. That is why if someone asks, are they circular? Wafers are always circular because you want to edge out remove all dissipation from the edges, okay. So is that okay? Extra line of atom is tracking fault because of which it dislocated the material and there are possibilities of oxidations or Carbon atoms may replace Silicon which is called precipitates, now these are essentially the problems in crystal waves and we will see now how crystal are pulled actually to get and how they are doped?

What kind of doping I am expecting? Uniform, if I say NA the wafer may have 200 chips, each may have 10 million transistors for each of them I want this to be known exactly, doping should be uniform because my designers have chosen NAS 10 to power 17 per cc and derive vt. Now if every part of the transistor is varying every chip to chip varying and wafer to wafer start varying then there is no way we can say that the performance is guaranteed because vj is minus vt is the current, vt is varying so is the current, so is the speed, so is the noise margin, so is the power, so everything varies as soon as this is not attained and therefore control is the major crux in all technologies.

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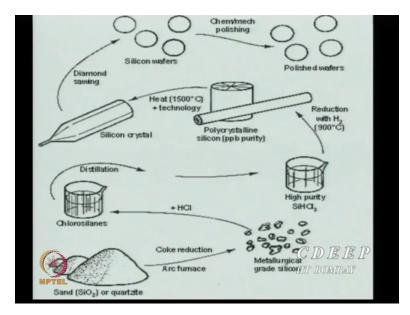


Have you been through (()) (55:58) technology, these are the 3 defects again shown here, this is 2 dimensional picture, one can see this atom is missing during growth, so it's a vacancy. This atom has additionally sat between the open space is called interstitial and this atom was otherwise fine but mood from one place to the interstitial side and by (()) (56:30), so what it did?

It created a vacancy, the pore of such interstitial and vacancy pair is called Frenkel fault. Please remember this has not changed the lattice, it has actually come and sat there. In this case atom during growth itself was missing whereas here the lattice was fine. However one atom during cooling somehow jumped, okay. So it created a pair of vacancy interstitials all of these will contribute to doping technologies as well as doping concentration availability therefore these defects are very crucial to know about.

At a given temperature these numbers will change, so as much doping will change as the available force with you, is that okay? Vacancy is missing atom, interstitial is additional atom in the void and Frenkel an atom moves from one to go to void area and lives a vacancy down is called Frenkel, is that okay everyone?

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So now we will start with crystal growth, Silicon dioxide is popularly available in the Earth as Sand, it is the second largest material on the crust of earth water is one, okay. Second largest material on earth is Sand, so as far as your supply of silicon is concerned it is like a sun source there is enough radiation for many many million years sand is always available, okay.

You required many small amount of Sand to create Silicon but there is enough number of sand or enough amount of Sand available. So we start with SiO2 and move on to (()) (58:30) finally wafers. So here is a quick path, okay. First thing that is the processing we will do, first thing we will somehow make sand to Silicon which is called metallurgical Silicon, Why this is called world has metallurgical grade silicon because in most skilled technologies one of the bio product is Silicon.

Actually in most skilled technologies to harden the steel we add carbon and also Silicon and so major metallurgical silicon is a by product which is actually not usable otherwise by any industry since the actual available source, so we need not actually need to have sand, actually so much mg grade silicon is available from steel industry it can feed another 50 years for us and this will continue to go so much so it hardly have to do conversion from sand to mg grade.

But let us say if I don't have silicon industry then what? So I have said say steel industry and I can go to Mumbai one of the beaches collect sand, so here is san to metallurgical silicon I treat it

with hydrochloric acid and we will see what? And I convert it itself into a gas or liquid depends on kinds of treatment I do is call Chlorosilanes. I may distil it, by distillation I can improve the purity of particular Silane I use, we will use surely this then I get the high purity Trichlorosilane as shown here.

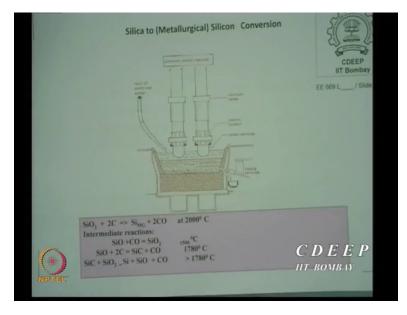
Then I passed through a (()) (60:16) which is called poly crystalline silicon this, I reduce this Silane, Trichlorosilane into Silicon and it deposits by process called chemical vapor depositions then I actually put it into some kind of reactor which is called Puller where I actually built the poly pieces, okay. Heating by1412 and above, once I start heating the silicon it melts then I put a similar crystal on the top, okay. Touching this liquid and start pulling that single crystal rod, if you have done, these days no one does experiment at home but just for the heck of it.

In earlier times we had in 5th or 4th class an excitement to be done at home to both sugar crystals and sodium chloride crystals at home, so school used to supply this so-called Horsehair you have to tie up with a good crystalline material which make a solution, dip it there and you say that will grow up next few days, okay. This was an experiment done in 50s by me and same technology used in silicon nothing great.

Once you have a rod of crystal which is highly pure then you actually saw it, cut it into wafers, polish it and these are polished wafers available for you, okay which is what our technology is, so today start with these, at least 1 or 2 of them will finish and we will show you how do I go about from sand with the polish, sand is done cheap very very cheap, just to convert from here to here you may have a 1 billion dollar industry to put. From here to here another billion dollars, okay. So to create a polish silicon wafers is a very huge costly business, okay.

This poly silicon is very interesting material because this is most likely to be used by solar cell people because it is better than Amorphous not as good as single crystal but cheaper, okay compared to the actual wafers you get. So the current technology for solar cells is essentially using poly silicon and of course their efficiency is not 24 percent of 28 percent they may have 12 percent to 14 percent efficiency, Amorphous have 3 percent, 4 percent, crystalline maybe 24 percent, 28 percent even higher these days in some other materials Silicon of course is not showing maybe, so we will see to first process we will go.

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You can see from here this is a reactor in which this is a Quartz reactor, okay and with carbon liners inside, okay. These are carbon electrodes, what is this furnace called? It is called arc furnace, okay when you apply electric voltage across the 2 electrodes depends in between it creates an arc, arc temperature can be 3000 degrees centigrade. So you have arc furnace, okay.

You introduce Quartz and carbon together from the top, here due to this arcing between the 2 electrodes the temperature here is around 3000 degrees centigrade it melts silica, okay. 3032 is the actual melting temperature but it starts melting but we have already introduced carbon along with it and here is a reaction which happens there, the final reaction is SiO2 plus 2 carbons is Silicon MG grade plus 2CO around 2000 degrees centigrade somewhere on the top surface, sorry lower surface.

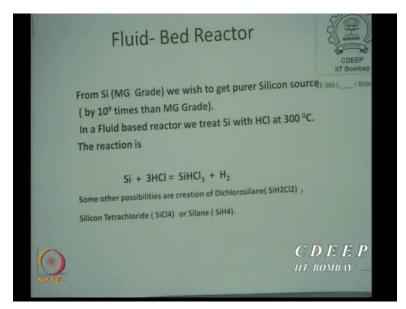
Why lower surface? Highest temperature is here actually where the arc starts, okay. So we get silicon grade plus carbon monoxide and that is taken out, okay. And you can see the liquid this actually comes out is collected into Silicon metallic grade and it solidifies, okay. There are intermediate reactions for those who feel I might had suddenly wrote this, so there are many reaction.

At around 1500 degrees the SiO2 breaks into SiO1 and SiO plus carbon monoxide reacts with (()) (65:05) SiO2, Si and then carbon dioxide then this Si also reacts with carbon to form silicon

Carbide and silicon Carbide and SiO2 themselves react to form silicon SiOCO and this is multiple reactions keep doing and around 2000 degrees centigrade the final reaction SiO2 plus 2C is Simg plus CO is the final reaction there are some more in between but I thought too many will not, you will feel bad how much chemistry, so I thought okay this is enough.

So you can see using arc reactor the first process was to get Silicon out of Silica, so we got it now? So once I get this material then since it is collected somewhere in the truff when it solidifies you actually break into pieces as shown earlier, okay. This is Silicon metallurgical grade this.

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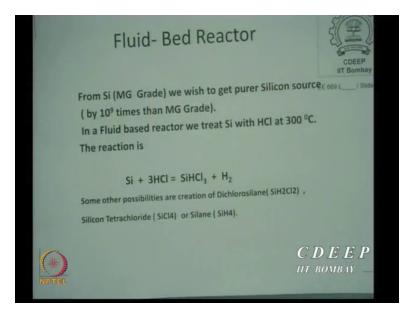
Now I want create from this I like to convert into pure silicon, metallurgical grade silicon has many impurities, almost all kinds of including carbon is the highest but many other impurities Strontium is there, Nickel is there even the Iron is there and sulphates are there, so many impurities, so that is not a good silicon material. I want to create highly pure, why I am looking into highly pure Silicon?

Because I am going to dope this Silicon wafer or silicon material by a given concentration of impurities typically silicon concentration is 5 into 10 to power 22 per cc for a given wood silicon I want to dope it 5 into 10 to power 14, 15, 10 to power 16 per cc, 17 per cc which means I am

doping roughly 1 part per billion or few parts per million, so if initially itself there are impurities and I introduce afterwards I don't know how many I have, okay.

So I want to make highly pure Silicon to start with, so when I start introducing impurities the concentration which I want, I want to achieve that because my circuit performance is hurt on that, so I am always worried that initially wafer should be highly pure, as pure as possible and only dope with the impurities of my choice to a given concentration, okay.

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So this first process to purify it is using a fluid bed reactor, essentially I did not bring because a big figure. One can see you treat it with Hydrochloric acid and it forms whether it is called as Trichlorosilane and this is very low temperature process it is around 300 degrees centigrade Silicon reactor with HCL and you form Chlorosilanes. Now why I wrote only one of them depending on the temperature I choose I think some chemistry you may read there are 2 ways of reaction to happen.

One is called the thermodynamically controlled reaction, the other is called Kinetic based reactions. In this case it is the thermodynamic based reactions which I am controlling. So if I change my Gibbs free energy, what is Gibbs free energy? Anyone? Nobody teaches Thermodynamic in IIT but you would have studied it somewhere else. What is Gibbs free energy?

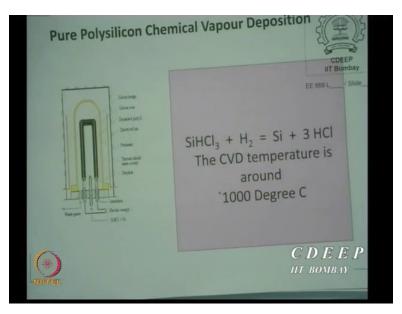
If you have done thermodynamics course very first few lectures we introduce the term entropy which is the measure of disorder it is delta H which is called energy of formation are called enthalpy, so H is enthalpy and S is entropy, so delta H minus T delta S is essentially your delta G change in Gibbs energy. So at given temperature this both H and ST, delta S can change and because of the delta G can change.

If it is positive reaction will be from left to right, if it is negative reaction will from right to left that is what the thermodynamic reactions are, okay. So by making a choice of temperature I can create varieties of Chlorosilanes one of course is Dichlorosilane SiH2Cl2 then I can pure (()) (69:53) monochlorosilane also SiH3Cl I can create all chlorine atom replacing Hydrogen these 4 atoms for Silicon, So I will get silicon tetrachloride SiCl4 or everyone gets only Hydrogen out of Hcl and we get what is called as Silane SiH4.

So essentially we say Silane if I replace 1 Hydrogen atom, it is monochlorosilane, If i replace 2 hydrogen atoms it is Dichlorosilane, If I replace 3 hydrogen atoms I get Tricholorsilane and if I replace all 4 hydrogen atom it is silicon tetrachloride. Silicon tetrachloride is a liquid all others are gaseous forms, okay. Silane is very very highly flammable material, what does that mean?

This English (()) (70:46) also changed in my time we used to call inflammable materials, okay. Inflammable material means which takes the fire fast, okay or which fires itself fast but off late Oxford dictionary in last 30 years said inflammable may actually contradict to flame therefore it is only called flammable. So SiH4 is extremely flammable material as soon as you release in the air the 27 degree centigrade hydrogen will blast it out, okay.

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From silicon Trichlorosilane we want to create polysilicon and please, you know in between I forgot this Trichlorosilane is done what is called as fractional distillations, we have done some chemistry we pour some liquid in the condenser and we even have a knob at the top, we collect it at the top, so every has a density so it collects at different this cooling and therefore you can have your silicon, Dichloro silicon gas coming out at one end of the port.

So once that highly pure Dichlorosilane gas is there we use another reactor which is essentially called Siemens reactor there are modifications to Siemens reactor but process is similar, okay. So you can introduce Trichlorosilane you can also introduce Silane, Dichlorosilane anything but I have used the most famous present-day technology Trichlorosilane.

So what I will do is, this is you can see here this black portion is called Silicon Bridge internally there is an electrode which is a silicon pore, this is an electrode and this is silicon pore, this is poly silicon rod inside which we have heating element. Now what we do is, we connect this heating element to a power supply this is an inverter based system which gives pulses of power, okay.

We even need power electronics when we make this then we have a reaction which is around 1000 degrees centigrade Trichlorosilane reacts with hydrogen which is also introduced to pure Silicon and that silicon deposits and this is normally kept in a particular vapor pressure which is

essentially better than vacuum, so it is filled with nitrogen, okay. It is first evacuated and some nitrogen is filled and then only hydrogen reaction starts.

If you do not do this, hydrogen may still blast it, so there is some level up to which hydrogen should be allowed in. These are all precautions which you actually take when in the lab as well. So what happens? This rod gates silicon depositions already available and keep this is called chemical vapor phase depositions CVD as the word. So the rod becomes thinner to (()) (73:46), okay.

And after sufficient amount of thickness which it can hold you stop the process take this out. (()) (73:54) all these highly pure poly rods into small pieces which are called Nuggets and these Nuggets will then be used to create single crystal silicon rod which is what we are shown that is on Friday.