Fabrication of Silicon VLSI Circuits
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Lecture No. 16
Lithography.

Ok so far we have done crystal growth, we have done diffusion, we have done the Integrated circuit lab facilities, what are they? And we have also looked into last time the thermal oxidation which was the major activity as far as IIT Bombay microwave (())(0:38.4) is concerned. We keep working on MOS MOS MOS or name like that MOS. So let's look into now further and we had started last time something called in lithography. And why that is the most important process, lithography, LITHO stands for some kind of sculpture of some kind of image 2D or 3D image or 3D material or a statue anything Litho. Generally made out of some metals for stones for something. So lithography the printing that you see and somewhere else is called lithography.

The major most of you have I don't know how nowadays the cameras are available you don't need to do what I am now going to say, in my not really childhood when I was young enough we used to have a camera called box camera and it used to work also black and white simple pinhole and it used to flash. So how was it acting? So same process which we do on a photography problem transferred in the lithography here. We are trying to take and image and transferring somewhere. So now this is like in photography what is that you have a film which is coated with some emulsion and the emulsion film is inside your camera you press the shutter it opens for a while given 10 seconds or lower depends on the resist you have there. And as the light shines on the emulsion part of the emulsion is converted into, this is normally silver Sulphide or silver chloride which is emulsion plates.

And silver is reduced to silver and that becomes hard light cannot pass through silver. So the way we do it there then when you develop the rest of the emulsion goes away except this silver part and that's the image. So if (())(2:48.7)this is the portion where the light did not pass come there so we say that the human image has come there, exactly the similar process. We expose and you develop you actually have to stabilize there are few more things you have to do so this is photography which we have been doing from ages. The person who actually did this has the name Stanford; he is not the same the Stanford University men. But he has the world patent for

image this the first photograph that he took was a running horse that fetched him the patent. So you can imagine what reality could be, till now we are following that. The only difference now we have instead of emulsion plate we have some kind of pixels which are made of CCD or some other kinds, (())(3:42.8) buckets and actually light shines on that.

So whenever light shines or doesn't shine something happens on this charged storage or not storage and that is the image that it stores and since charge is the one that we can easily recognize electrically so one can convert into so much charge one and so much not charge zero, so one can digitize a picture, earlier we used to have analogue now we can do digital pixels. Large number of pixels how many gets exposed will decide size and accuracy of the picture. Identical to this what I said is done in lithography okay.

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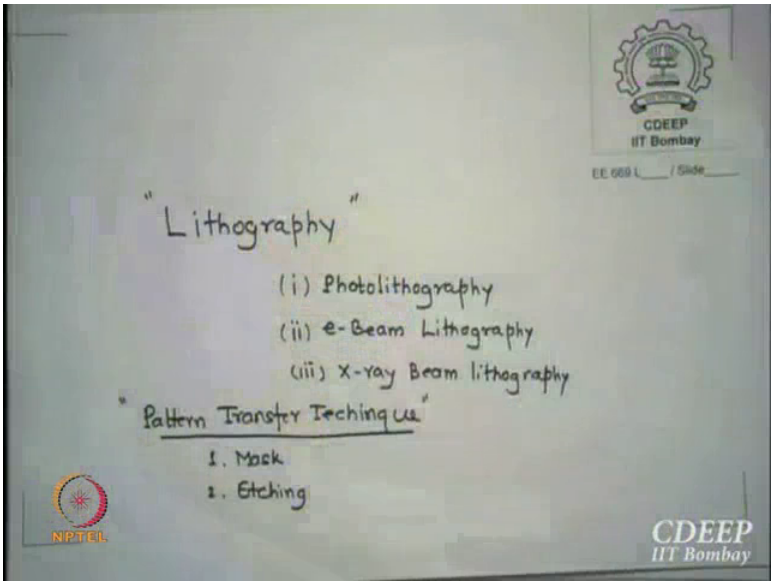

So the word which we used last time was photolithography, E-beam lithography and x-ray beam lithography. Of course x-ray will never come probably will remain in text books of course it's very costly and it actually affect the Silicon devices. So normally the radiation effect it gives so normally X-rays are not preferred and its mask is very difficult. You need a leather mask it's tough to handle. There is a 4th one Ion beam which may or may not at all ok. However E-beam lithography and photolithography will continue to work for us okay. We will see both of them, even now for at least 28 Nano-Meter Technology notes or even 22 we are still working on

photolithography. Now this word is slightly not clear to you but soon it will be that what is this feature has to with lithography or photolithography.

If you see any light shining through a lens on an object so the way it is that normally a convex lens if you are keeping a source of the light somewhere closer to focal point, then parallel beam will come if the parallel beam appears it will focus at the focal point. So this simple optics is still known ok and we still use that. So now we say that apart from the lens been what it is, it has a (())(5:58.4) of 1.45, but it has a curvature, it has a dia which is coming from a sphere this lens is cut actually. So there is a dia associated with it. And there is also what is called radius of curvature.

So now these terms are very popular in optics however we will require some of them if not all of them. There is a word called numerical aperture, there is a word called mean time functions, there are many terms relay fringes, Fresnel fringes all these optical terms are required because light will behave as a (())(6:35.8) it will defract, it will have (())(6:37.7) it will have all possible 7 possible evolutions. No we want to wipe this because smaller the image we want to create smaller aggression that I am expecting. Is that clear? So sharper image and a smaller image I want, that's what the node is asking. You go from 65 to 45, you say 0.7 times I will reduce everything. Now if you reduce the dimension, the image also has to be accurate even at the 0.7 times. And you go down further to 45, 32, 22 and maybe 0 later. Not this progression of technology node essentially depends how good is your lithography. The word that we use often there is resolution. So before we start something I will show you what is resolution?

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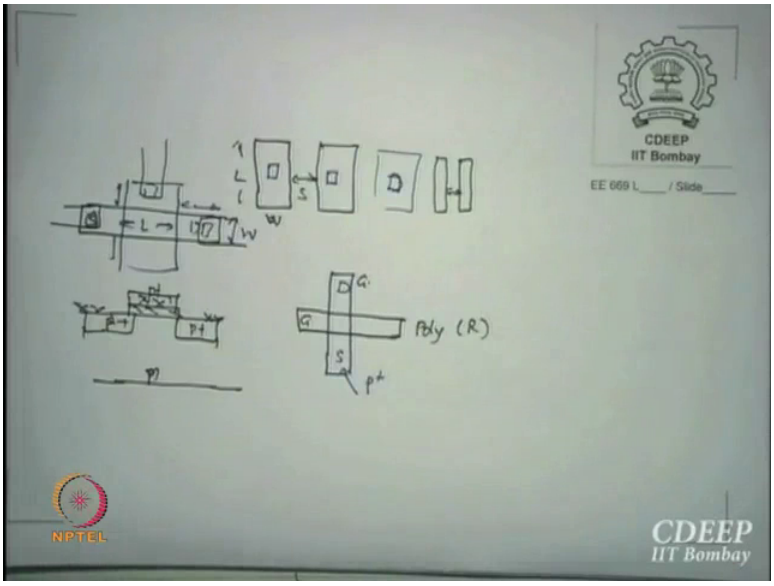

This is called smallest pattern which Integrated circuit will actually require to print on silicon. There is another one very close by and this is separated by some distance S let's say this is W this is length. So I want not only W capital L to be transferred as it is but I also I want separation between two patterns also identical same as, if there are multiple such patterns they should be separated identically everywhere by same amount and W (())(8:08.8) should remain constant throughout for each of the patterns. This is what I am expecting at the end of the day. But if I reduce the dimensions the problem right now I am getting here, this is called resolution. Separation of two lines or two patterns this is called resolution. How good you can resolve? Two lines how close you can bring they still remain 2 separate lines this is called resolution. So one of the major feature of lithography is, how to improve or how to get at least the available these resolutions okay.

Because in integrated circuits these days you may have 1 million transistors on a 2 cm by 2 cm chip or maybe slightly less, 2 by 1.5 3 square mm, 3 square centimeters. 1billion transistors will require your number of interconnect used number of transistor areas and they will have smaller patterns everywhere. In general the digital designers sorry that designers actually provide output of a VLSI design course is these patterns ok. This is what we actually designed there, from the circuit simulation, from the system simulation, to RTL, to VSDI, finally to circuit simulation and layouts. The layout is the one which is your last output, which is called the pattern generations.

Once the patterns are available you transfer all of it and you transfer at the word is called Tape Out. So you actually create the patterns on a, actually earlier we used to have mat tapes and since we used to send the mat tapes to our house so we used to called tape out. Now no one send that it's a GES transfer data even on the internet okay and there for there is no necessity or sending CDs or DVDs or Tape or anything the data is just transferred.

Now this essentially is what is called tape out for a company. If you go to any company which is the design company generally a white board, nowadays there are screens like this bearer companies. And they will keep showing how (())(10:23.6) they are and for each of them they will have a tape out page. All engineers can go like here 120, 124 never show up its ok there also no one forces you to come. But that paper out board cannot be miss or some end sum exam date cannot be changed okay same thing.

So you come anytime then 24 hours, at the end of the day you must use tape out and there has to be a lot of verification and a lot of design goes on, so this is what essentially we are trying to emulate here. Tape out if you have to create I must create patterns. For example I don't know we don't have colours in VLSI normally the layout is actually explained with colours because each layer like diffusion, implant or Poly each are given some colours so that I actually do what I really want to show.

So for example if this is my P region fusion done which are my source drain diffusion maybe P Plus. And if I intersect just buy a Poly this is normally green this is normally red. If you have a layout editor somewhere on the screen you can see a pink line a pink this intersecting the this. Now this is a transistor, this is a gate, this is a source and this is a drain, source drain are identical so it can be ascending. Now this is the one can say the pattern which you seeing is essentially plan. But what goes into silicon is something like this, maybe I will show you differently. This is my source drain and this is my oxide and this is my gate, ok this is N substrate p plus p plus, this is also P Plus.

So if you see a cross section in a wafer I see a transistor in this. But if you look at the plan then you can see this poly which is the gate, maybe here is a metal per source drain but right now I am

not showing. So corresponding to this there will be a diffusion term diffusion line which is from here to here and which is intersected by oh sorry I change the colour but doesn't matter for this. This is my source drain, this is my channel length and this is my channel width. Rather it should be other way lengths are normally smaller compared to widths. So this is the plan and this is the cross section, now days since electrical engineer do not learn drawings so they may have some problems but one can still visualize ok. So Mechanical drawing was a compulsory course in all B tech program earlier, now of course even mechanical don't have so then why should we have.

Yes interesting things are happening, they say everything can be done by simulations so why do it. You can't simulate your food inside if that can be done that everything is solved. You have to still earn money to cook food eat food do everything which is reality. But when it comes to doing something you say it can always done by simulation. So if simulation works for everything then it would have been ok but it's not true so let's learn what is reality? So if this is the plan which, there are two masking fact. This is one mask and this is the other mask. Mask means selective area of poly, selective area diffusions or implants are essentially possible if I protect one area and do the other process therefore these are called patterns which act like a mask for the other process.

So a designer essentially when he finds out W by L through circuit simulation or through many other simulations all that he gives me is W by Ls. Then if I want to interconnect, I open a window somewhere here in the source drain. I can open a window I can a window and Gate and then metal can one, so another masking is required okay. So if I have to do selective area processing I must generate patterns which are masked for next step. So this is what the designer will give, the technology has to do. So what are we expecting whatever designers have done should get transferred on silicon as it is. Because you have used that simulations lot of simulations to arrive at this value for circuit performance. You say I want this much speed, I want this noise margin, I want this plan outs. You have designed everything on that basis, and now you say that okay is transistor as these W by L, these are the connections and this act as a circuit. The process has to follow what it is.

If process cannot follow then the circuit performance will be different from what you have design and this may happen. So what will you do, we will see. Actually before actually committing on silicon what we do is whatever pattern we create interconnects for all of them we extract back the circuit. From the patterns we actually create the circuit back and we re- simulate and if the initial simulation result do not match the extracted one we tweak our circuit data. Again we will keep doing till this, extracted result is same as starting result, starting data. This is then transported to Silicon, you thought oh simulation has been performed back extraction has been done, so it should work. That is only the computer as a tool it has shown it will work. But when it comes to Silicon it does not behave the way you wish it.

So how does this technology people tell designers that ok unless you follow certain rules I cannot guarantee what you are I can transfer, these are called design rules. that is what technology people give the constraints and these are available to designers to follow during they are pattern generation if you follow them, then hopefully silicon people will say ok I can now make circuit to your spec possible. And when we still harass maybe one more turn around may be required before I get out of everything. But that is the cost involved. So please remember what is the whole procedure we are looking into and since we are from drawing two patterns we are trying to transfer, just transfer is the major activity in the whole Integrated circuits.

Typically a CMOS process may require as many as 16 mask minimum which is what Plummer and Griffins book has shown but may require 24 to 32 marks depending on additional feature you are creating. So these many masks so what is the problem you can see from here this pattern of a gate and this diffusion area there has a limit which will come how much distance minimum you should keep how much the edge to edge width we should keep these are design rules. But when you really transfer them follow equivalent rules. So how good they follow? And how much tolerance you have which is acceptable? This is what we are really looking into process that how much tolerance it should have.

Now the problem is alignment, there will not be a single transistor there will be millions of transistor. For example these are something. So I want to open a window here I want to open a window here and there are N such everywhere. But these second mask should get inside on the

last pattern okay. This is called mask alignment, so we are worried about the first mask I print so one image I can see and I print this second mask for the second process. I must see that the next pattern sits with where I expected all the million and billion transistors on chip. And there will be on a wafer hundreds of such chips, so each such chip will have each such billion transistor, everywhere this pattern should fit inside that's call mask alignment.

So you need a mask alignment system in which you can create multiple chips at a time, that's what the cost goes by number of good chips available per wafer and therefore one has to make the reliability so strong, yield so high that you can make some money ok. The typical lab I just said 14 nanometer lab has pass 6 billion dollars to Intel recently last year. And (())(19:54.8) it's not over they are still trying to make UV systems which may cost another million dollars. So you can imagine how much money they pump to just go to process which will have 11 nanometer circuits. Why are they looking at l1? Because they feel if I can pack more transistors on a chip larger systems I can build and a larger system more likely to work better than the distances apart reality wise and therefore more money I can generate. So that the investment.

That you are going to buy all kinds of electronics next many years and that's the whole hope that every 10th day iPhone iPhone 6 7 8 9. Because of that happens and you keep buying only then the Apple will survive otherwise Apple will wind up in no time. Apple has invested so much money it will not be there if you don't change the phone you don't stand in the line at night the whole night to get iPhone 6, god knows why but that's what people do. Ok so is that introduction clear what is that we are planning and what is that our effort is and why are we are so much worried about transfer of images on silicon. So selected area is all that I am processing I am looking for. And maybe configure I first show you and then maybe I will show you the actual something I will show you this is lithography.

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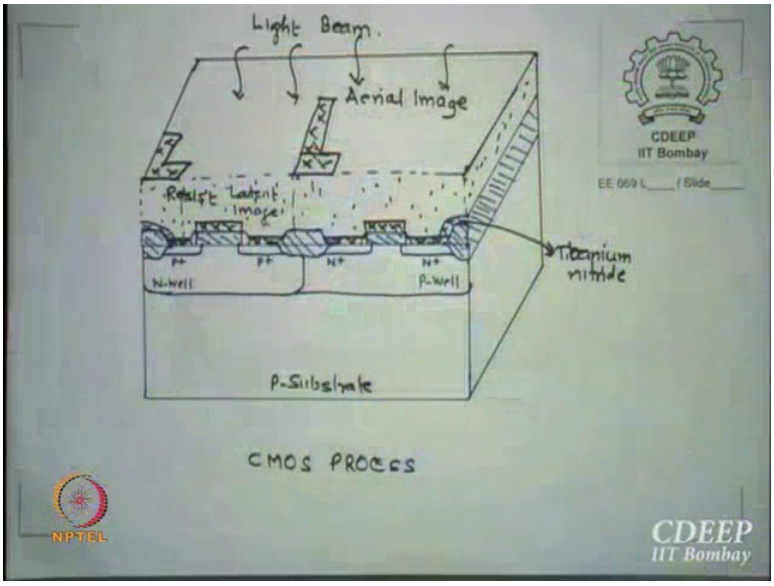

This is very simple CMOS transistor the way we start this we start with a P substrate, avoid that I have made a three dimensional even books has it so it's not very novel or something. This is three dimensional figure so please remember MOS transistor is a 3D device tough patterns are 2D but in reality they are 3D devices. So normally what do we say this is length X, may be this is sorry this X, this is Y and this is Z, so all three dimensions are required to actually model a MOS transistor. Then we do a lot of physics we say one is longer than the other electric fields die down after sometime so we used to 2 dimensions but that's only a matter of decisions.

Ok so what we do is we start with the substrate and create two reasons one is called N Well and the other is called P Well. Now one can say for N transistor and NFET or NMOS transistor I need P substrate so it was already available, they are doping's are not very much what I wanted. Normally I will start with a very low dope vapors and then I will create N Well and P Well areas to make my p channel and n channel device So P channel device will come in the N Well and N Channel device will come into the P Well. Now these two are implant regions, so one process which we will do next time after lithography is implants. Now one can see there is a thick oxide here some interesting features of oxide which I did not do last time I thought maybe processing time I will show you have this upper lower thicker oxides are drawn very interesting method, this is called local oxidation of silicon so we will see that.

So we need now first mask to create this must be in this P Well will be open area where P diffusion implant will go. At that time all other region should be protected is that clear? When I am making a P well I must close sorry I am making N well I must shut every other region so that impurities other than N type cannot go anywhere. So first mask should be to the well mask in wall mask. Then I will put another mask which can be a very interesting thing we do it it's called Minus Mask. Whatever N Well masks I can use N Well minus mask which is complementary mask for that. And I will use that, so it will open P Well but rest of the areas will block, so we would say N Well is blocked and I get P Well. Once I make P Well I will again block N areas and actually do gate first. I can do get both sides together so this thin oxide I must open windows I must put some weight thin gate oxide on both regions to make for both N channel and P Channel.

Then I will deposit poly so I will restrict Poly only on the gate rest area poly should go away. Then I will implant source drain, so when I am doing for N type transistor, I will do say arsenic or phosphorus and at that time this area must get blocked okay only N should come here when I will do P Well aa P channel device this area should be blocked and only P impurities should be allowed. So there will be 2 mask just for making source drain. Same will be diffusions on poly as we do, then we require contact so we must open contact to source drain source drain source drain also to poly somewhere we will show you. So we need contact where Silicon will be made available for metal to connect. But the overall deposit metal it will go everywhere again the process is universal. I cannot say selected depositions are very deep so I will deposit everywhere and selectivity etched the rest which I don't want okay that's called mask. So rest area should be etched and some areas do not get etched is what mask will allow you.

So again I can open windows here, here here I will put metal on this and etched out metal from these regions one metal here one metal one metal here and these two metal may connect to each other and I am a CMOS. Now the way we do it in general for every process step there is a resisting on the wafer there is a resist. Now what is a resist, it's a word photo resist as the word for photolithography we will use. Now this is the masking from the mask patterns, this is the image which is sitting on the resist layer. Let's say some pattern is sitting on the resist layer, but just image must transfer below through the resist thickness, is that point clear? There is a thick layer of resist the patterns are sitting here because your mask is sitting here. Now this light may

pass through and allow on the top surface this image to be transferred, but I want all the way it goes to full thickness of the resist. And whatever dimensions I had there should remain as they (())(27:09.1) go down. This is the actual challenge photography the image at the surface of a resist is called aerial image.

So from aerial image to Silicon image it should be as good as possible and there are many problems in the resist and it does not allow aerial image, firstly it's from the mask to areal image there will be some airs. And from the aerial image to the Silicon image Silicon surface image is even different. How good you are 3 match is your expertise and the cost involved on actually making as good. So this is essentially lithography process. So first thing is you must have a pattern which will have some dark and this region we will show you this little later. And once we shine light the dark portion light cannot go the clear portion light will go some resist will get light some resist may not get light and once resist properties are used some resist get hardened some resist get softened we will see that little later is that okay?

So this lithography is a pattern transfer from circuit simulator to layout, Layout to mask plate, and then mask plate to actual silicon surface or whatever the layer actually we have. This is the image transferring and there are so many places where things may not work to your advantage. So that tricks of the trade and design I mean processes how good you match (())(28:46.9) okay. And the cost keeps increasing how better you try to do it. Now this is the issue which probably have been bugging Gordon Moore from ages what Gordon Moore thought that lithography will always match my thinking which probably it did for a while many years.

He said OK 0.7 times the dimension will reduce so lithography should be able to resolve at least 0.7 times whatever value earlier and therefore I can print the same what I was earlier I was doing 0.7 times that I can still print. Next time I will come and other generation 0.7 times. So lithography keep this with whatever Moore was, Moore was always thought I have 40-50 years okay. But lithography would not match initially because that is what was the crux of the problem that lithography could not match Moore's this. Then he said 2 every 2 years, and he said every 3 years, now he may say every 5 year, he is still surviving so can be another Moore's 5th law okay.

So these tricks have been become because lithography was becoming a bottleneck at the end of the day.

So we are talking of a 7 Nanometer process, any optics 7 Nanometer is 70 angstroms. Smallest wavelength of of light which you can use even if you have deep ultraviolet as you say maybe 1000 angstroms or 500 angstroms, we are talking of something now 40 Nanometer 70 Nanometer aa 7 Nanometer 70 angstroms so the wavelength of the light is certainly much larger than the dimension that you are now looking. So all kinds of optical errors will come because you are trying to resolve a line two lines are dimensions of each line to be same which light which is always higher in their wavelength. But then human mind is very great, there are number of lithography techniques which probably still matched it and we still we will show a graph at the end or maybe here itself if I have to show you that ok before I show you that, this is my I don't know I don't have maybe but so ok.

So this wavelength of the light was the major crux how small you can go 7 Nanometer I would have expected 3 nanometer lines. So that is ok that is great but 3 nanometers 30 angstroms there is no light actually. Sorry even 70 Nanometer 70 angstroms is a….So what we thought then that the wavelength is proportional two a C by lambda is essentially energy is that correct? If you are talking about photons yes this is Photon energy so why restrict photons? I say I will use electrons which already higher mass compared to photons photons has no mass. So I say OK I will use electron beams then I realize it can reduce because there is a mass involved now with electrons. So I will be able to create high energies and therefore lower wavelength. So electron beams put lower wavelength than normal light put on wavelength ok. So lithography which changed over was from photolithography to electron beam lithography.

If you for the want to reduce the this you must have much higher, so you make ions for example which will have higher mass then high energy Ion beams can can have even lower much lower wavelength. And since they will have much lower wavelengths I can resolve even better lines but x-rays with heavy mass will also impinge on Silicon atoms of similar size and will remove from their position itself and create lot of mess in the circuit. So x-ray lithography all on this, Ion beam lithography was thought and then given up. It's not that it is impossible now we're looking

for what we call plasm immersion something and maybe if time permits I will show you what is current trend people are trying.

There are also interesting words which we will use like one is the, there is a word which come in Optics called numerical aperture and one cannot improve in numerical aperture so you put everything in water to improve a numerical aperture so it is called emulsion lithography. Then you do multiple lithography's so you will see one here one here some combination of lithography techniques I mean multiple exposures can create pattern of much smaller size. So there are multiple prints face friends emulsion lithography all these are techniques which we will not do it in so much detail but that's what 2012 onwards is now looking into. The problem as many of them are not successful and now the ultimate what we looking for is extreme UV light.

The extreme is typically I am looking for 10 Nanometer wavelength UVs and hundred angstroms or kind of that. And the machine may cost billion dollars and so far not a single company is successful in manufacturing defect free, I mean Intel is trying, Lemont is trying, even IBM have started giving up. So there is a huge cost and there is a very little return at the end, because how many people will really require 7 Nanometer chips that is also a market issue. Should I invest so much that the microprocessor market we'll bump and if it doesn't then what will happen this money will go waste. So companies always worry about how much is the market available so how much investment CA does a (())(35:02.6) and the company goes phat and hundred thousand people are removed okay. That's the way industries work.

So please do remember that your job is always at the chopping block any day any company can released thousand people in a day ok. That is called pink slip Aapke Haath Mein. Gaming is one area where technology is very highly required. In most games we used require excess speed we are looking for high speed. Now there are methods of improving high speed without actually doing great lithography you can do puzzling you can do pipelining can do many games in the gaming itself. So yeah I mean human mind is always thinking different which is good actually. Now what is lithography looks like?

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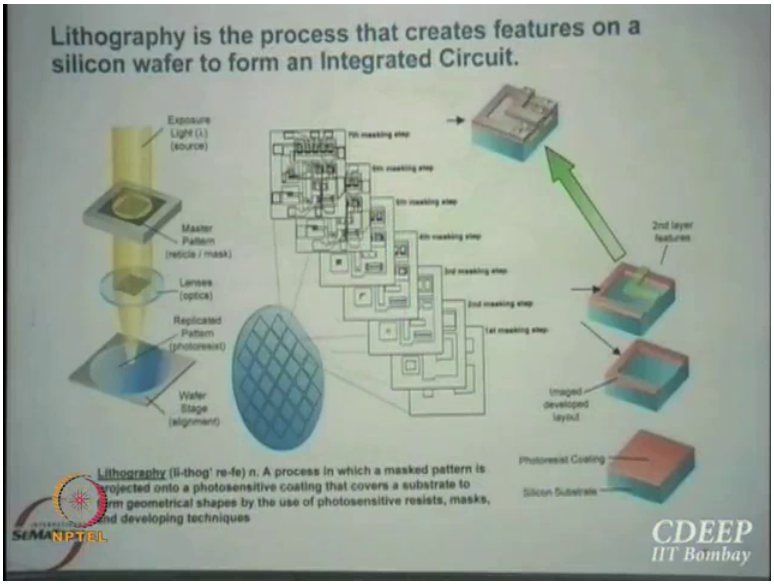

Here is a figure taken from semtech, semtech is a combination of it's a company which is funded by many companies including IBM and many others like Texas and they do research. And those who are the participants in the semtech program if the technology is developed by semtech it is given to every one of them it's now free because they have already invested. So its anyways free of cost but the semtech companies very important people who actually give developing new technologies and they get funding from variety of companies and they patent them only for these companies okay. So we can see from here the way it is I will come back to this again there is exposure of light there is a master pattern which is called reticle. Reticle is the image what is 4X 5X times the real actual dimension we are looking for.

So X is the actual dimension, 4X 5X earlier in my time we used to have 10X size so we used to call reticle as 10X, now it is 4X 5X. So one transistor pattern only is first taken and done repeated N times wherever (())(37:17.4) we will see that. Then this is done through a optics this pattern is transferred hear through a resist ok. And one can these are the number of mask you can see there are 7 mask that are shown here in which patterns are getting aligned one over the other ok. If you want to see a simple thing you actually got a photo resist on a wafer, let us say I want to develop this image. So I have a mask which has only this much pattern and I shine a light. Light doesn't go through this area wherever the Mask is kept and the other is exposed to light so the resist becomes soft whenever light shine the resist remains hard wherever light doesn't shine

it's a positive photoresist. And in that case the etching of the rest area is possible because the hard resist doesn't etch, we will come back to it.

So you keep transferring images one after the other over this using mask ok. This is essentially lithography technique and you can say as I say these are only 7 mask process shown here. Typical NMOS minimum requirement is 4 mask to 6 mask, generally 6 mask. Even in 4 I can make an N-Channel device okay. I cannot make a P-channel device in 4 mask may be I will need 5th mask. But typical mask set required now may be as high as 16 minimum for CMOS and can be as large as 36 mask for some special requirements okay.

Student: (())(38:58.8)

The actual dimension of the image which I showed you sorry. Let's say this is the dimension, so I will expand this 4X times, 4 times and I will put that as a pattern and when I will reduce it, I will get X below, is that correct? I start with a reticle which is earlier it used to be 10 times now it is only 4 or 5 times so it's for reticle. So this is called reticle okay now reticle is larger version of a pattern whatever you want to final. So it may be 5 times that. The reason is because light there will be a optics problem so we first start with a bigger dimension and using lens system I reduce down to a actual dimension. Is that clear? So this is reduction okay? The first stage is reduction, second is repeat will see that to do it, it's call step and repeat we will see this work again.

Student: (())(40:02.1)

If you're writing with electron beam you don’t need, if you're lighting with mask, if you're doing a optical mask yes you require 4X reticle. Okay you see light is required, electron beam generally you can direct (())(40:18.1) we will see this okay. You don’t confuse it with, that is done only on silicon wafer is that clear? This is mass generation, what we do is first create and optical mask we will come to it, and then use it on every time on silicon. I am right now creating a pattern on a create a mask itself, and then use that mask to paint on silicon, is that clear? Direct writing what he is saying is only done through electron beams and not through optical beam. But it will have laser writing, but laser writing can be done for a smaller dimension chip and for a

small area you can do. If you do repeatedly it itself gives lot of error and heats up of the wafers okay.

So those who have worked on a lab they immediately can guess what can happen. They are not probably may not appreciate but there are issues which are lab issues, things do not work then we discard it. So this is at the end of the day you can see you start with the single pattern and one over the other you keep doing and you get a multiple chips on a single wafer, it can be an area of 20 by 20 it can be area of 100 by 100 depends on the size of the wafer and the chip size. If you have 2cm by 2 cm chip, 4 cm square. Even if you have 16 wafer you may not more than 40 by 40 area okay. Now this depends on the size of the chip you're using and depends on the wafer size you have. Number of chips per wafer, one can decide okay. Earlier ones we used to have 2mm by 2mm square, 4 mm square chips are very small even RF amplifier presently which may use 90 nanometer or 0.13 nanometer process they require area 4 mm square.

So even now the companies actually sell the cost per mm square. I want to fabric they say okay 4 lac per mm square or 2 lac per mm square but if you talk about processor that mm square will blow up and the cost may become in crores okay lacs will not be there. So normally analog (()) (42:30.5) chips are smaller component chips and they can be actually got fabricated out of individual transistor making and therefore they are mm square based costing okay. Typical cost which we get it through academic discount is 1 lac per mm square either in Germany Austria rather Austria Micro systems or Microns or in TSMC which is costlier okay. So how these processes are essentially where processing is done nowadays have nothing to do with the designers okay. Once you create your pattern thank you very much.

Then the technology people these are called hub houses or foundries. If you're foundries you can work for anyone okay, anyone who pays I will them, but many companies, Intel for example does not believe in giving many of their mask set to any other company. Even TSMC they gave only Pentium 1 after they started Pentium 4 okay. So they are not very happy with release of their process to anyone okay or release up the data. And therefore Intel has its own fab. Apple does partly own fab partly does with Intel, look at their own competitors. But Intel doesn’t mind because their processor part time some processors part is made for them now. Earlier Apple had

its own processor, now it is Samsung which is taking it. So every company has a deal with someone who gives cheaper actually buys from them okay. These are called IPs, you can buy IPs and make everything.

So typically IC processing has to be realizing this that design to practice is not same. And how much accuracy you can built is the cost in the process you put okay. As I said you fabs are very costly extremely costly in fact and unless the product is shelf product, what is off shelf product? (())(44:31.8) microprocessors they are general purpose anyone can pick up from the shelf but if I am making a specific game I cannot million games, or may be millions at best. But I can't make trillions. Then who will buy them, because someone else is making some other game, like Sony may have its own play box station and others may also have a box, Microsoft will another its own. So now these people will not let them know, okay what is the processor? So they may have their own processor designs processor technology. Sony has its own process lags only for gaming purpose. (())(45:11.2) has its own labs. But many Mitsubishi has closed because they actually tied up with now Toshiba.

So many companies which had good fab houses have actually folded because they have no business now to support. So many companies micron has come, global foundries have come but these are the new companies and when they will fold God knows okay. Okay so this is typically what IC processing we're looking into okay. Is that point clear? So something here, this is all introduction to why mask are very crucial and mask printing is very relevant in all IC processing. IF that doesn’t happen well every other process is useless, that's where the failures are actually okay. So how good you transfer pattern is that (())(45:59.3) all the IC manufacturer okay. So if you go to a lithography place in an any fab it is the cleanest environment you have to have for example typical clean room may have a class 10 or class 1 clean room. But the lithography room should be sub class 1 okay. Now that is because any particles we have just now shown the figures.

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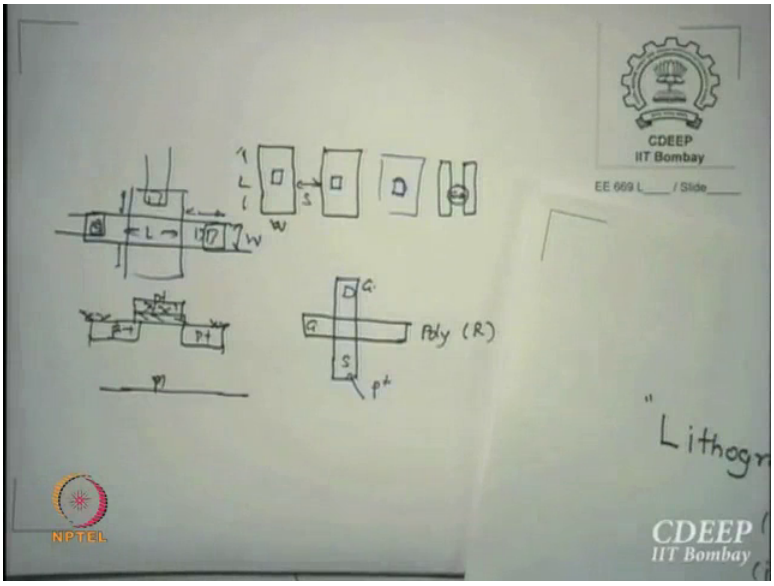

If any particle sits okay here which is larger than the gap you're putting this may not allow to resolve that okay. So now (())(46:40.1) shot depends on the wave mask is open or short the surface. Now this is very peculiar of lithography, so when I do mask processing and mask printing that area is the cleanest area in the whole fab house. And at a given time very few people are therefore actually allowed in… because as I see things if I move in a lab one million particles I move okay one hand one million okay. So I am worried about how much people I should allowed in a lithography system. So that is a cleanest environment and now when you're locking of wave length light exposures. So the light there cannot be white light because it has all (()) (47:22.6) all wavelengths available so it will expose the resist even before you do. So it normally have a yellow light and some have green lights now.

So some particular wavelengths are used which have nothing to do with resist wave lights okay and this is the color of that which normally doesn't not expose anyway white light is the worst because it will expose. White means it has all ultra-violet to deep infrared or large infrared so everything can be, anything kind of thing can be exposed out. So the clean room is very crucial and lithography is much more crucial for the success okay. Okay so if you have understood what I was trying hit on. Okay so integrated circuits could only be realized due to the most important process called lithography and as I say it can be either any kind of lithography, litho is transferring image or as it is.

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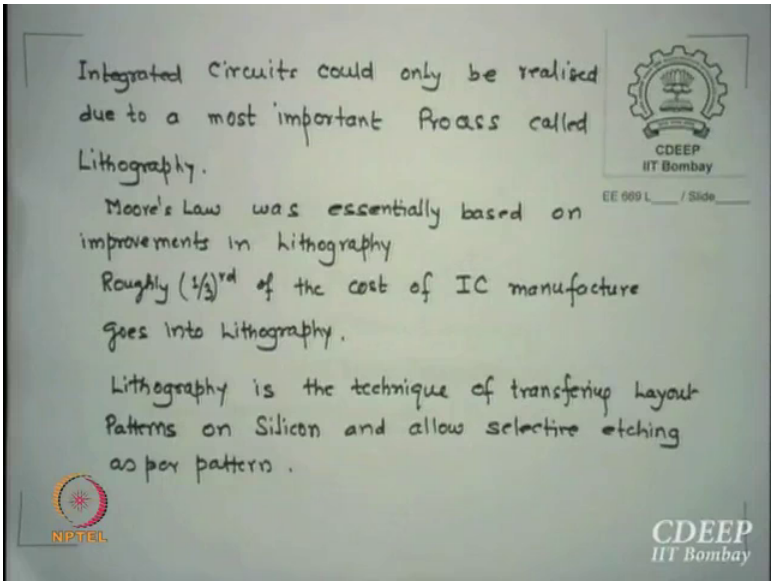

Moore's law was essentially based on improvements on lithography. Improvements roughly on this is something which you have to understand. The one third of the cost of IC manufacture actually goes in lithography. It's got 30 mask, 24 mask actually a cost is making a mask and successfully putting on a wafer is the major cost. So one third of the of a chip or one-third of cost in manufacture actually is attributed to lithography okay. These are the number which I don't know whether Plummer has given but these are the actual numbers from the lab since I worked in labs, I can tell you what kind of numbers they say. Lithography is the technique of transferring layout patterns on silicon or silicon dioxide or any other surface and allow selective etching as per the pattern. This is what lithography is all about. Is it okay? I have spoke so much general today and did nothing, so let's start doing something now is that okay.

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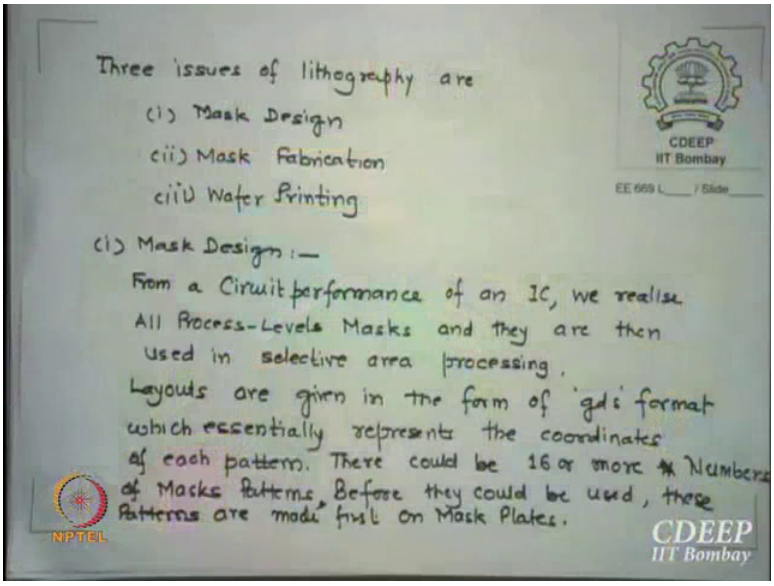

So there are three issues of lithography one of course is the is a mask design. So first is mask has to be available to do something. So I must design the mask. Now design come from designer or I may from here. But I need a design which has to be created. Then second is the mask fabrication to transfer it to process lab I need a mask I have to create mask. There are companies which only make mask they don't actually know further process. So you the payment they will generate mask for you okay and then they will send it to whichever company you wish okay like HCL, HCL does wafer from outside mask from outside, chips from outside and sell on HCLs name. And the last part is a wafer printing, at the end of the day I must transfer that pattern on the masked wafer, so there are 3 issues. I already talked about mask design from a circuit performance of an IC we realized all process level mask and they are then used to select area processing.

Layouts are generally given in GDS format which essentially represent the coordinates of each pattern, there could be 60 and more number of mask patterns before they could be use these patterns are made first on mask plates. These are called masked plates. This is of course the designer issue, this is how designer end up their job okay. So my job start from the mask plate, how to create mask okay. So this is VLSI design group this is sometimes separate group which makes mask and same company can do. And finally the process of CMOS or any other MOS. Or

any other semiconductor technology which may or may not come in next 30 years but can be worked.

I might have told you earlier also gallium arsenide was a material came with a bang in 1960s okay. And there was an effect called gun effect which everyone thought may fetch an over price and it just what I should say pitted down in next 4-5-8 year. No one remembers gun now. In my PhD unfortunately there was on gunn diode. Why I thought so because everyone was telling this is the material of future, gallium arsenide so I said let's do something, everyone was talking silicon I said you're welcome. Within 6-7 years I realized that Gallium arsenide will remain material of future because whenever it will come it will become present and it will go to future. So it never came except some for my student and others keep telling ho gaya sir ab agaya, 2050.

Okay the reason is obvious it will take enough time for them to mature a technology which silicon has matured in 70 years. So obviously it is not easy for them to mature a technology up with cost. So I am telling they will never reach but by the time, I don't know integrated circuit will survive. Then only by virtual thinking, do this may happen. From a CAD tool use we create a layout and then use Back Extraction to get circuit schematics. Circuit simulations prior and after layout simulations are performed and they should be matched. Further the layouts are to be checked for design that's why I brought the sheet because whatever what all design rules I say it has the technology constraints which a designer has to follow during layouts and they must be followed because these are constraints otherwise at no time designer this can be transferred. These are called design rule checkers.

Some new layout generators layout simulators, have built in DRC what does that mean? So if I want to draw a line next to it where it is highlighting the design rule then it will not allow you to use, it will start shouting. So it's built-in thing, but this is not true in spite of all DRC cleared the wafer may still have design rule violation okay that's the fun part okay. All companies will have who have this issue DRC run and chip did not, so there are a designer (())(54:14.1) okay. So I will show you, I am not teaching you design course otherwise I will show how this design violations come in spite of DRC checks. So mask making system uses a microscope like a systems which transfers images on photo-emulsion plates, sometimes this photo emulsion plates

could be metal plates also we will see them. These are called hard mask and one single pattern of the circuit needs to be replicated to a large number of chips on the wafer, thus we need a system which is called Step and Repeat.

We expose here for the next chip this for the next chip this, so this is called Step and Repeat. So mask itself is created by a process called Step down from 5X to X and keep repeating on number of chips you want to make as many mask patterns you must create okay. So this system which makes mask is a already I have shown you one of them but may be another figure I may show you hand drawn by me. Is it okay? So mask are actually created through a step and repeat system called Camera, it is also called a step and repeat camera. We are actually using a camera, slightly better version a microscope sometimes. So many of the lens system which we use there are convex or concave together, parallel plate convex lens. There are many lenses properties which people have tried to get what avoiding the average (())(55:59.9) okay. So there are many methods optics allow.

Those who are in optics you know when you try to solve one some other astigmatism may increase so you reduce that the defraction pattern will airy pattern will increase. So something happens so minimum of all. Yes?

Student: (())(56:21.4)

Yes you're right but that another mask is normally created from the CAD system itself on the pattern which is in the, which modulates the beam, is that clear.

Student: (())(56:38.8)

No you didn’t get it I had an image on the screen which it's coordinates I know so I can modulate the source of the light with these areas, what I am trying to say is the following, this is very you're great but of course you can create a mask by electron beam first and then use that ahead, but the way it is.

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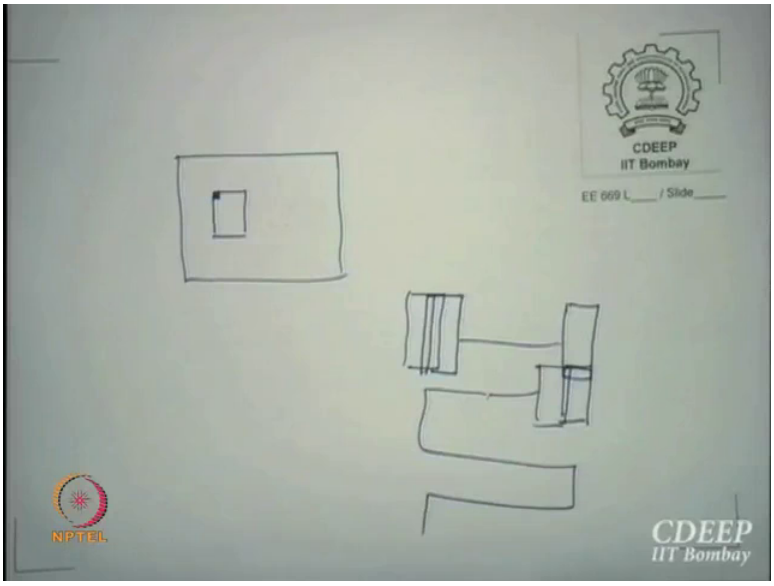

For example I want to create mask on this, let's say this area I want to fill okay so I have image somewhere in the computer so when I expose the light, it starts doing something like this, it exposes this much is that clear? On the emulsion plate itself okay. The way I do it is something very interesting. If this is one image exposure okay a 50 percent I do the next is shifted by 50 so it overlaps the last image, thought I don't want any gap light should be everywhere, when I reach the last for example this, this is the next scan is 7 90 percent down and you start exposing again. What is this scan called? Raster so the raster scan that image is transferred on the emulsion plates okay. You're right is that okay?

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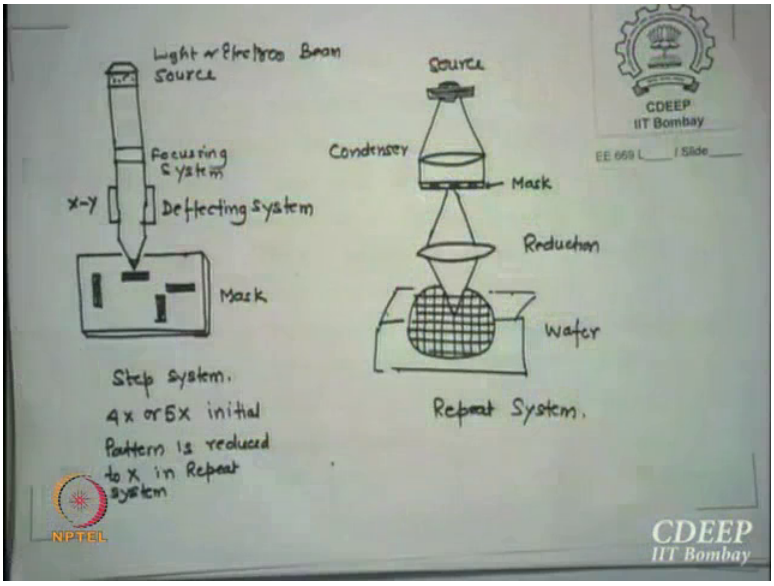

This is what exactly it does, it receives the data from the CAD this and actually modulates this light source or electron beam depending on what kind of mask you want to create okay. And through a focusing system can actually expose the whatever emulsion below, all emulsion this is a quartz plate which is has a emulsion coated okay. These emulsions we will see what are those emulsion but peculiar typically emulsion must receive light and sharp darkens itself, so when I develop those portions will be retained others etched okay. Now if you're using electron beam the deflecting system is electro-magnetic your plates, electrostatic plates and magnetic plates. So I can actually move the electron beam anywhere X and Y and therefore can expose exactly where I want.

So electron beam lithography is great because it exposes exactly where you want to exact dimensions you want, because it has small wavelengths. However electron beam system is very costly and individual chip if you have to do it, expose it for a wafer it will take months, so it's very costly. So what we do is we create a mask out of electron beams and use that as an optical mask for further work. Direct writing is also possible on the wafer itself I can like pen I can write patterns but electron beam. Some 100 chips are there 400 chips are there for each pattern I may actually program it, it will do everything like this for all chips. It may take 8 days to do these think of work, so it's very costly, whereas what we will do is we will create a mask plate using

electron beam possible for a better feature and then use those mask plates for optical lithography, this is what we will be doing.

So through this system a camera system which is shown here there can be light or electron beam source, there will be some focusing system, if it's a electron beam it's electro-focusing system, electron lenses can be created and we can create focusing we can have deflecting systems and you can expose lights on the emulsions I wrote already the step system has 4X and 5X initial pattern is reduced to X in the repeat. Step may as it is we create 5X in each. Whatever actual pattern size we actually expose 5 times, why we want to do this because accuracy in 5X is more likely to get further optics okay, but when I reduce I have another problem of reduce so air probably may multiple or may cancel depending on my expertise okay.

Okay so typical system which we may do repeat system is you may add source and you have created a mask which is set here, there is a condenser lens, light for example shines through this, these are electro-static lens whatever it is wherever these dark portions are there light doesn't pass, wherever clear portion light passes through. Light passes through, air does not pass. Then you actually there is a reduction lens system which reduces to X dimensions and expose on the wafer okay. Now this repeat system then I can do a step, step can be done by XY or it can be done by beam itself beam can be moved on from one position to the other okay. So either it is beam shifts or it is actual XY whatever control okay. Give a stepper motor, so much steps it will move so there are number of ways initially we used to have mechanical systems so steppers, nowadays it's all electron beams so it automatically scans okay.

So a typical first problem is to create a reticle so we can create reticle so these reticles are first important things and then they reduce X times of 1 upon 5 times 1 upon 4 times to X in each okay.

Student: (())(62:55.2)

People have tried but there are more errors than higher okay, it can do people have tried this is called, this is what multiple imaging was trying what you're saying. We're exactly trying on that

okay, multiple exposures okay. If you have done implant in your lab right now in your lab you must have seen the number of implants can create any profiles. So same techniques was tried but this is not Gaussian and since the patterns are not Gaussian the overlaps are very difficult, that's the problem. Gaussian everything is fine, where ions are known. I know how much peak values area so I can adjust my energies nothing happens here.

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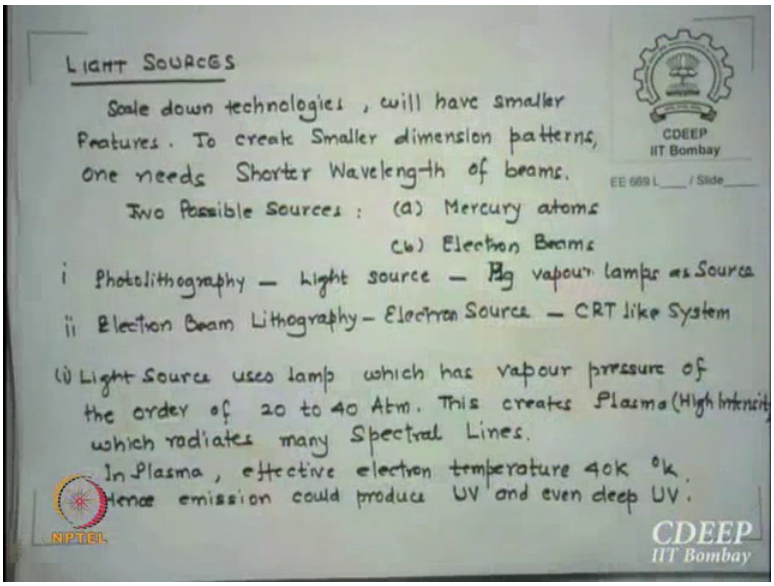

Okay you can look into the variety of books, this is given very well in the Plummer's book so there is a…I hope if at least some of you have Xerox copies of Plummer or Plummer's book itself or some still believe this is good enough and (())(64:02.5) at the end ke are yaar wo sab nahi tha usme. The first thing in a system which we require to do anything is called light source. What kind of light source I need as we scale down the technologies we're actually going to 7 nanometers now. So you will have small features and one need shorter wavelength beams is obvious 2 possible sources of light is used in exposures in lithography one is called Mercury atom beams and the other is electron beams. As I say X ray beams ion beams are still away and hopefully will remain away.

For photolithography, light source is normally so much common you know this whole good mercury sources all halogens all these tubes have essentially have mercury wafers and they act like a source of light which has a wavelength from ultraviolet to not far but little ahead of infra-

red. If you know the water purifier (())(65:21.1) actually shining UVs it's a simple UV lamp. The use of this photo lamps are slightly different kind of this along with mercury some catalyst added into the efficiency. The electron beam lithography is normally like an electron source like a CRT tube cathode ray you actually heat it. An electron copious emission of electron can be generated and then beams can be form by electrostatic lenses electron lenses as well as deflecting systems. So it's equivalently done there as well.

Now there is a problem which is (())(66:02.9), the light sources use lamps which are which are the vapor pressure of the order of 20-40 atmospheric pressures. This since the pressure is very high it creates plasma inside, plasma means state of ions, electrons, neutrals together is called plasma and why we need plasma is because I need high intensity beams of light so I must create plasmas. Now which and this plasma radiates the spectral lights which we are interested in. Just to give an idea 40000 degree kelvin is the plasma to electron temperature. The temperature of the actual gas may be room temperature but the electron temperature is as high as 40000 kelvins okay, that's why it's called (())(67:02.2) system. The energy is so high that increases the KT but it does not increase the environment or ambient temperature. So it's cold that's why cathode emits and so this is mercury vapors using a plasma mode to strike the gas and once you strike the gas you create mercury vapors plasmas and these plasma I repeat has electrons, photons and neutrals.

And you're applying it and problem for those who have done BE and have also not forgotten basic electrical engineering. Power (())(67:44.0) ye jo tube hai apki mercury tube mercury vapor lamp ism ek choke hai aur ek capacitor hai. Strike hota hai uske baad wo wahi rehta hai to fir kya hota hai, kaise wo, kyunki sustaining voltage is 110 strike voltage is much higher and therefore you need a choke and capacitor. So what happens after strike happens, uska to impedance ekdum low ho jayega. To wo kya karta hai? Socho zara ye ek serious issue hai, aaj tak ke tees saal ke itne interview me ye pucha hai mene aur 99 percent people don't know how actually a mercury vapor tube works, think of it and that's what I would like you to know okay.

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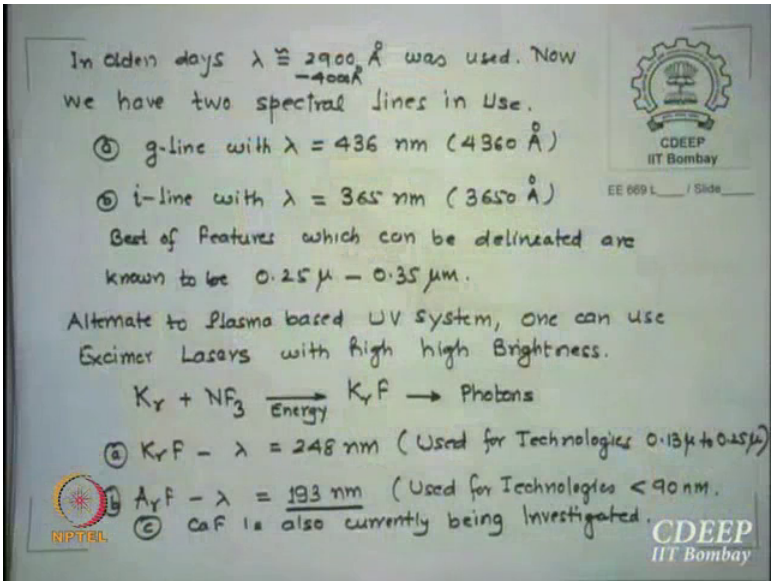

Last few minutes, in older days whether a mercury vapor lamp we used to use has a 2900 to 4000 UVs available okay, we used to use those lamps nowadays we're too separate lines, UV sources which are two specific spectral lines. One is called G line which has a wavelength of 436 nanometer or 4360 angstroms. The other is I lines which has lambda 365 nanometers which is 3650 angstroms. Please remember these are start spectral lines which are used lithography okay. Both these G-lines and I lines sources where useful till we were working on 0.25 micron nodes. 0.25 even 0.1 people have successfully done but below 0.18 or 0.25 these lines are not good enough because the dimensions are now smaller than the wavelengths you're actually using in order.

Okay so we will see what else, alternate to plasma based UV system one can use lasers okay. Excimer lasers with a very high brightness, double high hogaya but ek hi hai. Typically in a excimer laser your either required (())(70:04.4) or some other gas argon or nowadays even calcium chloride is used. So krypton plus NF3 and when you shine when you apply energy it form KrF and Krypton Chloride actually releases photons when ionized okay. Now krypton fluoride use a wavelength 248 nanometers okay so it is good for 0.13 to 0.25 microns. As I said some people try 90 nm successfully. Then we went to Argon fluorides which has a lambda of 193 nanometers and we are also now looking for fluorides alone argon fluoride is 193 if I use only flowing then it is 157 nanometers.

I didn’t write it but you can write okay may I have a figure I will show you. So we started with g lines 436 I line 365 then krypton 248 argon 193 which is the most standard line used in all wafer fabrication across the all industries 193 nanometers. This is some kind of a (())(71:28.8) number right now 193. Our effort is to go below that is why I said extreme UV we want to go to 10 nanometers at the day so that the dimensions would be as accurate as for 7 nanometers.

Student: (())(71:49.6)

Problem with E beam is say something like this you may create a mass but finally you will go on the optics. So the problem how optics will remain? Mass may be accurate, if you create and optical mask and use it optically further it's much more (())(72:08.8) so no more than 0.25 we actually use optical mask. Below 0.25 you just need electron beam mask created mask okay and then use optical. Since we have not done that those parts I am not telling you okay. So please remember very currently, ye jo material science wale log hai na, ye fluorine aur calcium fluoride dekho kya ho sakta hai.

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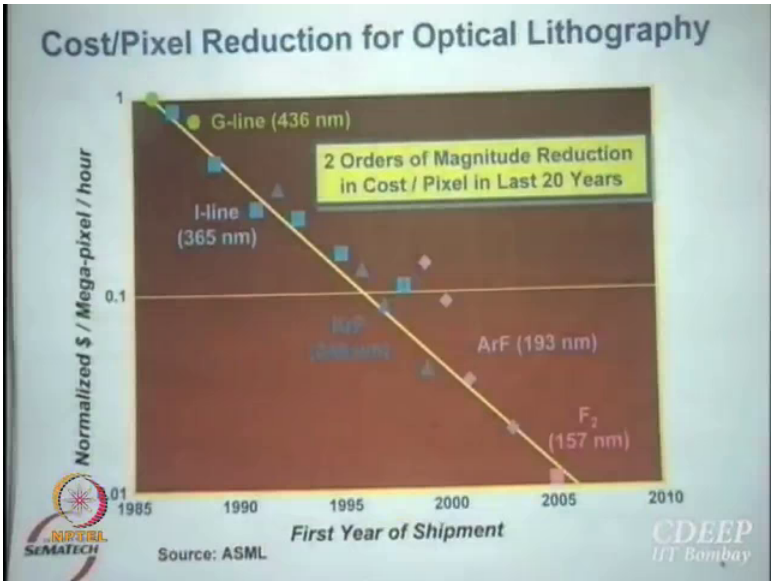

Here is for an optical lithography this is the what we call normalize dollar per megapixel per hour for your whatever up to 2010 they have shown. So that's what exactly it is, g lines 436, I line 365, krypton 248, argon 193, fluoride 157 and calcium fluoride one is believing may go to 112 okay so I am not sure, just numbers I read other read from some semi-conductor engineering book uhh journal but one doesn't know I am not sure of that number okay. So over the years can you now see this is the Moore law kind of you're trying to reduce and you're trying to match light with wavelength of that. But you can't do 193 nanometer even this 157 is not guarantee. So you have light of 1930 angstroms or 190 nanometer and your dimensions are what now? Few nanometers, you're talking of 7 nanometers 10 nanometers, the light wavelength is 193 nanometers how do I still get resolutions of my choice?

That's trick and that's most important optics okay. Optics have advantages and disadvantages okay, so next time we will first we will look into different photo resist and once we look into photo resist may be electron beam resist and thoda chemistry dikhayege apko ke polymer change resins hote kya hai and everything as I said this is given not exactly as I showed in the Plummer's book. Plummer has many papers in diffusion and in lithography, so his work in lithography is well known. Stanford has one best lithography system in 80s and it has the worst system 2014 they haven't got money so that's it. Okay so we stop here today.