Fabrication of Silicon VLSI Circuits Using MOS Technology
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Module 01
Lecture 15
Thermal Oxidation of Silicons (Continued)

So here we go so far what we are talking about mass capacitors this will also will be taught or maybe being taught right now by professor Vasi.

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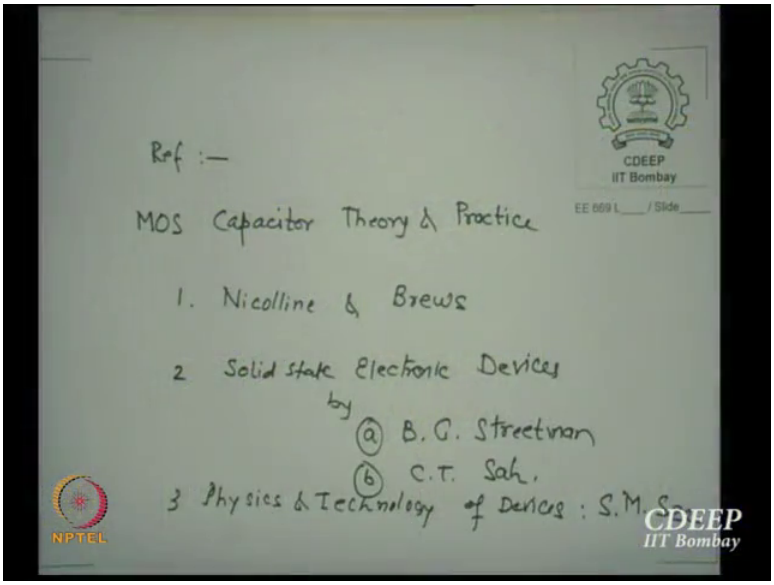

The books he may have been following or may not be I am not sure but these are some distinct where you can read mass capacitor theory practice measurement technology everything and the best of course for the mass physics and maybe measurement as well is by Nicolline and Brews they are the first few people who first time made a mass capacitor in Bell labs 1960 so they are the pioneers of mass capacitor business Brews is the president of gatech that is Georgia tech university Nicolline is no more.

Solid state electronic devices by B.G. Streetman this is the second year this a book which is teach most of us teach for the second year course on solid state devices electronic devices if you are really working on mass capacitor related or professor Vasi or someone is who is doing only

mass he best book probably C.T. Sah it is very difficult to read and understand, it has some 8 kinds of fonts underlines and everything so first one you have bold letters then you read the next one then you refer back somewhere so it is a great book C.T. Sah is very famous person as I said last time he missed his noble prize Gudzberg and Sah, okay.

You know long time if you leave Bell lab you miss the noble prize then he realize that time, okay. Let us talk about what we were talking so this is just for those someone asked me after the class so I thought maybe I will inform and I of course my notes are nothing to do with any of these books or maybe all of these books either of it, okay.

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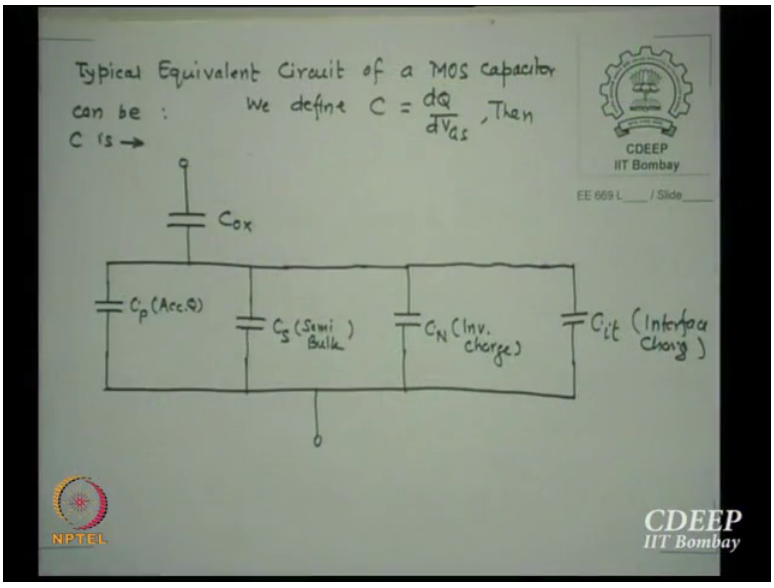

We were discussing last time something about the equivalent circuit of a so why I am spending so much time on mass capacitor because that is by bread and butter for microelectronics if you are working in microelectronics area with any of the faculty and most of the faculties now working in the technology or device area (())(2:40) few in circuits they will be keep hampering on this, okay so I thought maybe it is better if I give one more perspective of mass capacitor much details can be obtained by books or as well as discussion with your prospective or otherwise guides all your senior who probably still do not know.

We were talking about when the Vgs becomes minus value the in a for p semiconductor substrate the mass capacitor is called n channel device or electrons are going to come in inversion if you have a p substrate, sorry holes are coming to the surface and therefore we say is accumulation

mode and in accumulation mode larger the charges near the surface more will be capacitance associated, okay. So essentially what happens that in accumulation none of these capacitors come into picture because none of them is related to minus Vgs only Cp is related to minus Vgs.

However, the as the capacitance starts increasing because charges are very high in the accumulation so one can see Dq by Dv if the charge is very high with a small change in voltage obviously the Cp will be larger and if Cp is larger 1 upon omega C will be smaller. So in fact in accumulation I said earlier day that it is only oxide capacitance which dominates is also visible from this however in a weak accumulation Cp term may appear which maybe comparable to C ox value, okay but normally accumulation goes plus Vgs to minus Vgs Vdd and at those places the accumulation charge is so high that Dqp by Dvg is very very high and one can say Cp acts like a short circuit actually and the other capacitance anyway do not exist and therefore in accumulation we say the oxide capacitance is all that we measure or monitor but I repeatedly tell you very close to 0 value with minus Cp term will come into picture and then you will have a series combination of C ox and Cp, no one really interested in that area very much and therefore no one measures to much on this but in case someone wants to do yeah that measurement is also possible with minus small Vgs you can do some measurements at least hmlf measurement and figure out what is the Cp value but since Cp value keeps changing it is not very crucial for us near the 0 value where it starts depletion later so we do not measure this anytime but it is not said that it is not there it exists, okay so I always say what is possible and what is reality, okay reality no one does anything that is more reality, okay no one does anything but here is something you will have to do.

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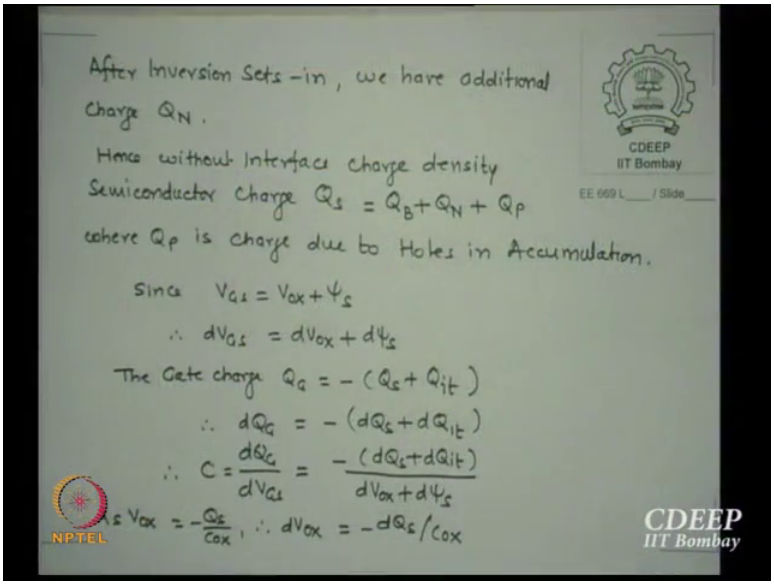

Once the inversion sets in maybe this figure I kept I will keep separate so that I keep coming on the figure once the inversion sets in you already have depletion charge which I described as bulk charge then there is a Qp which is essentially 0 because there are no hole charges in the when you go plus Vgs, however we will generalize the terms and whichever term is invalid we will leave that term, okay right now I keep all charges accumulation all other will go away only Qp will appear in case of (())(6:15) so I will keep writing all charges and whichever are not valid I will just leave them out, okay.

So in case of inversion so, okay so I (())(6:26) so now let us say if I say that gate charge or which is Qs plus Qit in case there are interface state in the silicon silicon dioxide interface then the gate charge or the total charge in the metal is equal to Qs plus Qit where Qs is of course is Qb plus Qn plus Qp but as I say Qp will not be there when Qn is there when Qn is there Qp will not be there so either way but we write all of it. So if I differentiate this Qg then delta Qg is minus delta Qs plus delta Qit differential simple then capacitance is defined as change in charge at the gate as function of gate voltage so delta Qg by delta Vgs is the net capacitance from gate to ground and that is what we are trying to monitor, okay.

So please look at it just before you I am measuring this capacitance total from gate to the ground, okay since I am measuring it I also write down so I say delta Qg is essentially delta Qs plus Qit slightly this worrisome here also the way we should define is Qs dash where Qs dash is now,

sorry Qs dash is Qs plus Qit. The oxide voltage is essentially decided by the semiconductor charge which is Qit plus Qs divided by C ox that is by, which law? D's Gauss's law D is epsilon e and this we substitute or D is minus D epsilon Qs is essentially Es is proportional to Q and therefore this is the Gauss's law.

So if I differentiate this Dv ox is minus D Qs dash by C ox just differential of this and then I collect the terms I divide this whole of D Qs by Dit or Qs dash in the denominator, have you noted down this please note down do not take snaps because snaps do not record of course they are mobiles which records as well these days but please do not do it because writing is the only solution for understanding whatever technology people may say I am in charge of what we call national program of technology enhance learning where we are giving video talks and this is one of them, okay.

The idea is that people who have no teachers of this area or not so called experts in that area at least the other university teachers students can see what is going on, okay. So these lectures are not necessarily for IIT but you can also use I am not denying and these lectures are essentially meant for people who have probably have no access (())(9:27) of a teacher and therefore we create video lectures, web lectures but these are something cannot be replaced by the kind of things which we talk here, is that clear to you?

So writing down is the simplest way of understanding thing over 100's of year this has been proved irrespective what technology people say because if I am talking as a NPTEL coordinator I will keep saying forget it I say just look 10 times you can listen everything you can understand all statements are fine, okay when I am in the other cab something I will say but in reality as a teacher I would say the best possible understanding is when you look at me, I look at you, you write down you probably should ask questions I hope you will someday, okay and then this interaction probably may help you to understand better this is what essentially the teaching one to one is, okay.

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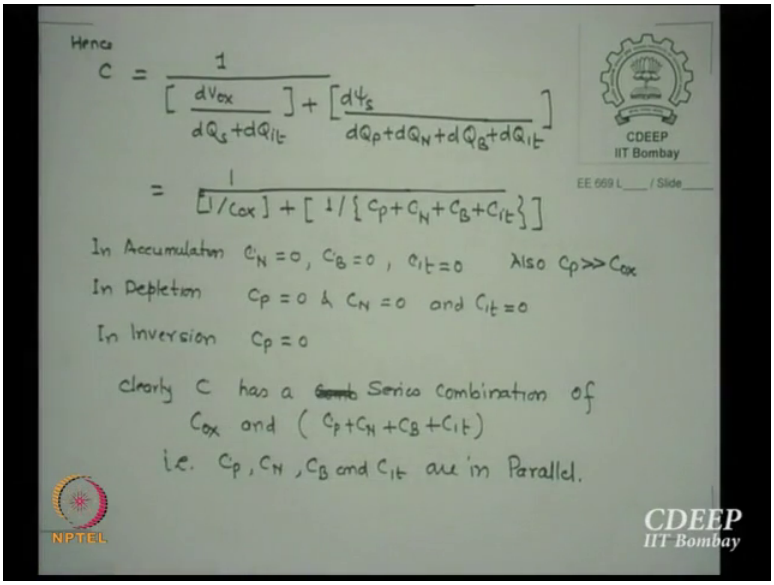

So if I divide D Qs by Dit both Dv ox and the (())(10:27) terms I will get D Qs plus Dit is all this full charge I did not write Qs here all of it in this I wrote but I know D Vox by D Qx plus Dit is 1 upon C ox just now I derived it, just a minute D Qs dash by C ox is V ox Dv ox so Dv ox by this is essentially 1 upon C ox so this term is 1 upon C ox this term Dq by voltage is a capacitance so these are this is accumulation capacitance this is inversion capacitance, this is depletion capacitance and this is interface state capacitance so all four capacitances are now coming into, so what is the suggestion you are giving that the Cp plus Cn plus Cb plus Cit means what? All four capacitor should be in what mode? Parallel because they are adding, okay.

However this 1 upon C ox is in series with all of them, is that clear? 1 upon C ox plus 1 upon this means C ox is in series with sum of all these which are all in parallel, so if you just a minute I will come back to that you can see from here C ox is series with all four parallel capacitances is what we said equivalent circuit and we also have derived from our theory that yes indeed this circuit equivalent is fair enough, when we want to do this because in real life I will only measure anything on the circuit all that I can do measurement in a lab is on a circuit, so I must know what I am measuring and what it means, okay.

So to prove this I should you that this equivalent circuit is same as what one can even derive from basic principle and what is basic principle in electrostatics that Gauss's law and nothing more, okay. So in accumulation we will say there is no depletion there is no inversion and there

is no interface state of course there are few interface state but they are called accepter and they are very few in numbers and difficult to charge them for a p semiconductors.

So one says that all other terms are 0, okay so this terms actually 1 upon infinite 0 means infinite means that does not react into picture they are all short circuited so if you see this circuit all of them are short circuited except this so when gets value of this therefore one can say C is C ox so in accumulation we always monitor C ox, okay. In case of depletion one now finds it that there are no hole charges because there is no accumulation inversion has not set in so there is no Cn and assume right now during depletion there is a very little Qit then it can happen you can add that term if you wish. So for a edge of depletion where inversion starts per say one can see this even assumption of Cit 0 is not very bad but it is not correct, okay somewhere it actually changes, okay.

Whereas in inversion we say Cp is 0 but all other terms are available to you, okay so what is that we are going to do now?

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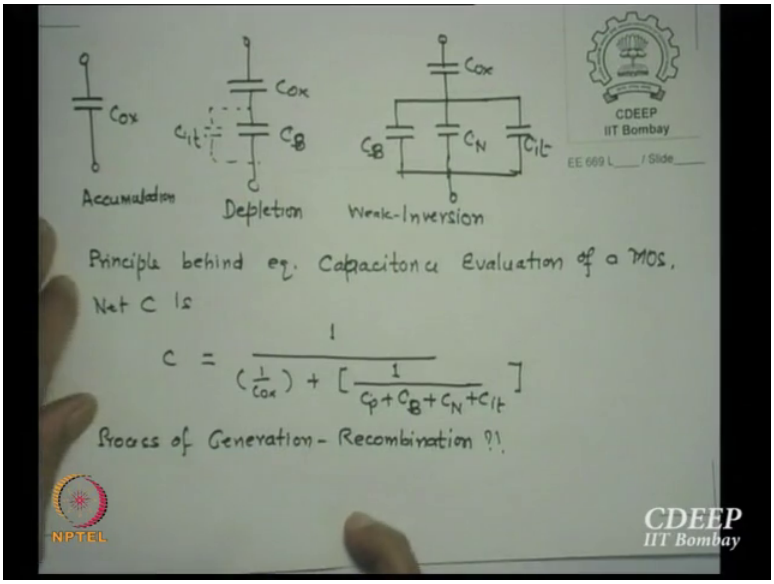

We are going to find out from a given equivalent circuit which we have I will say I have a equivalent circuit which shows something like this C ox in accumulation depletion Cs plus C ox in series with Cv parallel Cit if you wish, okay I mean some Cit will appear so you may solve which Cit but this terms are much smaller much higher and therefore open circuited, whereas in this case when the weak inversion starts all of them are present, okay in weak inversion the

depletion charge is depletion capacitance is there the inversion charge capacitance is there and also interface states are responding so Cit is also present there.

So this is an equivalent circuit where it is weak inversion starts? Prior to inversion where the Cv I will show you Cv there is a change in capacitance stronger than that near depletion at the edge of other side but as it comes down interface state reacts, okay and you see a stretch out the capacitance curve moves away from the ideal value, okay. So this however how do we know about this? We realize some theory and we figured it out that this is possible to monitor in some measurement techniques in which I can basically I am interested in bulk charges so I will be able to find if I just be below inversion only in depletion region or close to inversion then I can only measure Cv so I know C ox and Cv together C ox I know so I will always find how much is Cv, Cv means I actually know the concentration of the substrate itself, okay so one method of measuring concentration is measurement of Cv itself, okay.

However, as I keep saying you when I am inversion there are two possibilities after you, one is you still increase the voltage there are two things can happen and that depends on the measurement frequencies, if we say Cit actually responds to does not respond to frequency that is AC signal which you are applied to measure the Cv if Cit does not respond then it is only Cv which will be (())(16:20) bulk charges in series with C ox.

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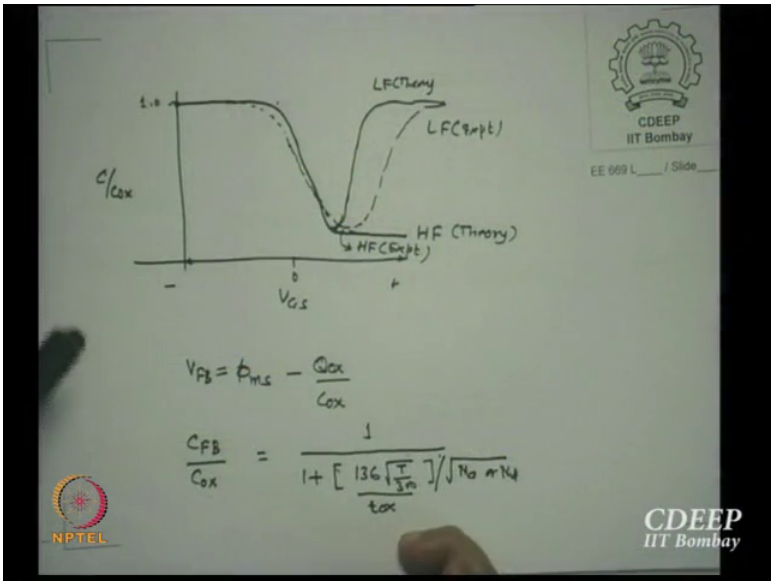

So maybe I will show the figure so that you may have better understanding I will come back to that sheet again but this is my high frequency Cv I plotted normalized value C by C ox so from here of course accumulation it is constant so we do not care so this is my depletion here is my inversion but if the Cit does not respond that is interface state do not follow the charge may change in the due to the bias polarity change then Cit's are neglected and you see a constant capacitance after inversion, okay that is the C minimum which is series combination oxide capacitance with bulk capacitance or due to the depletion, okay.

So this is essentially we knew that if Cit's are not responding that means we can forget about them and this can happen in the measurement system if the measurement frequencies are very high 100 megahertz 1 megahertz to 100 megahertz the interface states are unable to follow this change in voltage, is that clear to you? If they do not follow so at high frequency there is not much Cit effect of course slight stretch out as I said you will be seen near inversion because Cit there is not really infinite but it is some finite values so stretch out is seen even in high frequency but it is very small and can be neglected in most cases.

However the problem starts something we had noted down this of course we will back to the sheet I just wanted to so for high frequency one of the most standard high frequency measurement is something like telling you theory Cv equivalent of theory Cv with other parameters which we know. So it is some kind of equivalence whenever I measures high frequency I know it is a theoretical Cv as if equivalently I got, okay Cx series to the Cv, okay.

So this value is known to be the first measurement which is (())(18:26) high frequency measurement, okay. However if I have a frequency of measurement as very low 1 hertz to 10 hertz then everyone will follow the frequency variations bulk charges can follow, interface state can follow every charge can charge the charge with the because is a so low so they can actually change the charge as per the voltage you are applying, if that happens very low frequency signal we apply.

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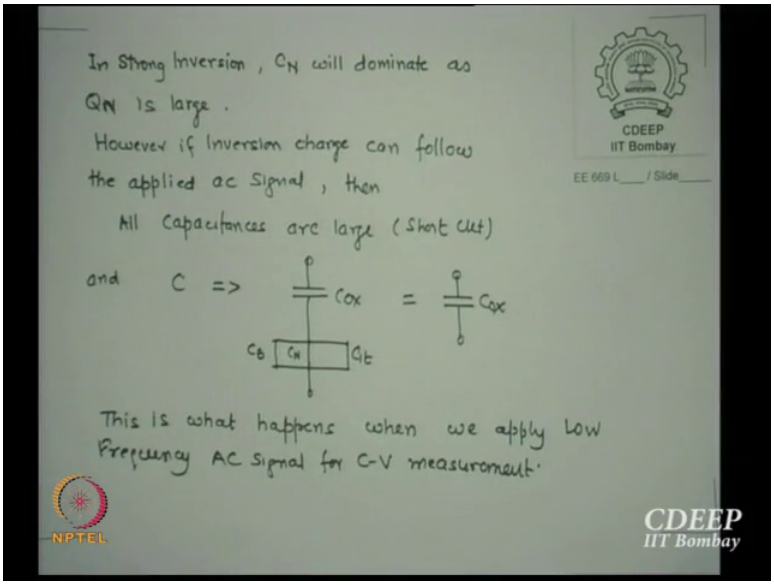

Here is a figure since the inversion charge is also following which is and Cn is the strongest charge term there largest strong inversion what is a charge density, maximum carriers are in inversion so if they can follow the capacitance associated with inversion layer is very high very very high, is that point clear? That means equivalently what is that 1 upon C is very low or shorting or something.

So as soon as you become higher than Vt value and you keep increasing your Vgs one figures out that all this capacitance are equivalently saying shorting itself because there values are larger equivalently short which means you actually measure C ox, okay in between this inversion and strong inversion Cit is responding and so is Cv everyone is responding so this, just a minute you can see from here this at low frequency of course there are two curve I have drawn one is due to without Cit and with theory and the other is with Cit measured, okay.

So till the voltage is large enough, what is this large enough voltage means? The inversion charge is strong enough there so that D Qn by D Vg is very high which means it will short circuit all other capacitance also, so that means only C ox will turn. So you can see as you increase this you finally go back to C ox value in between inversion and strong inversion the capacitance will keep rising towards C ox and as strong inversion is reached D Qn by D Vg is large enough to short everything else, okay and in that time what we will say C ox is reached.

So low frequency curve is essentially you can see inverted u or rather (())(20:56) and that is why we must have two cases one is high frequency Cv other is low frequency Cv and I know in low frequency somewhere here Cit is responding, is that correct? In high frequency except near the inversion there is nothing much is happening in Cit though it is happening but much smaller happening.

So if I monitor theory of this by theoretical low frequency curve if I know and if this is due to the interface states which have moved out because of the it is responding charge now so difference I will be able to find and that difference will be due to the interface states this is called quasi-static technique which is what is what I will write down this is called (())(21:45) quasi-static technique, what is quasi-static? Why it is not static, static means what? Time independent, no actually it is time slowly time varying and therefore it is called quasi-static thermal equilibrium can be attained, okay and therefore it is called quasi-static lot of physics interesting physics maybe professor Vasi should tell you more about it I should not keep telling and otherwise it will happen I will be teaching his course and he is certainly not teach my part so we will be missing something else, okay.

So having shown you the figures this left, you want to write down something? Okay this expression please if you need this figure you can write this is given in different books in a different form I try to simplify as much as possible so that at least it gets into your mind why low frequency Cv is going back, okay there are some more theories to be involved and more maths there is a second order equations will appear lot of game goes on, okay when you start continuity equation with Poison's equation one is very high, okay so having fun is very high we I just wanted to give you physics on what is happening the real value calculations are not trivial people like professor Vasi should explain you how why that has happened or how it can be evaluated so I am teaching a course I will also do it but right now I am not, okay.

So this figure which I brought, is that okay now? Please note down this is very important for people who are working on microelectronics labs they are every now and then they grow some insulator these day names are changing but at the end of the day you will measure some Cv, Iv, Tv whatever for Cv, Ct and there this capacitance is one of the measure experiment we do, okay and it does give us almost everything what I am really looking for from C ox I know T ox, okay. So I am actually measuring a Cv to characterize all of my oxide, okay and therefore it is one of

the strongest measurement technique which allows you to monitor your oxide and why we are so much worried about oxide last time I said you if there are variation in oxide properties then many things can happen one is Vt may vary the other it may vary mobility is it may vary also break down of the oxides, okay.

So lower at some Vgs it may break down so there are many possibilities in which mass circuit may not function, okay or at least not function to your spec, okay in this scenario we must understand if I am making a circuit or making a device I must know whether I will be able to achieve a circuit performance at the end of the day I am least bother whether Cit shorts or does not shorts but if my mobility goes down then I am coming back and say where is the possibility of mobility going down, okay why it has gone down, why ids, vds characteristics does not show good slope, okay then I am worried because that is decided by my circuit performance I want this speed and I am not getting it so I will look into it where is the problem.

So all this microelectronics theory is related to finally circuit performance I want to tell my other colleagues on the other side of the building that they also should tell something about the circuit because we are actually doing circuits and we are hampered by their process not being correct, okay and they keep saying, no no you are not doing well your models are not correct all statement but if I want technology I will say the same things, okay this is the game, okay.

Another thing which I did not say but maybe you can read in a book where do you monitor your capacitances this shift in this at what capacitance I should monitor the shift so there is a capacitance called flood band capacitor, what is flood band? Whatever voltage initially apply there may be a band bending, so opposite of that voltage we will bring the bands back into flat band. So any shift from that is called shift in flat band voltages so this flat band voltage is gain by phi ms minus Q oxide total charge by C ox and can be derived as of course which is not very accurate maybe I should, “ye engineering hai ye thodasa equivalence hai” 1 upon 136 T by 300 by T ox divided by Na or Nd depends on p substrate or n substrate.

So I can always evaluate for a given oxide thickness what is on given doping substrate what is the Cfdb and at that Cfb by C ox I should actually monitor all shifts, is that correct? Because flat band is the natural point from where every voltage everything was measured so flat band capacitance is also monitored and from there evaluated and from that Cfb by C ox I actually

monitor all variations how much from that flat band I am away from this, okay and that is the measure of any measurement I do I must therefore know this theory, theory means I must know without interface states how much and what is Cfb, so I know okay at this point, okay theoretically there are no dit sign here but now I am going here so this voltage shift is essentially Q by related to charge in the interface states and therefore we know how much are the interface states.

So this monitoring is very very crucial because we will able to know, and of course if this is too small is it good? Yeah smaller the Dit better for us we are very close to theory that means it will not change motilities very much, not change thresholds very much so that is what we are attempting and when we make any insulator on silicon or any other substrate, okay the interface is very dominant in the actual mass characteristics.

So please remember why so much papers millions of them are published in this so called oxide system is because of this that every time we do something or change something something else appears and then you have a paper, okay. So, where? Depletion is quibble, no no in flat band is essentially the before we apply this you want bands to be flat and this I will come to this phi ms and Q cox I already said this is only additive term so that will shift the Cv by Q by C ox value but this additional term phi ms will come to it so this is called flat band voltage.

So if you apply this voltage before you apply even with without Vgs applied this bending will start and I want to see how much bending equivalently already has achieved so that difference we call it flat band voltage, okay.

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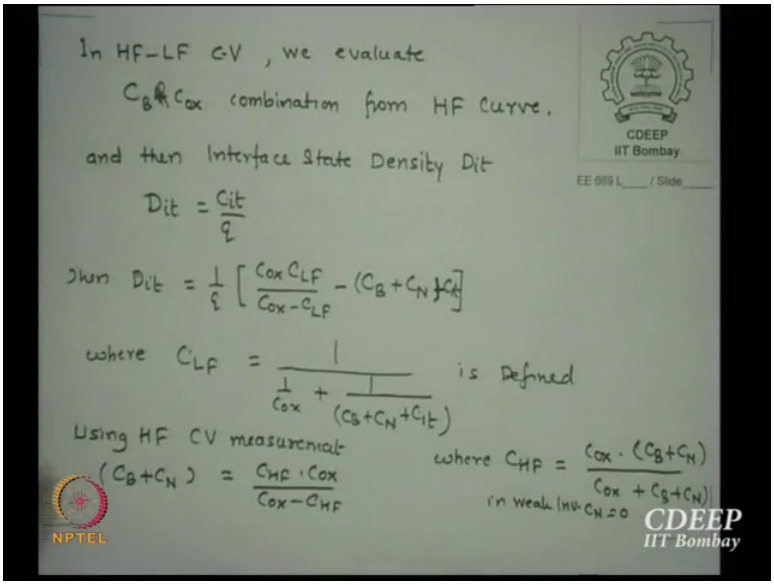

So if I monitor, how do I monitor real life? I measure what is called quasi-static measurement in which both high frequency and low frequency Cv's are monitored and we know Dit is Cit by q so one can say of course (())(29:07) I will not derive can but I do not this Dit is 1 upon q C ox Clf by C ox minus Clf minus Cb plus Cn plus Cit where the low frequency capacitance is given by this expression, okay you can always derive this I have derived and written it if you someone wants I will send that derivation but I think I have given you references so read somewhere.

So I can monitor Clf and I can this is theory because this is what I this at theory only (())(29:41) Cit I will say Cit is 0 in theory but in real life Cit will appear and I will see how much, okay. Using a high frequency Cv we know in high frequency what is the net capacitance oxide parallel to Cv plus Cn, okay because there is a inversion so Cb plus Cn so in weak inversion Cn is 0 but in our strong inversion Cn presents itself. So one can say Cv plus Cn from this expression is Chf into C ox minus C ox minus (())(30:15) this is small algebra this expression is rewritten to get this, is that clear? "Thoda maths karo isko idhar lao isko idhar aisa hojayga wo, okay kaise karte hai 1 upon Chf is 1 upon C ox plus 1 upon Cv plus Cn aisa karna this is essentially equal to 1 upon Chf is equal to 1 upon C ox plus 1 upon Cv Cn now you subtract other side and get this expression, okay".

So I got Cb plus Cn equal to this which is what and as I said Cit is the additional term which I will monitor so right now I am only looking for this Cv plus Cn so if I substitute, have you noted down? Please.

Student: Sir when no voltage is applied there must be some depletion with.

Professor: That is Cb (())(31:11) is actually Cv Qna x.

Student: Sir why we have not taken that (())(31:16).

Professor: Ye likha hai na Cb me, in a flat band voltage that theoretical we are measuring every from the theoretical curve without any bias initially, okay. So initial is Cf no I am interested in Cfb what I am C actually is the plot but at what point I should measure I should you I measure from at the Vfb where the capacitance is Cfb I am not calculating delta V from there I am only trying to tell you that where do I monitor delta's so I monitor everything at Cfb as if there are no effects of work functions as well as the fixed charge only semiconductor is present whatever charge I put on a metal is reflected in semiconductors, in case they are present I must first say are not there equivalently so how much voltage equivalently they are already getting present there is Vfb.

So at that time point whatever is the capacitance at that point any other change is monitor from that value, is that clear? Because then when I apply Vgs Qs will change I want the (())(32:20) so initially where we were, so from there what is the shift, okay is that okay?

Student: (())(32:33)

Professor: Ye series me capacitance hai to ap zara karo na 1 upon C is equal to 1 upon C, no wo plus nahi minus hoke aega na idhar, abhi maths thoda jaldi karsako toh zada accha hai baba is term ko udhar le ao, okay. Ab me bhi bina dekhe karraha hu toh apko toh maths karke toh ana hi chahiye, anyway. So I monitored I can now say Chf is very close to theory because we already said it hat Dit effect is very little there.

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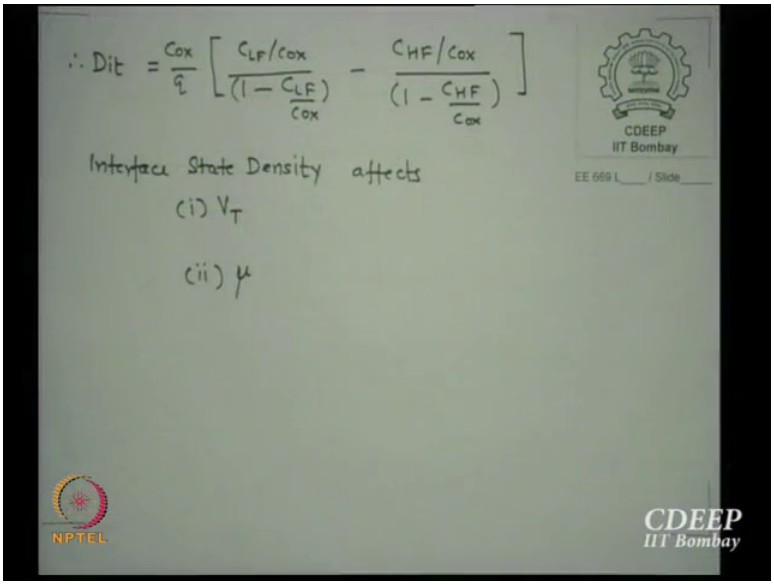

So what I actually figure out from Dit is this this expression is available in Nicollins book hopefully so. C ox by q into Clf by C ox 1 minus Clf by C ox this is essentially C ox minus Cls C ox cancels so I actually divided C ox, why I divided C ox everywhere? Everywhere I am measuring ratio so from C ox I just divide everything C ox there is Chf by C ox 1 minus Chf by C ox Chf you can monitor Clf you can monitor and therefore Dit can be monitored, is that clear? That is how interface states are actually monitored, okay and I repeat why we are so keen about Dit I keep saying you my worries are threshold voltage and mobilitys if they do not affect me at then (())(34:15) whether this state exist or do not exists whether Shockley was present or not present if Shockley states are there fair enough, okay we will take care somewhere else in theory but nothing to do the experiment but in real life they affect so much then we are worried about, okay.

Is that point clear? So why hf lf this is the simplest Cv there are I will list now some of them there are n techniques available which are more accurate sometimes they are quicker sometimes this like if you are in circuit area solid states circuit (())(34:52) very famous for us it does not publish a single paper on any simulation unless you have a actual chip measurement data.

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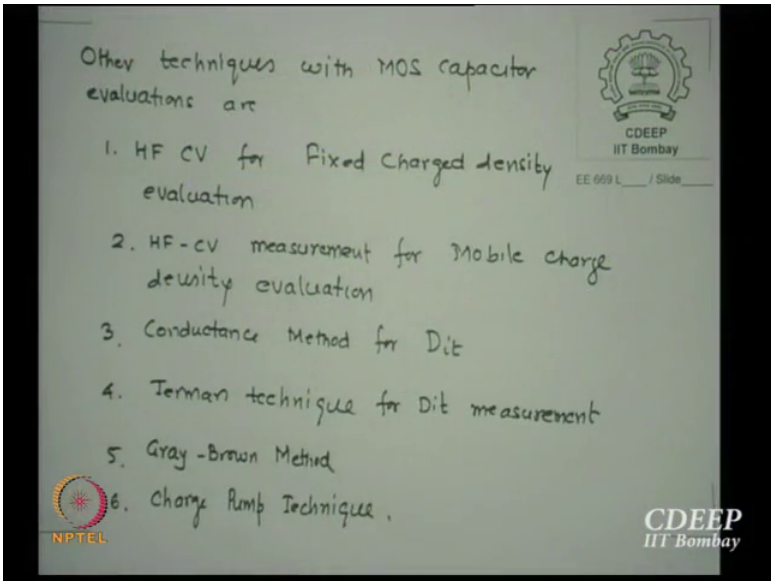

Hf Cv for fixed charge density evaluation clearly only hf measurement can be done and we will show why then hf Cv measurement for mobile charge there is an another measurement technique for dit which is very popular technique actually and this goes (())(35:17) technique it was very famous is called conductance technique any capacitance will also have along with it its conductance, is that clear? Sigma plus j omega as we say so there will be some resistive part and some capacitive part so actually instead of capacitance you can also monitor conductances and that is a very popular technique in many industries they mostly conductance technique to monitor this some who we have in (())(35:48) by Cv so in our life mostly Cv measurements where done but it is not true that conductance measurement conductance measurement little more thinking has to be done because it has to be matched the matching sometimes is not right and therefore it may give wrong results, okay but all (())(36:05) this is not that this statement is not valid really everyone must do collect.

Then there is another technique which is called Terman technique (())(36:14) for Dit measurement it is Dt time dependent measurement then there is a technique called Gray brown which is temperature measurement like you can cool the capacitor and you increase the temperature shift in this can also be used to measure the Cv's and there is a most popular among all the currents law people is called charge pump technique we just pump it and see how fast it discharges, okay and we from there the time constants we will be able find what is the

capacitance this, okay charge pump technique is related to capacitance transient technique Ct's, okay.

So these are as I say those who are actually working in the lab hopefully few of you, okay.

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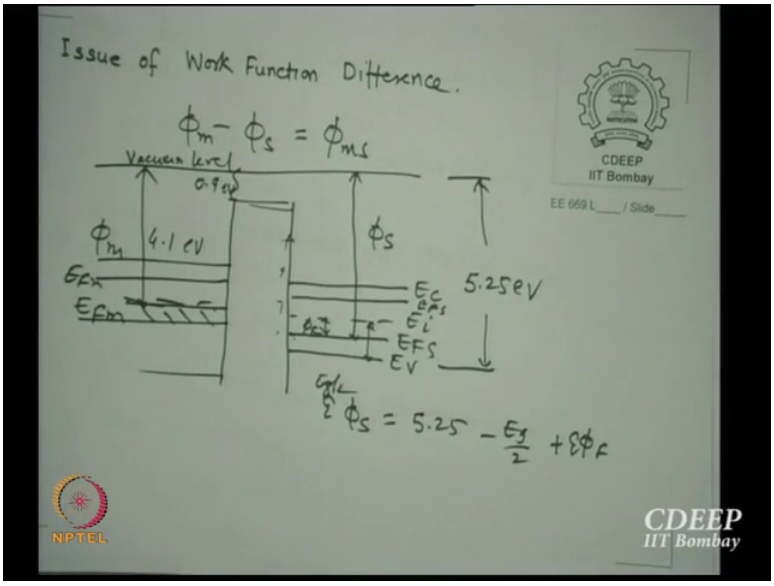

Someone was asking about phi ms and I said phi m minus phi s is equal, sorry is phi ms the difference of work function so this comes from a fact something like this, let us say I have two materials separated by right now insulator this is the Fermi level in the metal, what is Fermi level in metal defined? The field band up to which all electrons are available is called the Fermi level whereas in semiconductors maybe you have somewhere here and then there is a this is my Ev this is my of course these are not exactly same places where it should come I am just drawing randomly right now Ec then there is a level which is called vacuum level, what is vacuum level? The energy required for a metal to be heated to come out of the material in a vacuum is called that is why this energy is picked up from here and this is called metal work function semiconductor work function is measure let us say it is a p semi-conductor is measured from here to here so this is phi s.

However phi s is a function of phi f Fermi level how much is the doping will decide your away from that, okay. However one knows in semiconductor at least in silicon from the balance band to the vacuum level this energy is known 5.25 eV, okay if this is aluminum this will be 4.1 eV this vacuum level to the this is 0.9 eV so actually if you see both the aluminum work function is

given 3.2 electron volt but from the vacuum level it is 4.1 eV, okay. Now if I two materials and I join, what will happen? The carriers must go across for what reason that the Fermi levels get aligned there is not current to be flown in the system so as soon as I join this efs has to match this, okay.

Now if phi ms is lower than phi s then where the bending will start if phi m is equivalently where it will go please remember that this value between Fermi level to vacuum cannot change, okay that can cannot change, okay because that is the work function so where do you expect bending if phi m is 0.4 0.1 phi s is can you derive phi s from here tell me now for p channel, this is 4 5.25, okay this is Eg by 2, is that okay? So minus Eg by 2 plus phi f or maybe now (())(40:22) it is all energies, okay is that okay? 5.25 minus Eg by 2 will bring it Ei plus Ef phi s so it is the so the work function on semiconductor is derived from the band wherever is your Fermi level depend if it is n channel substrate device your Efs will be somewhere here so then how will it be 5.25 minus Eg by 2 minus phi s will become for n substrate, is that clear?

So any substrate doping given to you, you should be able to evaluate phi s the metal will be given to you gold or aluminum or any other titanium or whichever it is titanium has a band gap I mean this work function of 3.2 electron volts so it is very close to aluminum but it has its own properties good or bad both. So gold has 5 so it is very large of this that is why gold is very stable it requires very high temperature to actually evaporate gold aluminum can be at 1800 to 1850 gold 3300, okay so that is the reason why it takes energy to actually take the carrier out, okay.

So this minus this is what you have to evaluate and I will not now that I have thought you mass Cv think of it how bending will start, okay where I actually join them whether this will be like this or whether like this whether this will go up or whether this will go think of it equivalently what I am doing, okay. So initially itself there will be band bending in respective to whether you apply bias or you do not so that already bands are bend now I always measure everything from the flat band so I apply opposite voltage to compensate for that, that difference is the flat band voltage initially whatever has happened I compensate the opposite polarity voltage so it comes back and that voltage we call a vfb.

The similar argument I already said if there are positive charges here the semiconductor will already receive negative charge, what does that mean? The bending has already started down so to come by again you will have to apply some voltage and that voltage plus this phi ms is essentially called flat band voltage, is that correct? So given a mass capacitor with some doping you should and material of gate you should do, if it is silicon then what happens? That is a very important question, if I start the silicon will there be phi ms, will there be phi ms or will that be phi ms it will always be there the reason is something different which he said in correctly but not exactly slight difference there the normal n channel devices that shows lonar n plus, is that correct? And the substrate is p the gate (())(43:38) receives the same doping as source and drain so poly will be n plus but the substrate in Vp if it is a p channel device the source generally p type so is the polynomial will become p type and substrate is n type so it will be always be opposite to each other, is that clear? Of course there are some technologies and (())(44:02) but some other day, okay.

In most silicon gate technologies this will be (())(44:08) whatever is the gate doping it will be opposite to the substrate because source during doping will be same as what will go on the poly, okay. So if it n type p type and then it if it is a semiconductor let us say here this is exactly same now, okay even if Efs is same the Fermi level now is here in the case of metal in the case of n substrate. So there is a difference between Fermi level of n semiconductor to Fermi level in p semiconductors, okay and that difference is phi ms, so phi ms always exist do what you, okay also catch up something that normally n substrate show lower phi ms p substrate show much larger or vice versa think of it, okay yes.

Student: (())(44:57).

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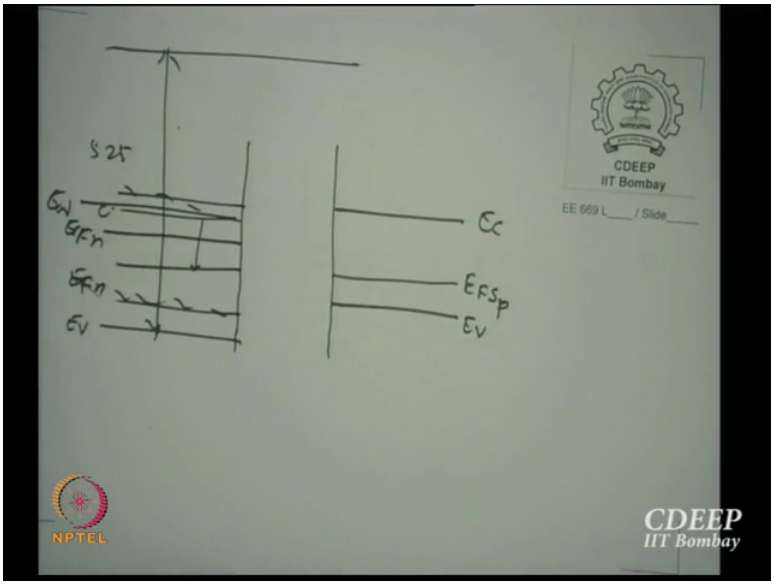

Professor: If, okay now I will have to do (())(45:01) page so that you understand, okay I have semi-conductor both side poly is also treated like good semiconductor though it is not, okay. So now Fermi levels are aligned in p substrate this is Ef in n doped poly, okay they are all aligned now for example. So now of course initially they are not aligned but after the I am saying so if it is n type this is the conduction band and this is the balance band, is that okay? if this is p type this is the conduction band, this is the balance band, is that clear?

So this please remember the work function if they are aligned this is the situation but in real life they will not be aligned because Efn will be higher compared to Efs. So they are little here and this is your Efn now this has to go down to match to Efn equivalently saying let us say just for this if this is your semiconductor this is 5.25 eV from the balance band let us say forget about right now going up only this, how much is 5.25 this is your Fermi level, sorry, “Efn abhi mat karo ye Efn lo abhi n substrate hai aur ye balance band hai”. So this is 5.25 minus Eg by 2 minus phi f, “yaha kitna hoga 5.25 minus Ega by 2 plus phi f toh dono ka difference me 2 phi f ka difference aagaya phi ms me”. So even if you are having silicon both sides there will be always phi ms present to you the idea is the poly gate always will be opposite polarity to the substrate because of the technology we do but it is not 100 percent true now we do some initially monitoring and may change, what is the disadvantage of having n or m?

Student: (())(47:15).

Professor: Vt can be adjusted that is the work function engineering I am doing but the problem there is additional mask because when I am doing (())(47:22) I cannot open gate so I will have to do another mask to open the gate and that takes extra mask 1 million dollars, okay and now more, okay. So this is something cost wise otherwise it is much easier now because if nothing is working cost is what, so I will put money so that it works, okay. So in technology something like this if things work at the lowest cost fair enough it does not then take, okay.

So this finishes of course there are many more things can be told this finishes oxide, okay thermal oxidation with all kinds of measurement all possible technologies dry weight, dry everything I shown you pressured oxidation I gave you some formula that if you pressurize the growth rate increases, okay steam it increases. So I have given you general idea of silicon dioxide growth please remember this is silicon converting to silicon dioxide so therefore it is called growth, if deposit any substrate maybe silicon and I deposit something that technology is different from this, okay which one will be better if am depositing silicon dioxide or growth, growth because all bonds all possible to be satisfied in the case of deposition that is a major worry (())(48:45) oxide siting on silicon does not give you good interface states I mean simply because they are not grown out of each other, is that clear?

So there is issue in other insulators being deposited on silicon, okay though you know hafnium is very good and one of the problem is mobility so you do some other gain to improve the mobility, okay some (())(49:09) stress you apply and so that you get additional mobility enhancement, okay so the technology keeps growing because of some failure some success so match which is more success, okay. So this finishes basically the oxide technology which I was talking about thermal oxides are one of the ideal oxides but now oxides itself has to be given up.

65 Nano meter process still uses silicon dioxide the next equivalent oxide which was tried or equivalent insulator was not hafnium or something we tried silicon nitride which is also grown out of silicon, silicon nitride has an advantage or disadvantage whatever you say is directly constant is not 3.9 it is more than that it is 6.2 so it is high k than so the first attempt to go for a higher k was due to silicon nitride but silicon nitride is a stressful thing because silicon nitride creates hell of tensile stress on the silicon, okay so it improves mobility for some other reason but decrease in mobility for some other reason so how much to match, okay so there is a then there is come with a word called stacks silicon dioxide, silicon nitride or silicon oxinitrides or

gain circulate in technology and,"ek paper har k sath", okay this is called bias temperature stress measurement very important measurement which we do particularly this is true for mobile ions concentration to know how much sodium, okay.

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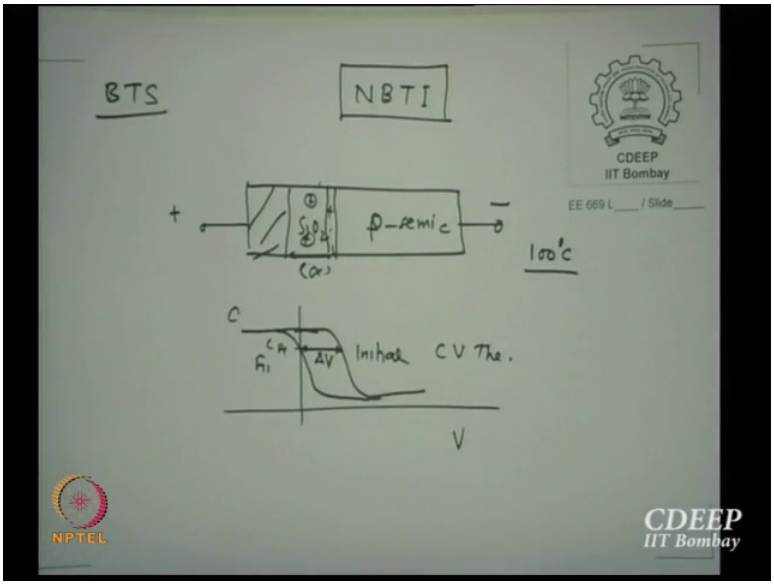

So what we do is the following you have a capacitor this is your SiO2 or any insulator and this is maybe right now (())(50:57) talk about p or n whatever it is, okay this is your mass capacitor and there are sodium everywhere but if you follow poison's equation properly that is rho of x in the oxide the charges which are away from the interface do not because it is proportion to the distance the effect of this charge here is practically 0 t by t ox as we say so it will be 0 and maximum effect will come at the interface if the charges are at the interface they will have immediate reaction to the semiconductor, far away from that they have the least and at the test side we will have no effect, okay at metal silicon dioxide interface any charge siting there will have minimal or 0 effect on the semiconductor charge theory, now this gives me idea but sodium can sit anywhere, okay it is not in my hand that, oh please go here, okay.

Student: But that can terminate the field (())(52:04) charges placed near the gate interface.

Professor: I agree but metal have infinite charges they do not really worry too much they interaction is very quick and very fast, okay. So sodium come from any Na2O bond and this is Na is very easily released at some temperatures, okay even at thermal room temperatures. So what we do now that I want this all this sodium ions to go to the interface, so what polarity of

voltage I should apply? Sodium should come here so I apply plus here minus here, okay so if I apply here positive the electric field is direction from positive negative so all sodium ions will try to go towards interface, okay but they will not remain there because they are thermal energy with them they will keep moving firstly how many will be available also we do not know because they are whether (())(53:07) bonds are not.

So the first thing we did we heat this wafer, okay around 100 degree centigrade the mass capacitor is heated around a 100 degree centigrade most of the ions are mobile because they will now leave the Na2O will break and most sodium is free now, okay I applied sufficiently high field across this capacitor so almost all sodium ions will come towards interface here, is that clear? But as soon as you cool them they may go back as soon you remove the field they are still heated so they may go again I mean there is no one to stop them sitting there.

So what is done is that first time you keep the field on then all the ions are moved to the interface hopefully so you actually let the wafer cool with the bias on, is that clear? You let the wafer cool till bias is on and once that cools to room temperature then you can remove the because now they cannot do mobile because at room temperature they are few who can go back, okay. So all the charges are now left at the interface like a fix charge, okay so if I have a some charges at the interface and I measure high frequency Cv let us say p substrate so like this see this is a positive charge, where Cv will move? Minus Q ox by C ox towards left side so actually this is initially this is final and if I know my Cfb this delta v essentially is a measure of sodium charge because prior to that we assume hardly any sodium was there so that was initial I heated the wafer, applied bias, cool the wafers, remove the bias and measured the Cv, okay and please remember so the electric field when I apply should be larger than the measurement electric fields because otherwise they will come out, okay so they are that is the way it is very heavily voltage first 10 volt you have to apply push everyone there, okay once they get pseudo bonds at the interface then we actually remove the voltage and then apply at much lower voltage Cv's, okay.

So this delta Vq is equal to C delta v, is that clear? So I measure C I know the Q I mean this delta v so I know this Q must be proportional to Qna into that distance typically it is becoming Armstrongs so this how much is sodium concentration there is now known and we do not talk of concentration, what do we call? Density per unit area forget about how much is the thickness per unit area is how much is sufficient to know Q by Q is also density C ox is Cf is also density this

delta v is the measure of the sodium same measurement can be done for fix stock side charges, why fixed oxide charges are always present so we instead now there this is not initial but theory Cv theoretical Cv.

So you have that Cv which is theoretical first and then make actual measurement on a capacitor the shift is because of what, Q ox so that is also monitored by talking a theoretical Cv and compared with measure high frequency Cv the shift is at Cfb is the measure of Q ox by C ox is the shift so Q ox is monitored from Hf Cv by same technique no temperatures just make a theoretical Cv (())(57:12) Cv with no Q ox that is Q ox if phi ms is 0 and then use this this will give you some idea of phi ms plus Q ox by C ox phi ms is again calculated by the work functions available and then you figure out how much is Q ox.

So this is the same Hf Cv can be used to figure out the fix charges as well as mobile charges, so this is the technique which we.

Student: (())(57:41).

Professor: No it does not because the charges do not leave come they have a time constant (()) (57:47) never do that theoretical Cv just draw you are perfectly justified in theory but in real life charge does not move at all all of it, okay 90 percent will do then that 10 percent will be error for you, your thinking is very good but thinking to reality has to be verified, okay in case in your case measurement comes same it is very good nothing wrong that means your oxide has very fewer charges they could move out but larger density will nothing 90 percent will at best move, okay.

So this is Hf lf Cv Hf Cv quasi-static everything is available in number of books number of journal papers as I say in till 2014 maybe this number is million or so in the oxides, okay you can see,"zara sa bhi hila k log khus hote hai, okay". The last part in this why this there is a word which professor Mahabatra keeps talking these days of course now he has moved to (())(58:46) so earlier then he was working on flash he was keep talking about nbti everyone asked me,"ki sir apne class me kabhi nahi padaya mene kaha tab nbti koi sochta nahi tha" now in flash it started and (())(59:03) the programming that is writing and reading is through a thin oxide of this through which the carriers are brought by tunneling, one is (())(59:13) other is tunneling. Now if you do number of such read writes, okay or programming and reading the oxide does not is does

not have a free of charge it actually retains charges all charge does not come that is what I am saying and that this charge is inside the insulator which is a floating gate there is no way I can move them out and these charges are sitting there they may when I actually apply voltage to read and I figure out that these charges are now contributing, okay this is called bias because device starts at higher temperatures start working and since the temperature rises they move and because of that there is a instability in Vt's and instablitity in actual measurements of the eprom beta e equare prom beta.

So flash because you keep writing erasing everything in one way you want all thing to tunnel down it does not happen, okay and if does not happen then there is a what is called bias temperature instability which is essentially negative because of positive charge sitting there electron siting there so that is why it is called nbti there is a pbti also holes possibility other kind of substrate which is smaller effect and therefore not much talked about, okay there are some 100's of theories whether nbti is really what I am talking that is another area you can talk to professor Mahabatra.

Now let us start another new topic still 15 minutes we can introduce it, please there is a lithography which is the actually if this word would not have been there, no IC could have been made, okay.

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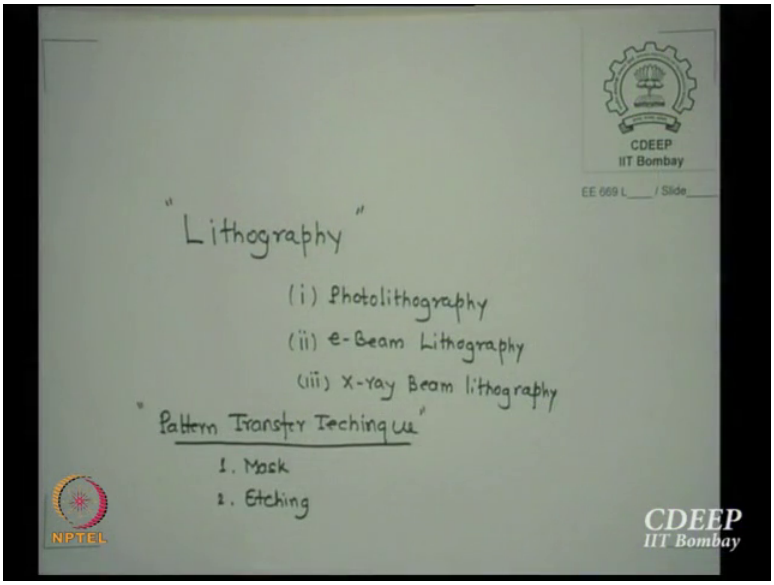

So if you really want to make an integrated circuit or any semiconductor device (())(60:58) you have to go through this process lithography this has felicitated making IC's and this has also now hindered process of enhancement, okay. The lithography techniques are the major worrisome part now when we are looking 7 nanometer or 11 nanometer nodes, okay we will see why they are worried about and what is the solutions, okay Intel is still struggling to go for 7 nanometer extended uv's and it may extended uv machine may cost roughly 100 million dollars in making first machine and still they are not successful there are 7 companies trying 5 given up only 2 are now trying, okay. So you can see (())(61:44) and Intel is only one who are still trying to make extended uv's I know in my time whether it will succeed the only hope it succeed because my son is also working on that so maybe, okay at Intel so I will hope for the best for him, okay.

For the lithography there are three kinds of lithography maybe fourth also but at least 3 e-beam lithography, x ray beam lithography photo word suggest that the something has to do with photons so lights so it is something light related lithography e-beam instead of light if I have electron beams to do that job we say e-beam lithography and if you do instead of e-beams if I use x rays then it is called x ray beam lithography and if I use ions I will be ion beam lithography, okay.

We still do not want work on e-beams, x rays, ions beam you want to work on photo lithography that is the large amount of wafers we can be produce by these are all not manufacture able technologies that means the through put is very small if the through put is small cost is higher, okay in photo lithography the through put is very very high so cost wise in industry things like photo lithography. So we are now trying to improve photo lithography as much as what e-beam can do, okay or of course x ray beam may never reach (())(63:12) x rays but at least you will try to come closer to Ev's, okay that is the effort what is we are now looking into but once you talk of photons the optics starts coming into your mind because there is a light and light actually is essentially governed by optics.

So lithography techniques require lot of optics, okay some idea of diffraction, some idea of ray (())(63:36), some idea of (())(63:38)many things are required to actually understand how why certain things are not happening and certain things are happening then whatever lens system you put there are 7 kinds of abrasions there then how to avoid some of them some may never (())

(63:55) will never go so how do you take care in your wafer on that so all the problems of lithography are related to optics, okay this is one aspect.

So what is we do actually in the lithography? The actual process of lithography is very simple, okay the basic idea litho means this something some kind of statue or some kind of body if I transfer as it is on somewhere I say lithography, okay "ek picture yaha se yaha par", okay same if it is the copy it can be sold as a original and make money out of that painting many people are actually sold the such varieties so if you have a (())(64:39) of arts please do not buy things are which are copied which are much cheaper in fact from the originals, okay lithography does that so transferring an image from somewhere on silicon is what our job is this image is essentially called pattern, okay.

So this pattern transfer from some other place which we call mask on silicon is essentially called lithography, okay why do we want to do?

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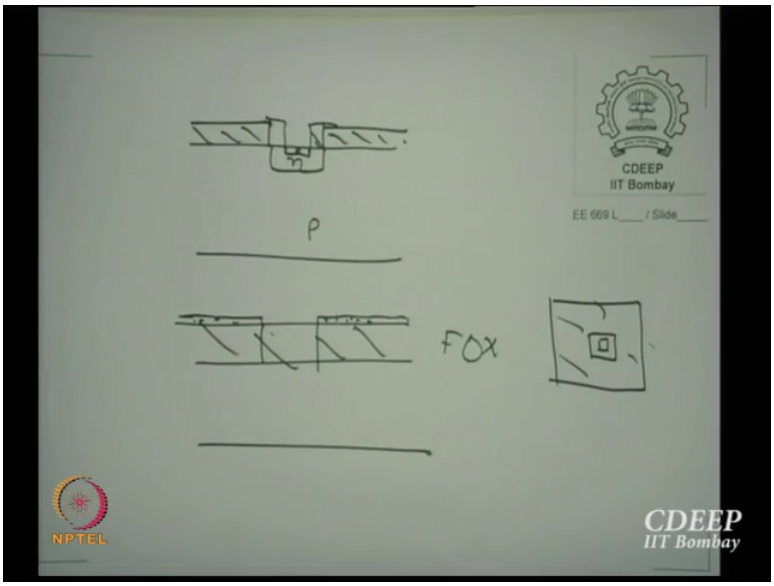

Just a minute a quick this if not to do this, "abhi apko exam me ek problem bhi diya tha" I want to do selective diffusion let us say only this region but whatever process are solid state diffusion we did what was that if impurity start they will not see anything they will go everywhere this is called isotropic, okay.

So I must rotate the regions where I do not want n to go, okay so this is called selective area diffusion that means I must restrict this area from the rest so the rest of the area is called mask it does not allow n to impurities to go, okay for silicon dioxide is a thick oxide which is fox the word I use their field oxide thicker oxide actually does that job, okay and when I diffuse now so first thing I must do I must have a wafer I must have grown thicker oxide called fox, okay then do some patterning on this such that I code something some this is the word we will use is called photo resist I create a pattern through a mass on a photo resist and edge photo resist only from there is called developing and then a silicon dioxide, see if this photo resist will not allow anything below to be h so this is the mask for silicon dioxide for edging.

So this resist edging, okay here there is no resist so the silicon dioxide is exposed so I put it into any ion beam or Hf liquid and this silicon can silicon dioxide can be edge so a window is created in so what should be the kind of mask you should look from this in the center I want this the rest should be should not allow anything to happen, is that clear? So this is clear field mask we will see this later.

So we have to create this pattern this is a pattern now, so in a mask transistor if you see there are so many areas so (())(67:28) gate and there are number of contacts elsewhere you are doing so every time you are going to do a process for example if I want to make a npn transistor pnp transistor I now want to make inside this n region a p so I must gain somehow protect this by another process and gets inside this, this is called alignment and there will be millions of such on the wafers so everywhere this window should get inside the earlier window, okay then only I can make a pnp there this is selective area processing and that is only possible through a method of transferring patterns on silicon to do this we will put some resist which is called photoresist and these photoresist will allow us to do selective area edgings and therefore selective area processing.

So question is what kind of resist it should be? Which are responsible to allow this so there must be some light initiated process light activated process which this photoresist see before we go I just named the two, one is called positive photo resist the word is positive or resist are essentially regimes one of the thing which all environmentally keeps saying that you know plastic is one of the worst thing to happen to this society which is true to some extent from the environmental point it is non-destructive.

However polymers are the invention of this century 2000, okay this was the invention because it changed all concepts of us all aero planes to everything if you do not have plastic you cannot survive including the this Formica everywhere you have a plastic. So much of the problems of human race was solved by plastics but we keep saying we keep hearing from environmentalist plastic is the worst thing to happen, why? So people in chemical engineering must be shouting day and day out, ”ek toh hamne itna kiya” and everyone is abusing us, okay.

So recycling is one possibility and they are not biodegradable so one of the research in resist if you are working there many IBM people are working biodegradable resist, okay so they are something which bio people can you put some ants or something which will eat away that, okay something,”nahi nahi apko hint dera hu me jaise me circuit walo ko bolta hu battery research karo yaar baki kya hai, battery ka hi problem hai sab jaga bar bar charge karna padta hai” smaller area larger (())(70:08) “hogaya apka sab kam hogaya toh kaiko itna IC and ye sab battery bano”, okay.

So this resist essentially positive photoresist positive I will come back to it later but I just want to name them today a positive resist is one when the it shines receives light it actually, okay first I must say regimes are essentially cross link carbon chains Ch3, Ch3, Ch3, Ch and they are open chains, okay but if they combine chains are connected to each other then they become cyclic chains and cyclic chains are very difficult to break that is why they are edgeable whenever there is a cyclic chain of carbon chains they are unedgeable benzene is very difficult to edge because there is 6 bonds on that 5 bonds on 6 atoms.

So this (())(71:02) property is essentially decided by linking of the carbon atoms, so what we do now if you shine a light and if this if you have a resist which is already cyclic and you shine the light and it break the bonds, okay these resist will be called positive resist so whenever light actually breaks the cyclic bond then we say you have positive resist then there is a negative photoresist which essentially is open chain resist and wherever you will shine the light it will become cross linked, is that correct? What is the difference between negative positive? Positive is when it is a cyclic regime shine light this is energy photons and it open the chain and opens it so it is edgeable, if you have open chain resist and you shine light wherever it shines particular where the energy is received absorbed that wavelength at that energy this linking process will happen, okay.

So those areas will become cross linked and there area will that then be non-edgeable because cross links are very difficult to edgeout, okay. So negative photoresist hardens the resist when receives light hardens means unedgeable parity photoresist softens the resist when receives light, is that correct? Since you are going to use two kinds of mask clear field and dark field we should know which resist to use when or if you are using only one kind of resist then the mask should be kept changed or if you have same kind of mass you should keep changing the resist every seconds different steps, okay.

So we will see tomorrow, tomorrow means next turn lithography first I will give you simple photo lithography technique which you should follow in lab generally, later I will show you actually what are other issues in 14 nanometer, 30 nanometer what is the problem going through so optics learn optics.