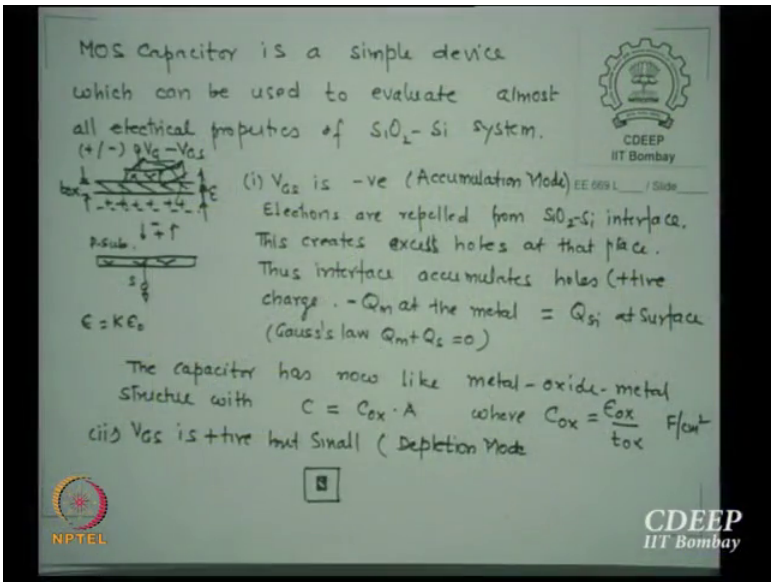
Fabrication of Silicon VLSI Circuits Using MOS Technology
Professor A.N. Chandorkar
Department of Electrical Engineering
Indian Institute of Technology, Bombay
Module 01
Lecture 14
Thermal Oxidation of Silicons (Continued)

(Refer Slide Time: 0:19)

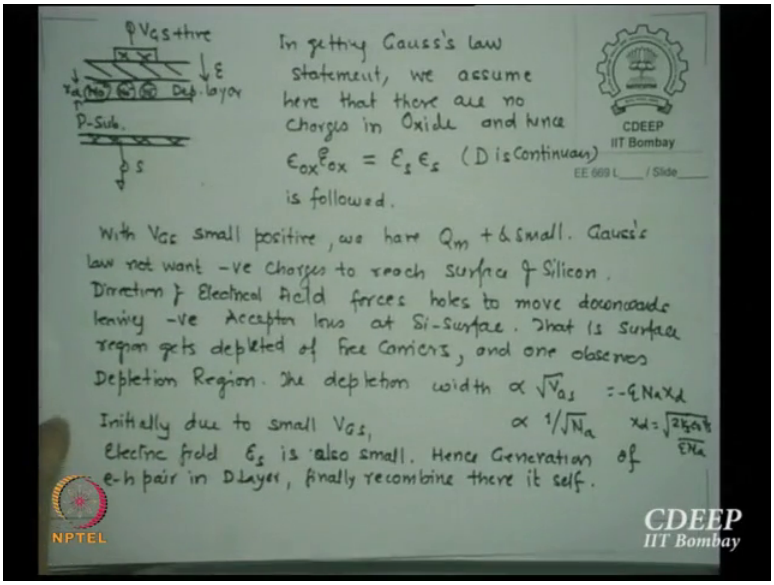


Okay we were looking for mass capacitors and we said there is a we always start with p substrate whatever is true for p substrate with opposite polarity of voltages it is true for and substrate, okay. So right now we look for p substrate for simple reason p substrate gives what we call n channel devices and we know n channel devices are better in performing compare to p channel devices as far as there area wise and threshold wise values are concerned simply because the mobility of electrons is higher than mobility of holes even at this surface.

And because of that n channel mass rates are most used as drivers and p channel devices are used as loads but in c mass this statement will be has to be modified there is no load there is no driver both coexists then we have to do something to p channel so that it becomes equivalent of n channels, okay digital course will tell you more about it what is a logical effort when needs to make it equal, okay.

So we said that if Vgs is negative so the electric field is from bottom to upwards hole starts accumulating at the surface and since holes are more like a metallic system so you only getting net capacitance of oxide which is C ox decided by epsilon ox by T ox please remember capacitances in our case are mostly defined as per unit area they may monitor actual capacitance infrareds but the theory always you will have C ox which is epsilon ox by T ox simply because Q is equal to Cv the basic Gauss's law has to be satisfied and Q we use there as charge density and since it is per unit area there C is also coordinate area here because voltage cannot be per unit area voltage at the per unit centimeter which will be fields but otherwise there is nothing called per unit area.

(Refer Slide Time: 2:30)



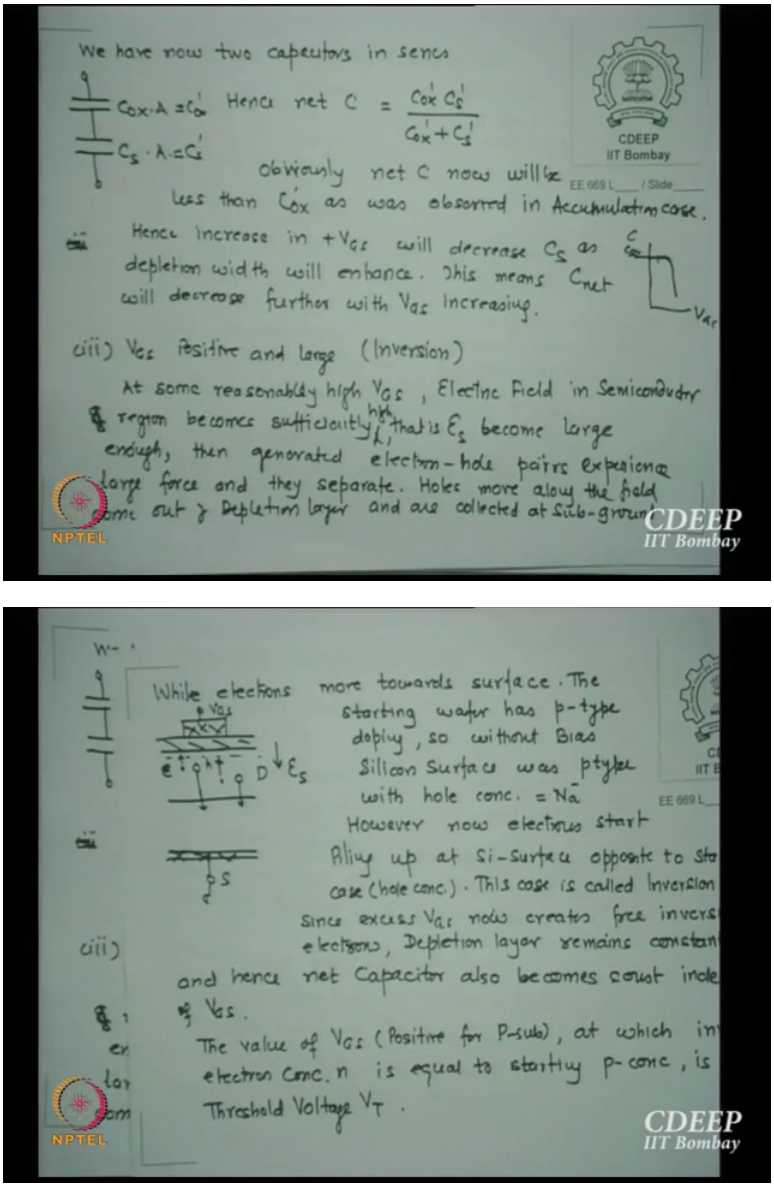
So everywhere you find that I normally use C ox as epsilon ox by T ox we also said that if I apply Vgs positive and small the first thing we have seen the electric field is now downwards the holes I repeal down because of this and since holes leave the surface there are accepters which are negatively charged appears there and this is called depletion layer. We also assume that there are no oxide charges as of now and therefore if the D vector is continuous then we say epsilon ox into T ox is epsilon s into t epsilon this is electric field the reason why I started using this capital other kind of e is because this normal E is actually energy in Wien diagrams so this e and that E should not get confused E capital E is normally given for energy that is Q into v and therefore I normally write zita kind of e for my evaluation you can use capital E also there is nothing wrong with it.

Now if depletion layer will keep enhances if I increase Vgs because we can see from here will prove this that depletion layer is proportional twice case epsilon not Si s will see what is Si s surface potential by Q and e. So if one can see from here that if I want larger charges to appear there are two ways either this na should have been larger which is fixed substrate so we cannot (())(3:59) so xd must increase as the Qm that is the charge on the metal plate Vgs increasing means metal charge increasing which means there should be more and more depletion layer widths so that the charge is balanced by Gauss's law net charge is 0 across the loop, okay.

Now this theory is very simple and as I said right from 7th standard we have been telling capacitors, registers and inductors and even after your mass stress (())(4:31) that much, okay nothing more. Now if we initially when the Vgs is small the electric field due to the depletion layer is also very small relatively and since electric field is small please remember in semiconductor whether it is depletion layer or neutral region constantly whole electrons are generated this is called thermal generation where the rate of generation depends on generation time if these carriers are generated they also have recombination time so by that time they are actually taken out by electric field they may (())(5:11) so there will not be any contribution from free electrons and holes because they will be able to recombine the electric field is very small.

However if I start increasing the voltage at the gate down this electric field it was depletion layer will also enhance and there is a possibility that the force on electrons holes maybe exceeding now and if that happens this is what we say, okay.

(Refer Slide Time: 5:44)



Before that maybe in the depletion region I am sorry before we come to inversion so if there are only two capacitances involved due to the depletion region which is called semiconductor capacitance and the oxide capacitance look at the figure one capacitance due to oxide one capacitance due to semiconductor or depletion layer.

So they are in series and series capacitance is always this dash is only to take care of area nothing more, so the net capacitance is C ox dash by Cs upon C ox dash plus Cs dash since Cs dash will start decreasing as voltage start increasing please remember as Cs dash increasing voltage start increasing depletion layer width increases so epsilon by x will actually small

decreasing if Cs dash decreases the net capacitance will also decrease as voltage increases Cs dash decreases therefore the net capacitance start also decreasing that is why higher frequency Cv you see decrease in capacitance as you increase Vgs you can see from here the capacitance start decreasing as I increase Vgs, okay.

However, this Vgs is still not large enough to create large electric fields in the depletion layer but once this electric field is large enough that is Vgs is sufficiently positive there is a possibility of hole electrons get separated by the electric field in this depletion layer, holes will move down because the electric field is downwards and electrons will start piling up at the interface that is something very interesting can happen holes simply move down at the depletion layer electrons will start moving towards the interface if there is a silicon dioxide electrons cannot cross the barrier there but they will set at the silicon interface, silicon silicon dice interface since we started with a p substrate at the layer just below oxide is become electrons negative now we say you are in inversion region you have inverted carrier inverted the layer there you have p substrate and now you have negative n free carriers available.

So larger the Vgs you apply more and more electrons will come and then the charge balance require, there are how many charges are now there? One is the depletion layer charge plus the inversion charge but the way inversion charge increases with electric field is e to the power something Q Si s by kind of kt whereas in the case of depletion layer how it increases, root upon is proportional to xdn which is proportional to root of Si s, okay which moves which is stronger exponential terms are very strong.

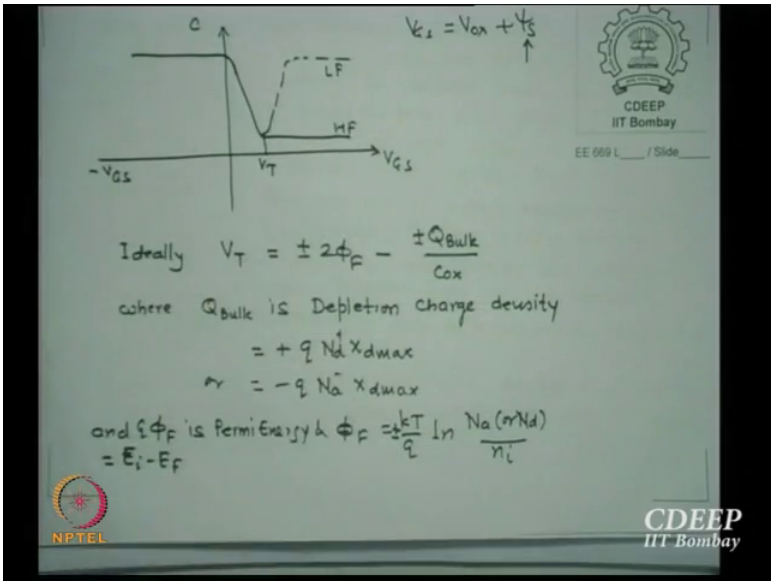
So whatever additional charge you put on the metal will be now easily supplied by inversion charge and depletion charge does not exceed it does increase one cannot say it does not but in ratio it may be 1 to 1000 so we say depletion layer becomes constant and all the charges are now made available through inversion charges so the balance of net charge 0 can be now attend through the available free electrons rather than from the depletion layer. So there will be a fixed depletion charge plus inversion charge is equal to whatever Vgs you apply corresponding to that whatever metal charge you have and that always will be net charge will be 0 please remember why inversion is stronger because the way if you solve the poison's equation there you will be able to figure out with continuant equation we will be able to prove that e to the power Si s kind of terms.

So si s increases surface potential carrier generation is very fast, okay and therefore this electrons are available in larger number even a smaller change in the vgs so you do not need to increase depletion layer since the capacitance now if the charges here are not very very large right now or the variation in this charge density is not very large we will see this is what we want to prove later the net capacitance is now whatever is the maximum bulk charge you create here that divided by xd max, xd max Qa xd max what is xd max at the potential one Vgs depletion layer becomes almost constant that is called xd max someone asked other day what is xd max so I was little worried but now as a microelectronics students at least if you do not know mass cv (()) (10:36) leave the group as fast as you can, okay.

The value of Vgs at which this then you know what is called invention layer what we call threshold. We define a threshold voltage as that voltage of Vgs when the number of electron and electron density electron per unit per cc is exactly equal to the substrate concentration, is that clear? If na is the subset concentration any holes so when the electron concentration is exactly equal to any at the interface or surface then we say we are in a strong inversion case but where inversion will start whenever electron starts there inversion has already sit in for a one Vgs even if the electrons are smaller than number of holes available in substrate even then inversion has set in this is called weak inversion, but what is the definition of threshold we will give? We will give for a strong inversion and in strong inversion we made a mischief we say okay whenever number of electrons per cc is exactly equal to na's at that voltage we will say threshold has the voltage Vgs is actually the threshold voltage that is the definition not very correct but it is okay that is the way to find I define that, okay that is the way it is.

So if I plot capacitance versus voltage characteristics this is of course again professor Varsi will tell you in more details so please look for that.

(Refer Slide Time: 12:15)



If you see very carefully if I have a two curve as shown capacitance versus voltage for a piece of straight mass capacitor and I figure out for minus Vgs its accumulation and therefore oxide capacitance is constant if I increase Vgs the depletion layer starts enhancing so the net semiconductor capacitance decreases so net capacitance decreases and somewhere here at this Vgs sufficient electrons are made available so we say inversion has started and depletion layer capacitance is constant, if that is constant C ox series to c depletion is constant so it becomes constant this is called higher frequency cv.

The assumption here is that the frequency is high enough which is typical even megahertz to 10 megahertz one is standard but many people use 10 megahertz then you can use 100 megahertz. What is the way capacitance are monitored? You can do through a have you anytime thought about the meters which you see lcr meters and how do they monitor capacitor all that we are doing there are passing a current through 1 upon 0 omega c and measuring the voltage vac by iac is 1 upon 0 omega c if I know my omega I know my capacitor that is all that we do, okay.

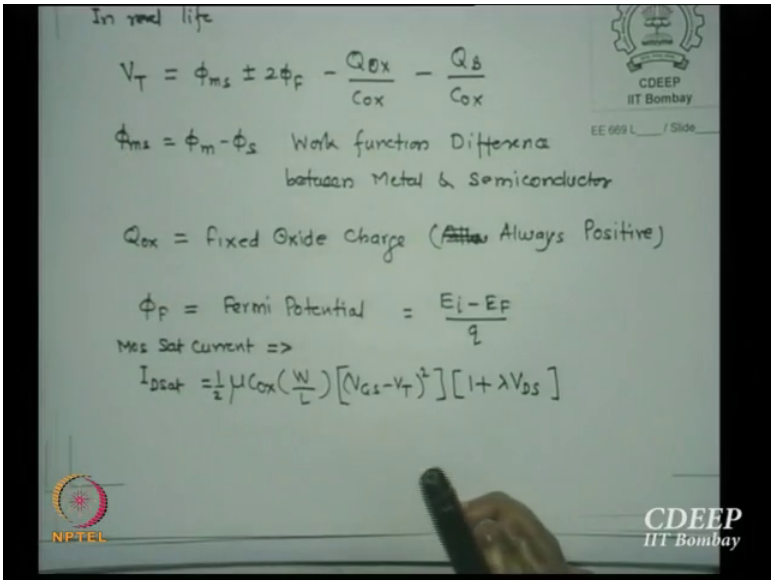
So the frequency of measurement is this omega, okay so AC single which I am applying to measure a capacitance it has a frequency so this high frequency cv is this measurement frequency which is 1 megahertz and above at those frequencies we say no other charges follow this change in voltage if AC becomes positive negative if the charges at the surface do not response to that only depletion is fixed so it remains constant there oxide capacitance is without

this you are measuring so C ox plus a series of Cs dash or Cs is all that capacitance you will see in all this cases so capacitance is always seen as constant once the inversion sets in.

However if the measurement frequency and we have lot things to show later if the measurement frequency is smaller maybe 1 hertz, 10 hertz then this charges change in inversion layer charge, change in everyone can follow this (())(14:46) frequency signal or voltage and if that follows then some of these capacitance will d cube by dv is capacitance if the change of charge is followed by v then we say there is a capacitance so then the (())(15:01) capacitance will start also appearing in your circuit and then you will see if large at the after inversion and then we will show you this that the oxide capacitance the net capacitance climb backs to the oxide capacitance, okay.

So low frequency after inversion you climb back to the oxide capacitance, we will see this little later few minutes how do we evaluate everything out of this why we are spending this time because at the end of the day for me the mass device performance which maybe I will show you first so that, “pehle yeh dikhao tabhi kuch ap manenge aisa hai toh”, okay.

(Refer Slide Time: 15:53)



I will just show this slide of course this right now we are not done all the terms here but the threshold voltage in real life is given by phi ms plus minus 2, why plus minus if na it is 2 phi f plus and if it is nd because charges are opposite it will become minus 2 phi f minus Q ox by Q ox is the oxide charge and we want to monitor that minus, okay here also we should write plus

minus because minus Q na xd or plus Q nd xd depends on the substrate you start with but this is always minus, so minus Q na xd make it plus plus Q nd xd will make it minus please remember very interesting thing phi ms is always negative, okay always we will show you this for a pre substrate or n channel device 2 phi f is positive Q ox is always positive, okay so Q ox by C ox is always negative Qb which is Q na xd minus will become positive, so this is positive term this is positive this is negative term this is negative term.

So that can happen there is subtract, okay it may happen in some cases that if Q ox is very large then this plus this will become larger than 2 phi f plus Qv by C ox or Q na xd by C ox, what does that mean vt will become negative for n channel device we always want threshold to be positive turn on, okay Vgs should exceed Vt to start currents, okay now that may not happen. So one of the technology worries are how much Q ox I can maintain, okay so that this plus this is always smaller than this plus this this is something where in the case of p channel device this is minus because this is plus Q na so this is minus, this is minus, this is minus, this is minus so all four terms in p channel devices are relatives of Vt for p channel device is always negative the larger these values more minus Vt will appear since larger Vt means you will require larger supply to Q at the same current so p channel devices will require larger threshold larger supply voltage to get the same currents Vgs minus Vt, is that clear because Vt's are negative.

So there also we must this Q ox because then Vt becomes lesser negative, okay somehow should increase 2 phi f, okay (())(18:33) 2 phi f doping should be such. So if you can adjust your doping and oxide charges in technology then I will be able to get Vt and equal to vtp in circuits I want n channel devices should have same as p channel Vt's (())(18:51) sign wise Vt n is equal to absolute value of vtp, okay magnitude of Vt that is what we say symmetric circuits.

So we will like to do that that means some way in technology for channel I must control very strongly so that vt becomes as small as possible which is closer to because n channel will be smaller, why it will be smaller? Because two terms are positive, two terms are negative so it will be smaller so to if I want little more positive I must increase actually 2 phi f, okay so that I get larger the doping I will get more Vt out of it.

So larger Vt if I want I can always increase the doping in the case of p channel I want 2 phi f to decrease so I will actually reduce this substrate doping, okay that is what p channel areas are

different from n channel areas in all CMOS circuits, okay. So this is my expression this term here phi f minus phi s will look into it time permitting since the work function of the gate whether it is aluminum, gold or titanium or any other (())(19:59) or any other these the work function will define little later is the energy required for a electron to take out of a metal is called its work function in vacuum, okay.

Since that is the material property semiconductor work function is of course is depend on the doping in the semiconductors so one can see from phi f minus phi s phi m depending on what kind of metals are used this phi m minus phi s can change, okay one of the recent techniques of last 5, 6 years is called work function engineering so the threshold is actually adjusted my the metal which I put, okay because I cannot done play too much about the other values I say okay let us look at the other metals which probably can vary my Vt, okay this is something in Nano meter 45 Nano meter down or even 28 Nano meters have not same aluminum of course have been given up long time but other materials are looked into whose work function difference is more controllable and one can choose of that (())(21:03) sulfide for example is very strong candidate for that, okay (())(21:07), okay.

So this is why say why phi ms is so very crucial but phi ms is the term in Vt please remember so that has to be looked into, Qox is always positive always positive and very close to the interface very close to the interface inside oxide that now this term just cannot be avoided I can minimize it how much minimum I should have that it should have a much influence is all that we can try, okay then the phi f of course is called Fermi potential which is nothing but (())(21:41) for me and energy minus the actual Fermi level divided by q and if you look at mass device current, okay let us say for any of the device the saturation current I Dsat as it is called is half mu C ox W by L Vgs minus Vt square 1 plus lambda Vds so any change in Vt any change in mu is going to affect my current and current means in circuit everything depends current available for a given bias or given Vgs but this value how much ideas I will get is decided by what is mu I get and what is the threshold I get.

So the technology people are forced to worry about mu and Vt because the current people are telling this is what I want, okay because of the circuit performance is decided by charging current for the capacitor I want for a smaller voltage large current currents of course power deception may increase we will see whether then the other people say no and reduce the current, okay then

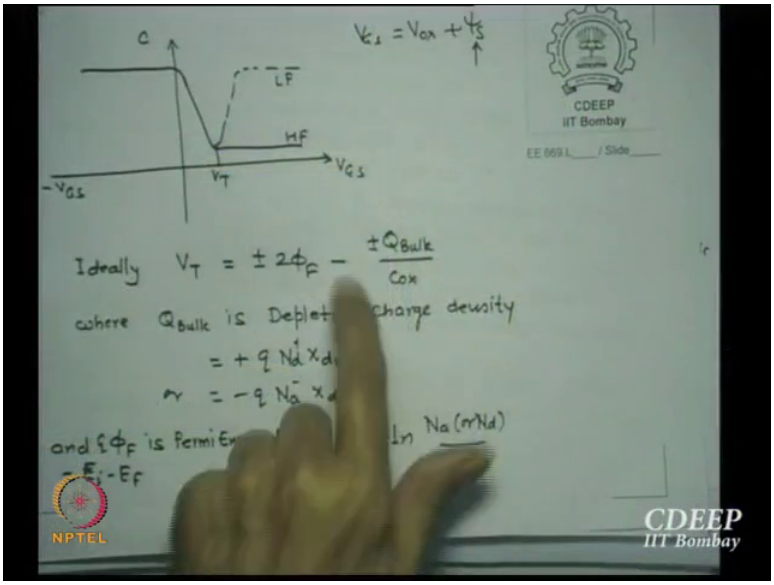
what do we do? So we play games on that, okay as much as possible. So this is why we say technology why we look into all this theory because they will come and tell me I want this Vt and plus minus so much and I want this mobility.

Now I am force to now work to my this I want to go back in see in theory which terms actually affects me and the threshold as well as in the mobility and this processes are those terms and must control in my process because that is how the mass circuit technology will actually perform this is gigahertz Intel processor may want to make 10 or something it is okay saying is very simple the power may boost by 10 times to 100 times then it can be done but I want power to be 1, 10 we want the speed to be double this is something which is triangle as I say you push 1 the other will go down, okay.

So that is where the technology people are called and say," Are thoda madat karo bhai", okay. So one other of course is the choose materials which are higher mobility itself, okay so that one probably do not have to too much worry about silicon, okay but we do not want to listen silicon technologies, okay as I say, "2015 me dekhega nhi but 2050 tak ap log CMOS k uper zinda nahi rehsakte kitne bhi research karlo ye mera wada hai apko" silicon will never go if anything else then money may will matter if I know if the cost have one thing is 1 rupee and other is 1000 rupees even if it is 5 times better, 3 time I say,"yaar 1 rupiya thik hai".

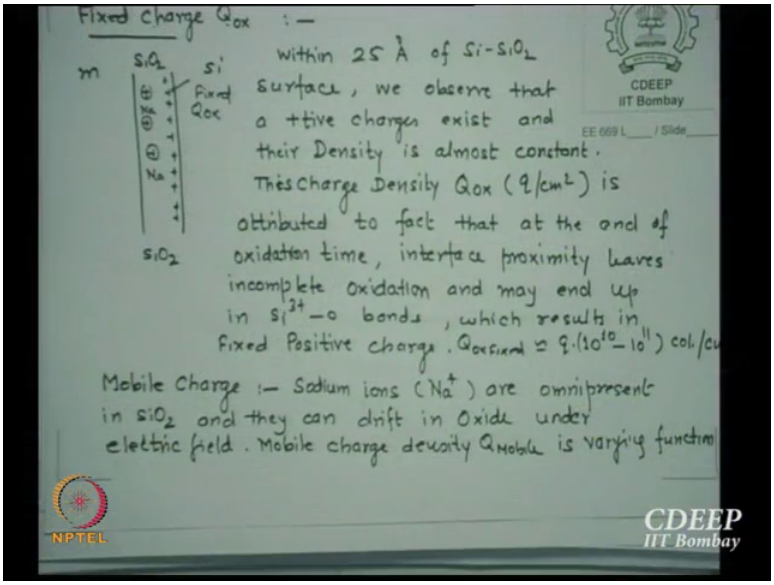
So that is the game technology is essentially money related economics side, okay.

(Refer Slide Time: 24:58)



So one of the thing which we will look into later is this Q cox which as I say in this case I have said Q ox is 0 and phi ms is also 0 is called ideal capacitor, what is it called? Phi ms is 0, what does phi ms 0 means? The work function of semiconductor is same as (())(25:10) impossible but assume and if you assume it is called theoretical cv ideal cv, okay in which phi ms is 0 and we say there are no oxide charges, okay then whatever Vt we get is essentially ideal Vt which is not the reality but from there since I know theoretically what is ideal, what I can do then? If I measure something then I know the change and I know this is because of this, is that clear?

(Refer Slide Time: 25:47)



That is exactly what we do now there are fix charges which are called oxide charges which is essentially called travel and silicon sitting at the silicon silicon dioxide interface inside oxide, okay.

There are positive charges and there density, please remember this word density is always per centimeter square, okay and if your charge density charge coulombs per centimeter square cube by centimeter square, okay. So this positive charge is always exist do what you do they may be smaller they may be smaller or larger depending on the technology we use, so can you think why in 1970's everyone including ti or every company Intel or whosever are working goes in silicon IC process they are working on p channel devices till 1978 or 76, okay 4004 worth p channel microprocessors, okay only the first 8080 when it came it was n channel one, why? Because this Q ox could not be controlled so it Vt is to become 0 minus and therefore no enhancement, okay so we said okay let us work on p channel at least okay I will increase 10 volt power supply when it will enhance Vgs minus Vt I can get, okay.

So all initial processes where p channel devices simply because oxide charge was non within your technology control now of course great technology experts are (())(27:17) which can probably reduce this number to a great extent. Also one can see about this cube by C ox this term will becomes smaller when C ox is larger if C ox is larger means what the oxide thickness should be smaller this is what is happening it help you when you (())(27:41) the oxide thickness reduced

so your C ox increased but that C ox increase has some other problem where the current also start increasing so power start (())(27:55), okay so there are issues then the area started building so yeah you have to adjust many parameters together something for optimal values, okay.

So typically if I want fix charges it should be of the order of 10 to the power 10 percent meter square or 1.6 into 10 to power minus 19 into 10 to power 10 is minus 9 so coulombs this is the kind of charge density I am excepting 10 to the power 10 per centimeter square, what I may get is 10 to power 11 and whole my work is to see that this becomes closer to 1 into 2 or 2 into 3 into 10 to power 10 kind of numbers and that is my process, okay that is why processing is very crucial how do I actually push my wafers in oxidation furnace how fast I take them out, how much is the (())(28:50) I create, what is the laminar I could make there inside, is the temperature remaining constant, is the wafer was properly cleaned all these issue may decide the fix charges, okay and that is something very very crucial for us, okay.

Apart from this fix charges which are always which is called incomplete oxidation system called travel and silicon this is the kind of bond you get some other day some other time how trivalents are obtained but let us look at it further. Apart from this we kept saying the clean room environment we were talking that there should be at no cost sodium be inside, okay sodium or potassium or (())(29:35) such element be inside. The reason is sodium has a strong affinitive with water, water has strong affinitive silicon, okay so silica normal silica which is called soda glass has huge amount of sodium in that that is why it is called soda glass sodium based glass, okay SiO_2 with Na_2O inside, okay as a bond.

Now if this is soda glass huge sodium there is a density maybe 10 to power 14 per centimeter square so much large sodium. Now the problem with sodium is now, okay I have no objection if sodium present if it does not hurt me but if it hurts me I will have to check what how it hurts, it hurts something normally since phi ms is also negative or if I apply plus Vgs with reference to semiconductor I figure out this sodium which is well inside the silicon dioxides placed everywhere now and they are ions na's are ions and little energy they actually break the bond, okay this sodium ions have a tendency actually they are very they are quite large with velocity in the oxide which is where they can diffuse faster. If I apply Vgs which is the direction of electric field plus to minus so where sodium will go? Towards interface any charge which reaches at the interface will be seen in the Vt as Q ox plus Q na, okay that if okay one time I did it and I find

fine,"chalo ab paucha diya udhar aisa nahi hai", as soon as I change the temperature or I change the bias which are in circuit I will the sodium will come back partially here there, so what it means? Vt will be constantly varying as the mobile charge keep moving in the oxide thickness, okay but I cannot tolerate if Vt keeps varying my currents is varying my (())(31:40) will varying my power will vary that certainly I will not appreciate, okay.

And therefore somehow this mobile charges should be minimized and should be less around 10 to power 10 percent meter square all that I may tolerate, okay preferably 0 but 0 of course is nothing so as low 10 to power 9 people are now getting per centimeter square, so why sodium comes? We, okay the biggest source of sodium is we, okay however where everything and of course everything so that at least that perspiration is does not come out, okay but there are materials which are self-absolve like even polyesters or polymers they actually become sodium, okay over the time.

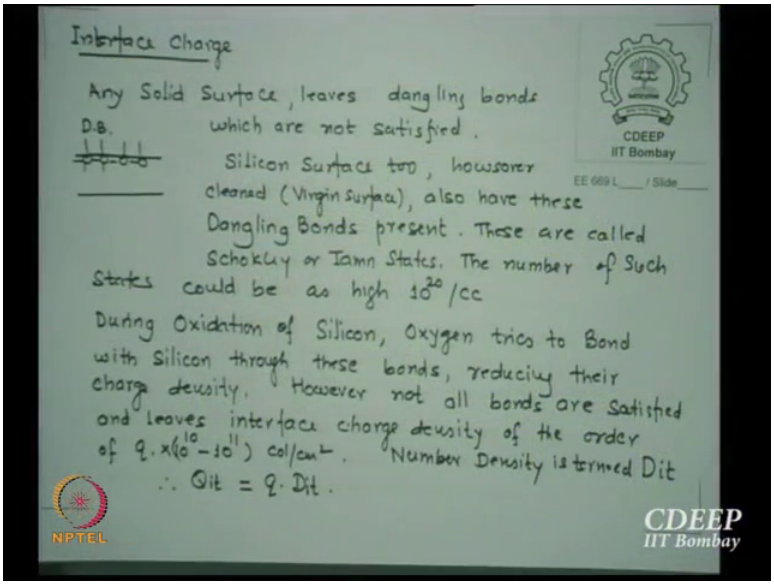
Now they as soon as you start air conditioning initially heats sodium is released, so come hurt me aluminum, alumina has been made various sodium sitting on it, okay. So as you move on this it scratches and sodium is released so do not think sodium is any clean room is sodium free of course the per centimeter square is very small that is density is very small but it is not that I can make it 0 parts where which I have also will have some sodium.

So in every sense and I am putting a 900 degree 1000 degree I am allowing sodium to really come, okay. So no time sodium can be made 0 all that I will do is to minimize sodium content in the facilities as well as from me. So (())(33:17) at least I know I will cover all of myself from everywhere two specs and small but you have to breath you cannot say I will not breath so that is the way you know whole problem you breath and there is a sodium, okay whatever filter you put here some part will come because air has to come in, okay.

So inhale and this has to be done so there will be a sodium inside do what you, okay. So please remember if any one says is sodium our statement is good nothing is sodium free in the world, okay sodium is omnipresent but let us look at the other side if sodium is less in your body you start getting cramps so sodium is very relevant material, okay so do think sodium is bad larger sodium blood pressure increases so you will have to reduce your sodium so all problem is sodium at old age I know everything now, okay.

So this mobile charges which hare essentially sodium based probably have to be controlled and we will see how we monitor all of this so what are the charges are said, I said there can be a fixed charge, there can be mobile charge and there can be the third charge which is worrying me most in fact, okay.

(Refer Slide Time: 34:48)



The last but not the least important is the interface charge and that is something which is probably partly controllable partly not controllable now if you look at any surface of any material solid material the top atoms of any materials the upper bonds will not be satisfied the lower bonds will be satisfied but the surface will always have one bond in the air or two bonds in the air, okay. Now this is called Shockley states or tamm states these bonds which are available at the surface and they maybe in large numbers because so many atoms in the surface so many bonds are available so we say these positive charges or dangling bonds dangling bonds are such a large numbers that they can be called they are actually named as Shockley states or tamm states.

However as soon as you cover this surface by any other material some of these bonds will get satisfied so this state surface states now will become called interface states and there number will decrease, is that point clear? From the surface there are too many output oxide on the top now silicon to silicon dioxides some will take bonds, okay some may still not be able to bond, okay. So whatever is not able to bond is a dangling bond siting at the interface, okay any charge in semiconductor (())(36:14) is equivalently saying there is a charge state or energy level in the

bond gap, okay what is any charge they are sitting they will create an energy level in the band gap of semiconductor, what is the problem with (())(36:31) this? They act like a trap centers, so why is that if you put something charge there they may act like a traps.

So some time interface states are also called interface straps, okay they are also called interface straps. Now this interface straps are not a constant quantity unfortunately, okay for example over the if you apply large voltage which is called constant stress for a given time or we increase thermal stress or the wafer is being held in a higher temperature ambience which in a real circuit will happen you are in a space or you are or it is receiving radiations.

Now all in cases this so called interface states are not very much fix they actually change, okay the problem starts there if they fix there is some control and the (())(37:24) are not fixed where do they effort, now one can see from that mass transistor theory or mass transistor somewhere maybe I will draw over here, okay "ek minute", I will come back to that this is my source drain and this is my oxide, okay.

Now if I create an inversion layer here by applying Vgs positive let us say now the current flows current flows from so electrons flows from source to drain due to the electric field lateral electric field called (())(38:09) currents. Now these electrons are not in the bulk alone they are near the surface if there is a charge state here and this carriers which is in conduction band you say now finds possibility of trapping, okay there are two traps there actually one is this silicon and silicon dioxide are two different material so there is a physical adulations like this whichever flatness you make never polish (())(38:41) between the two materials there cannot be one to one this, okay.

So there is a surface traps because of the adulations and surface trap because of interface state. So if the carriers are affected by interface states then the mobility will start decreasing and that is my worry because that current I decide I looked into its proportion into mu, okay. So if mobility goes down my current goes down my everything goes down, okay I am suddenly worried so this dit word or interface state density what we are saying they are worried too much about it because we feel that also is one but as I say even from Vgs going from minus to plus you will find dit's are not constant so we say okay at the bandage maybe anything in the mid gap how much is there the one more likely to in any trap near the mid gap near eg by 2 will have maximum probability

of trapping by electrons or holes, okay recombination center 50 percent probably here or here so that there was any one treasures to balance band only holes probably we can trap anyone closer to (())(39:57) can trap but in between they can do any machine the problem is exactly this the cv as we show they keep changing there as you move from bandage to bandage, okay and (()) (40:10) major worry, okay how much I how much dit really I have number which are density there that will influence my mu, okay and also it is indirectly not seen but we will see even Vt will keep varying with that because if you see the Vt variation here this Q ox essentially contains a term fix charge plus Qit what are charges in the interface, there are fix charges plus interface charge plus maybe I will charge all these charges at the interface will contribute to net Q ox which means Vt will get also affected by Q it or whatever charges in interface and they are varying so Vt will keep varying.

So my worries are not just this I am not only worried about mobility but I am also worried about my threshold getting not fixed, okay. So why we are so much worried in technology because people will insist the all designers when I am as a designer teach I will say the same thing they are great technology people, "ha yaar tumne ye nahi diya, okay" I told you I want this, okay we gave you something technology people they said you but this is not good enough. So every now and then the technology people where hammered now its last 10 years is the other way we can give anything what you can do now take designers do not have any options they cannot do much things they cannot think bigger system they cannot do anything, "oh low power now newest thing aagya low power ka oxide badlo ye badlo", so every time a designer does not get his performance he looks at process people, okay please help or I cannot do either way but that is the way work.

So now in 2011 onwards 5, 8 onwards no designers should forget technology or technology should know not about design because they individually together we can now solve the real issues which the newer technologies are facing (())(42:21) Nano meter process if you do if you are designing a chip of course (())(42:25) circuit is made so I am not bluffing (())(42:29) there 7 is already there. 7 Nano meter chip has huge technology problems, okay so what is the problem? 1 out of 1000 chips work then who will work for it, okay so the reliability is major worry so now everything is looked at Intel's chip what is called bore now bore is looking into it how to make reliable circuit 7 Nano meter circuits are available, okay not in market in the lab.

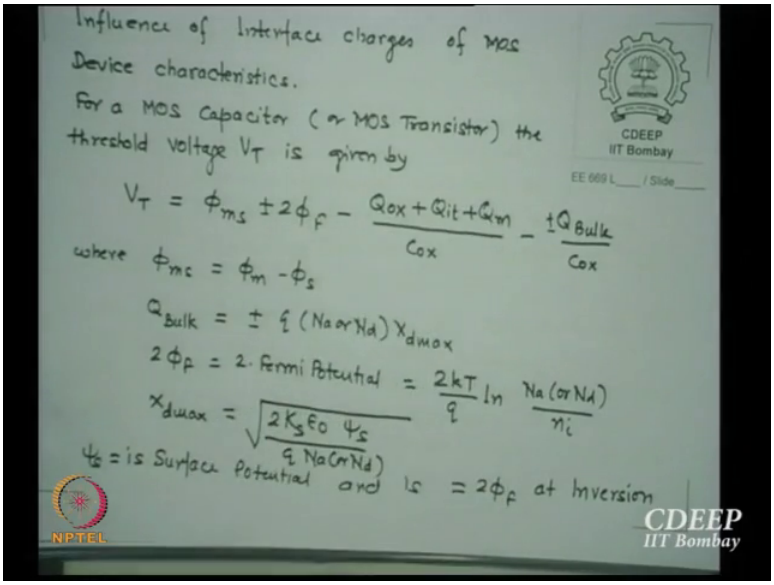
So this is what the process is so why process people become very strong because at the end of the day they only can solve the problems designers only will sit with the computer and sleep only and the process people will come and say, okay here is the model here is something now this is a device this is equivalent models start designing, that is good, okay. So I already said, okay so the as I keep saying dit is very very crucial for variety of reasons and one must somehow control them to around 10 to power 10 per centimeter square so that the effect of dit is minimized, okay I am not saying it will be 0 but will be minimized same as fix charges reduce this Q ox term which includes all of them as small as possible or Q ox by C ox term in nutshell then you will be able actually leave some hope for circuit to function, okay.

So all technology people should not feel you know that that is why some material people must be feeling bad that you know lot of circuit related things are told the reason is we are not material scientist we are VLSI technology people and for us circuit is the ultimate or system is the ultimate, “unko kya chahiye wo ham denge”, that is the way it is.

So process people should know what designers want or what device wants and we should be able to give that, okay. So if I keep correlations please take it because I work on every area or I do not work in any area now so because of that I can tell you where it hurts, okay. Typically (())(45:00) says 10 to power 20 per centimeter square, sorry per centimeter square and we want to reduce it to as low as 10 to power per centimeter square but as soon as you put silicon dioxide on silicon much of the oxygen will get bonded to silicon SiO Si bonds will be formed some which are not able to they are still dangling they are called interface states.

One of the technique is to pass chlorine during oxidation that is what we tried, okay so we say these bonds will be picked up by chlorine but chlorine itself has a problem so we left chlorine then we said, okay HCL may be more worrisome so use trichloroethane tca as it called then it has a carbon content there so it starts correlating there so in 70 it was very interesting technology anything you can try and you will get something funny, okay now many things known so not many achievements are in technology as in those days I dip in something and oh different oh great, okay now it is not so, okay is that okay?

(Refer Slide Time: 46:33)



So I am interested in dit for control on Vt and control on mobility and therefore I am worried, okay let us say now forget about all this Vt is fix charges interface charges and mobile charges all three are actually coming into Vt term, is that correct? So any one of them can hurt you, okay of course sodium can be easily removed much of it if you take super clean systems fix charges by technology by proper oxidation process you follow Q ox can be minimized there was a time when we worked in 80's when students of mine where working in lab so I use to do oxidation for most of my students in those days so many of my ph.D student used to say, sir let us do let me do I say okay do it then he used to measure Cv and he says my charges are 10 to power 11 and yours are 10 to power (())(47:28) you do the same thing which I do, I said that is my hand that is when I push something I myself do not know what I do but I push the rack in or push (())(47:38) out at what rate I do how long I wait there which zones is unknown to me, okay but my mind is set for that over the years I know what to do, okay.

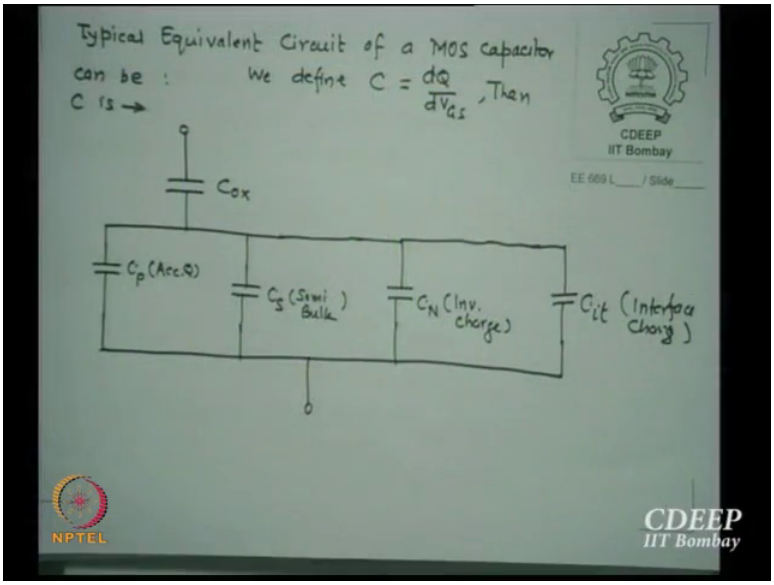
So even if you do 100 percent automations someone has to model this what I did so they photograph they do lot of enough imaging processing and then figure what exactly I was doing so then computer can be told do this motor control, okay. So all automation was done by actually monitoring what humans do, okay but humans are smarter they always do better than what machines can so again machines have to learn how much humans can learn, okay. So this statements are already made Fermi potential system twice kT by qna or (())(48:29) plus or minus if it is na by now it is plus if it is ni by ni by nd it is minus xd max is twice case epsilon not Si s

now Si s is called surface potential I will take the figure just now and that is equal to 2 phi f at inversion surface I will just draw the band diagram quickly and then we will show you (()) (48:50), is that okay?

So these are the expressions which last time also I gave I am just repeating this is (())(49:00) expression which worries us in our controls and therefore technologically if there is change in substrate doping variation can you think that since 2 phi will vary, this will vary so Vt will vary so it is not that whole wafer will have same Vt so there is a called Vt map we actually see how much Vt varied just because of the substrate concentration, so what should we do? We actually make wells as one well I should you other day in my this which diffusions are implants are fixed value for all regions since I can do much better control on by selective this I will be able to get more much more control on na or nd's, okay therefore all CMOS processors do not use substrates, okay they use prols and n wells to make n channel and p channel devices, is that clear to you?

So this any nd's are not no more control by actually controlling the Vt's it is the doping in the wells which we will do see later implants, okay.

(Refer Slide Time: 50:18)



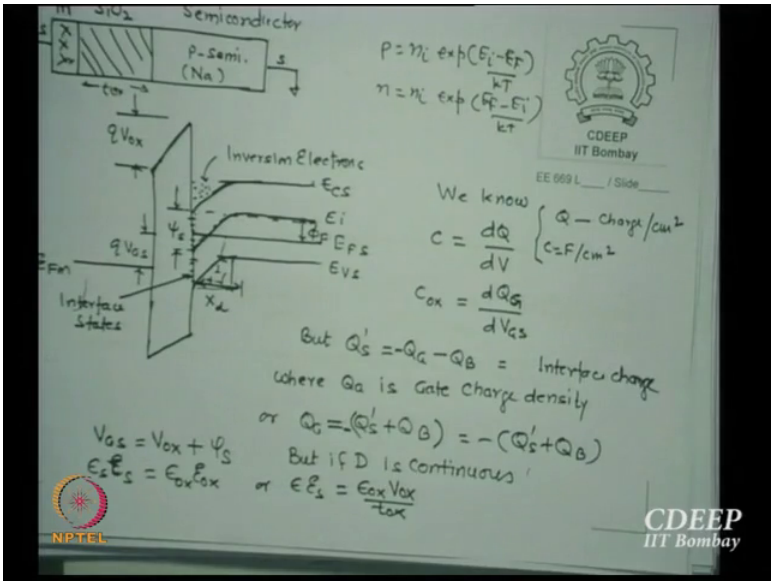
Before I start working again on this capacitance you can actually write note down this circuit this is called equivalent circuit of a mass capacitor some are important in some regions some are not important in some regions some are (())(50:29) in frequency tip downs so we will see what it is

but this is called that mass Cv so if you are really a mass capacitance man you should know how this (())(50:39) are different (())(50:41) this there is a Cp from this how p substrates so we says na's so Cp which is accumulation Cs is the depletion charge or capacitance due to that then there is an inversion in capacitance and there is a interface states capacitance, why we say this? Any charge variation with the voltage leads to capacitance Q is equal to Cv so dq by dv is C so if charge is varying with voltage there is an equivalent capacitance associated, is that clear? This is a basic theory which we use any change in charge with voltage leads to capacitance, is that clear?

So anywhere you see charge change of charge as you change voltage then you say there is a capacity effect coming in, okay. So this net capacitance is this C ox is always in series with this hole of there may not all four exist simultaneously but many of them may we will see what. So these are in parallel what do they mean? They add they all add whereas this is in series means they actually go harmonic way 1 upon C is equal to 1 upon C1 plus 1 upon C2, okay this semi (())(52:11) depletion, okay now the reason is this is taken from Shah's book he is defining C I mean many I have recently added but my way old sheets has ccs there so I wrote that but then I immediately remember make it bulk, okay.

There are 4, okay I will show you the circuit before we come to it we will show you, "ek minute ye alag alag region me equivalent capacitance itna rehta hai actually, okay". So we want to (()) (52:47) for each region what is the equivalent circuit or equivalent capacitance we get, okay this is what I am trying to do, okay. So and this is what I know all these capacitances adds to itself not necessarily present all of them, why? Because during accumulation there will not be any depletion you know so obviously both will not be there, okay.

(Refer Slide Time: 53:18)



So those people who do not like physics still I wish to know at least or those who like physics is better for them but those who do not like look at it anyway, this is a p semiconductor mass capacitor shown here typical oxide thickness is T ox have a p type semiconductor substrate has a doping of na and this is a metal plate so it is mos as we want this is the band diagram this silicon dioxide band gap this is the conduction band this is the balance band has a 8 electron volts band gap.

Now right now assume that the Fermi level in metal and Fermi level in semiconductors where align when they brought together, so phi ms is 0, okay we will add that term in case real life what will happen if I put that and I apply positive Vgs with reference to substrate which is grounded positive Vgs means what is energy associated with plus Vgs energy minus Qv, okay so energy is minus Qv so we wish if energy diagram shows upper energy increasing, which side is the energy going down? Going down.

So this Fermi level of this metal, what is the voltage we apply between the Fermi levels whatever potential we apply is the separation of the Fermi levels but the Fermi level will metal should go down because its energy is more negative then Fermi level in semiconductors so the difference between Efs and Efm is the applied potential Qvgs, okay Q because (())(55:07) voltage energy diagram otherwise difference of potential is Vgs.

Now please take from me that in all over band theories all mass capacitance theories (())(55:21) we do not do but in case of mass I always show Efs constant in pn junction I will actually say whenever the Fermi level bends I say current is flowing that is the word if there is a change in Fermi level with x d phi by dx then the current flows j is proportionally d phi by dx, okay. In this case the across oxide there is no current there is no DC current across the oxide so therefore Fermi level is semiconductor is held constant at 0 potential because you have grounded that such reference to that now we will measure all other potentials, is that clear to you?

So Fermi level in semiconductor is fixed but if it is a dope semiconductor then semiconductor to Evs balance band should be fixed because that is depending on the doping we use, okay. Ei minus Ei is called the mid band (())(56:25) level Ei minus Ef is how far the Fermi level is away from the mid band is the Fermi potential which is phi s so it is the phi f. Then if I apply initially Ef is equal to Efs the bands will be flat, is that correct? No bending but as soon as I apply Vgs this energy goes down, okay which means now applied positive charges at the metal, so what is that semiconductor charge should receive now? Negative charge so the first thing is holes move away if holes moves away, okay,"kisi ne agar pucha e by kt me e is q times the potential so q by kt is 25.8 millivolts at 300 degree so e energy voltage bohot chota rehta hai thousands me nahi ata hai 10 to power minus 19 ka multiply kiya aur k minus 23 hai toh value adjustable hojati hai, okay".

These are called (())(57:52) relation the holes are related to Ei minus Ef and electrons are also related Ef minus Ei. So we now say since Ei is above Ef holes are appearing Ei is away from Ef the hole this is the p type semiconductors so your holes in the conduction band balance band but as you apply plus Vgs and you expect whole concentration to leave surface where they will go because of the electric field holes will move away from the, sorry I am sorry since the electric field is opposite this side so holes will move away from this and will leave a depletion charge, okay will leave depletion charge, what is depletion charge? Minus Qna xd, okay.

These charges are essentially in this region so that band the band start bending down because holes are moving away Ei is coming closer to Ef if the hole concentration start reducing what will happen Ei will come closer to Ef Ei is the mid band so both Ec and Ev will also follow Ei, is that point clear? The balance band and conduction band are Ei is always 50 percent either side. So Ei bends Ec Ev also bends, okay. Now if Ei is equal to Ef what will happen? "Nahi

exponential 0" that is (())(59:39) if Ei is equal to Ef p and n equal to ni that is material becomes intrinsic.

However if Ei goes below Ef that is this become minus or Ef minus become this what is that Boltzmann relation is saying, electrons must appear that is the inversion as you start applying Vgs the band start bending as Ei is above Efs your holes concentration reducing but depletion layer is enhancing because accepters are opened as you further increase Vgs band further bend down to adjust to this Vgs as it bends down and touches Ei Efs then we say material has become intrinsic and if you further apply Vgs then Ei crosses Efs and you except electrons to come so this electrons start appearing in the conduction band, is that clear? They start appearing in the conduction band this is inversion but Ei when it starts becoming inversion when Ei just crosses Ef inversion sets in few electrons will come because we have just crossed Ei Efs.

However definition my threshold was that when this number of electrons bending is so much that the number of electrons here is same as number of accepters only then we say strong inversion is set in. If Si s is measure as the bending for Ei Si s is measured as surface potential so this is Q Si s Ei bend how much is Q Si s surface potential. So when the Si s then equal to please take it Si s is same as when Si s is 2 phi f 1 phi f here 1 phi f here, what does that mean? The concentration here and n are same as p if opposite now. So 2 phi f whenever surface potential becomes 2 phi f we have a strong inversion, okay is that clear to you?

This for a n channel device p channel device all (())(62:01) will go above and there is a interesting thing another thing before we (())(62:05) if this contains interface states where they will lie from conduction band to balance band there will be interface states at the interface. If I apply charge here now not only there will be charge in the semiconductor but there will be charge in the because some charge will be picked up by dangling, okay.

So we say there will be interface states will start uncovering themselves, okay so they will start sharing charge with metal charge whatever you expect some pat of the charge will now go to interface and rest of the charge will go to the semiconductor, so what will happen to Si s? Si s will not be able to bend as much for the same Vgs, is that correct to you? If there are no interface charge all Si s will be reflected by Vgs, okay increase this will bend but now there is additional mechanism which is changing with charge equations, is that clear? So what will happen? To

make strong inversion it may take longer voltage now, is that clear to you? So if the interface are larger some charge will be picked up by interface so you will require larger Vgs to attain to this Vt, is that clear to you?

So inversion which is 2 phi f in strong inversion case will appear now late, why? Because initial charge was picked up by interface state as well and you apply and it will start picking some charge in the interface some will go to semi-conductor that is Si s plus Si interface total will be the applied potential at the Efs minus this. So any Vgs change now is not directly going to the semiconductor but it is also shared with interface states so that is our worry that the Vt is varying as many states are here as many below the Fermi level as many above the Ei they are called donor states or accepted states and they will share the charge and if they share the charge the Vt will vary with Vgs, is that now clear why I am so much worried about this dit word because I see larger the dit larger sharing will (())(64:31) interface so my Vt will become even larger and which I do not want, why I am not interested in that? Vgs minus Vt is the proportionality for the current if Vt increases my current goes down my circuit fails so I am not interested, okay so I now tell the people,"kuch bhi karo Vit reduce karo kuch bhi karo" how do they do it it is a game it is not so easy it is not so difficult in technology there are good games played something you do and you get and then you are left to think how did you get next time you do you do not get then you are again left to think why you did not get, okay.

So is very interesting because I keep saying silicon behaves as it wants it does not behaves as you want, okay after many days your hand at least if not brain actually picks what silicon does, okay and it starts following it, okay that is interface so my hand start interfacing with the process and I know if I do this it will happen, okay that is why technology cannot be learnt on (())(65:44) it can only be learn in the lab, okay do whatever this is the only that is why I am facing so much on the (())(65:52) because that I can explain without going to the lab whereas actual technology I cannot tell you do this and many will tell you,"thoda ye karo hota nahi hai, kuch nahi hota hai balki jo bolra hai uska ulta hojayga because wo bhi guaranteed nahi hai na what we said and what you understood also is not same so".

So it may happen that you will get then you will do not say I did this and we say it cannot happen, no sir it happened this is result (())(66:23), oh is it then he will put another theory and another experiment so it keep interesting work going on, okay "jis din ye fix hogaya usdin

research khatam", so that is how we keep doing result because this and this does not match as long as it does not match we both are happy, "ek aur paper ek aur citation ek aur so jis din match hogaya fir kya khatam".

So anyway this is fun part in the course, okay. So now little quickly we go if you do not read this part right now you just look for this,"abhi hai aur pandra minute hai". Please if I increase Vgs opposite side what will happen? Efm will be above Efs and the band field bend which side then? Upwards because now I am applying minus Vgs and I expect positive charges so holes will come closer to so larger the Ei minus Ef larger will be number of holes so Ei should move away from Ef as much as so that larger number of holes are created, "so accumulation me kya hoga" bands will bend upwards, is that correct? But maximum how much they can go up to? Once the balance band touches Efs it cannot cross, is that correct? The balance band cannot Ef that is called (()) (67:56) once you reach d generate case Ef all carriers are possible only in the balance band and no more additions, okay.

So once (())(68:05) reaches nothing extra happens (())(68:09) bands can bend upwards to access hole please remember if Ei goes above Ei minus Ef becomes larger means holes become larger in accumulation you mean holes to the surface, is that clear to you? So in accumulation bands will bend upward in depletion bands start going down and one Ei cross Ef we say it is inversion initially till Si s is equal to phi f it is just at the age of inversion when Si s becomes equal to 2 phi f we say it is strong inversion and between Si s equal to phi f 2 phi f is called weak inversion, okay weak inversion, is that clear?

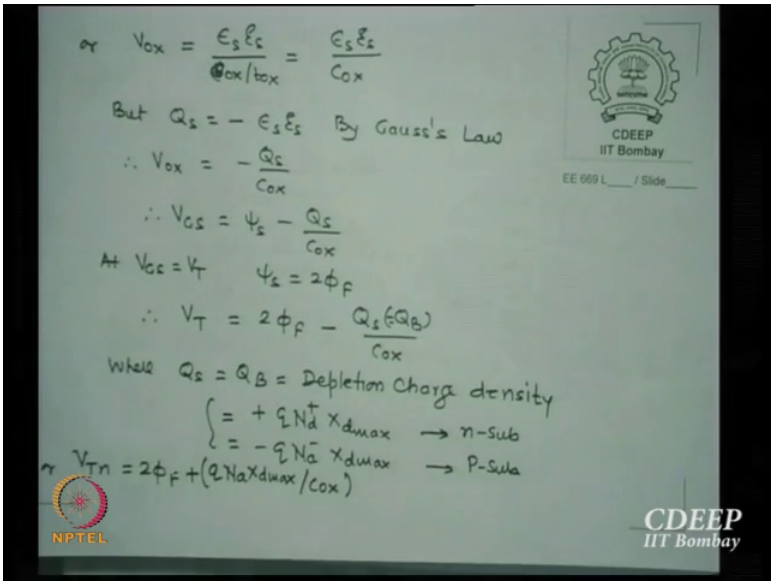
Is that now clear to you many peoples say that if you reduce Vgs below Vt the current still flows, is that clear? The reason is obvious you are in a weak inversion your cross 2 phi f above but you have not crossed Ei equal to Ef value so far so current still start moving and this called a leakage current simply because you are still in the weak inversion and weak inversion sub threshold currents will keep flowing, okay the problem with sub threshold for someone who there are two problems in sub threshold current one is power force the other major issues of threshold is in the design of (())(69:40) and now also in the nand flash, okay this sub threshold problem is a serious issue for nand circuits flash RAMs, ROMs and also in DRAM designs.

So all these technique why I am relating you every time because I do not want you to feel that,"me sirf ye apko kuch oxide karke dikha raha hu aisa nahi hai iska ek relation hai mere dimag me". So all of you should realize that all things which we do has one goal, "ek Pentium 4 se uper accha processor banana hai", okay why do we want to make better Pentium or better processor? To design another better processor, "wo generation hai, okay", there is nothing more to it, okay. If I apply Vgs you can see from here metal of course is a very good conductor so very low resistivity material so no drop we assume, so where the voltage will drop now? Partly in the oxide and partly in the semi-conductors, is that correct?

If I apply two resistor r1, r2 apply Vg part will go to r1, part will go to r2. So we say Vgs this part will go to Vx and part will go to any conductor Si s surface potential but this V ox I do not know the way I show V ox is the band bending of the oxide band is essentially the V ox but that I do not know how much, okay. So I must replace this V ox by some terms which I know, okay so that is a next thing which I want to do before I (())(71:20) is how do I replace Vgs term in terms of Si s plus some term which is not V ox but connected to the terms which I have I know about.

So I say from here as I just now said last time if the D vector is continuous, what is D vector? Electric intensity vector D epsilon E is continuous then epsilon is Es is epsilon ox E ox or epsilon of Cx is epsilon ox by T ox, what is the electric field in oxide? Vs divided by T ox so it is v ox divided by T ox, is that okay? Vgs is V ox plus Si s then use discontinuity epsilon S is Es is equal to epsilon ox V ox I write E ox as V ox by T ox so I get epsilon s that permittivity of semi-conductor into electric field in semi-conductor is permittivity of oxide divided by oxide thickness into voltage across oxide, okay.

(Refer Slide Time: 72:30)



Now from this equation I write oxide voltage is epsilon s Es upon epsilon ox by T ox this is epsilon which is essentially epsilon s Es by C ox, okay C ox is per unit area, okay however by Gauss's law epsilon s Es is how much? The semi-conductor charge density Qs this is Gauss's law, okay. So Qs is minus epsilon s Es this is how Gauss's law is defined, but how much is Qs how do I calculate semi-conductor charge? Qna Xd plus Q inversion I know charges in I know everything in semi-conductor but I do not know anything in oxide so I said, "fine, thik hai I replace V ox by charges in equivalent charges in semi-conductors so I write uses Gauss's law I write V ox is minus Qs by C ox, so what is Vgs now? Vgs is Si s minus Qs by C ox at inversion strong inversion Si s is 2 phi s so Vt is 2 phi f minus Qs by C ox where Qs is the bulk charge depletion before enumeration sets in strong inversion sets in which is Qnd xd max as n substrate minus Qna at p substrate.

So this relation which we earlier derived Vt is equal to 2 phi f minus Q by (())(74:11) what are the conditions we applied here in doing so, phi ms is 0 no work function difference and oxide charges are 0, is that clear? This is called ideal Cv this is called ideal Cv, okay from sorry from ideal Cv I will able to get Vt so anything additional term appears here from experimentally if I subtract this ideal that experiment the difference is what value I will get from that that is what my whole measurement technique is about, if there is additional Q by C ox something this theory I know, okay this values I know so I know my this value so I will actually see (())(75:00) see

how much shift it was from the ideal, okay the shift is whatever is the extra term is the shift from the ideal, is that clear?

So the first thing we plot in the Cv curve is ideal Cv then on the top we plot experimental Cv and the difference and there we will measure see that difference is the additional term appearing in this terminology, is that clear to you? So this expression Vgs Si s minus Q ox is the only expression I used in all my Cv measurements, okay all my Cv measurements, please remember that will give me all kinds of parameters which I am looking for mass system, okay I can measure phi ms also through that I can measure Q ox I can measure Qit different techniques there are 7 interface state measurement technique we will only show you what is most famous among them is called quasi static or (())(76:01) method there is a (())(76:02) there is a triangular sweep the conductance, (())(76:06) technique then there is a pure low frequency Cv's and there are dits there are n number of ways you can evaluate dit's, okay.

However we will only look into the simplest which is called quasi static very fast high frequency low frequency Cv anyway why we are not I am not so keep about getting exact value because exact value does not help me anyway I know how much maximum I need to get, okay I control only that even if it is 10 to power 11 I 2 into 10 to power 11, 10 to power is same for me how much one order I have to reduce, okay. So I am so keen in places to know exact value, "per aur kisi course me aisa mat kehna" because there actually 1.875 into 10 to power they will ask you this, okay so do not put it 2 into 10 to power 10 there put 1.8796 "job hi calculator dikhata hai likhna wo bohot khush hote hai" in real life it does not matter, okay.

So next time I will use this give the Cv techniques faster Cv techniques and we will finish.