# **Power Electronics**

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## Lecture No - 9

Hello, in my last class we discussed the operation of power MOSFET, metal oxide semiconductor field effect transistor. It is a very fast device, much faster than a BJT. There are 3 terminals similar to our BJT. They are drain, gate and source. Gate is insulated from the source. There is a  $SiO_2$  layer which is an insulator. So, the input impedance or the impedance between gate and source is very high and it is mainly a capacitor. So, how does a current flow from drain to source? When the applied voltage between gate to source is higher than what is known as threshold value, N channel is formed and which connects the drain to source.

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See in this figure, when the applied voltage is higher than the threshold value, N, a small channel is, conducting channel is formed below the silicon layer. So, electrons starts flowing from this N plus layer to N minus layer in this fashion or the current starts from drain to source.

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So, in the conduction mode, the on state voltage drop across the MOS is slightly higher than a BJT. So, in the linear zone, in the sense, in the ohmic zone, I can represent MOS as a resistive element. Just see the characteristics, they are almost linear. So, for the same collector current or for the same drain current, see the characteristics of a BJT and a MOS. See, I have plotted these characteristics for  $V_{DS}$  or  $V_{CE}$ , collector current or drain current, I kept I<sub>B</sub> constant. Here, gate to source voltage is held constant. See the characteristics, this is for a MOS, this is for BJT.

So, the equivalent resistance in this case is much smaller compared to a MOS. So, on state power loss in a MOS is slightly higher than a BJT and this is one of the drawbacks of a MOSFET. Another point that I discussed was that the capacitance between gate and source remains almost constant whereas, the capacitance between gate and drain varies with  $V_{DS}$ . So, this capacitance is high when  $V_{DS}$  is low. In other words, when MOSFET is on, at that time  $V_{DS}$  is low, capacitance between the gate and the drain is high and this capacitance decreases as the voltage between the drain and source increases.

A BJT is a minority carrier device, whereas, a MOSFET is a majority carrier device. The current flow in the device is only due to the electrons. It has a positive temperature coefficient and therefore paralleling is easy. About the safe operating area in a BJT, there are 4 zones, whereas in a MOSFET there are only 3 zones.

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See here,  $I_D$  limit, maximum power dissipation limit and CD is the  $V_{DS}$  limit. There is no secondary break down limit as in the case of BJT.

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Now, let us see the variation of  $V_{GS}$ , is a function of charge carried to the gate. OA is corresponding to the charging of the input capacitance  $C_i$  under full  $V_{DS}$ . See,  $V_{GS}$  is very low, less than the threshold value then there is no flow of current. When there is no flow of current,  $V_{DS}$  is very high. So, OA corresponding to charging of input capacitance  $C_i$  under full  $V_{DS}$ .  $V_{DS}$  is high, therefore, gate to drain capacitance is very low.

So,  $C_i$ , the input capacitance which is equal to  $C_{GS}$  plus  $C_{GD}$ , now  $C_{GD}$  is very low, therefore,  $C_i$  is approximately equal to  $C_{GS}$ , a capacitance between gate and source.

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Now, AB, What is AB? AB is it corresponds to  $V_{DS}$  decrease from the supply voltage to  $V_{DS (ON)}$ . Once, the applied voltage between the gate and the source is higher than the threshold, flow of electrons starts. So, current starts flowing from drain to source,  $V_{DS}$  falls. So, that region corresponds to AB, see AB.  $V_{GS}$ , voltage between gate and source remains constant and the charge supplied is used to vary the voltage across  $C_{GD}$ , gate to drain. Now, I told you, see the voltage is falling from the full voltage, full rated voltage to DS on. So, as the voltage falls from the full voltage to the on state voltage,  $C_{GD}$  goes on increasing.

So, whatever the charge that is supplied is used to charge the capacitor and this BC corresponds to the input capacitance charge when the device is on. Now, what is the input capacitance when the device is on? It is  $C_{GS}$  plus  $C_{GD (ON)}$ . During on,  $C_{GD}$  is high. So, this is corresponding to a device on ...

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Similarly, the change in voltage with the charge or during turn off, E to F for the removal of excess charge, F to H is corresponding to discharge of  $C_{GD}$ . You are turning off the device. Voltage across the MOS is increasing. In other words,  $V_{DS}$  is increasing. So, this is corresponding to the discharge of  $C_{GD}$  and  $H_J$  is corresponding to the discharge during current fall,  $C_{GS}$  discharge. See, these wave forms we require while designing or while studying the turn on and turn off of MOS. So, I will just show you how power MOS IRF640 is mounted on a heat sink.

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See, the parameters. This data I got it from their site.  $I_D$  at 25 degrees, continuous drain current  $V_{GS}$  is 10 volts, maximum is 18 amperes, gate to source is plus or minus 20 volts. See here,  $R_{DS(ON)}$  is 0.18 ohm, it is mentioned here very clearly.



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The other voltage or the parameters, gate to source threshold voltage, see, minimum is 2 volts, maximum is 4 volts. Gate to source charge  $Q_{GS}$ , 13 nano coulombs, turn on delay, that is 14 nano seconds, rise time 51 nano seconds, turn off delay 45 nano seconds, fall time 36 nano seconds. I will explain to you what exactly this means. They are almost similar to BJT. See, just now I showed you the variation of  $V_{GS}$  with Q, total gate charge. See the variation and this is the variation of the capacitance.

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Now, the switching characteristics, if you know how exactly  $V_{GS}$  varies with Q, understanding the switching characteristics becomes very simple. See, the variation of  $V_{GS}$  is shown here. I have not shown you the variation of drain current because it depends on the external circuit. I have just shown the steady state current here.

Gate to source voltage, it starts from zero, is increasing. Till it is the threshold value, there is no conduction,  $V_{DS}$  is still high. All the charge or all the current that is supplied is used to charge the gate to source capacitance. This region, whatever the charge that is supplied, it is used to charge the capacitor between gate to drain.

 $V_{GS}$  remains constant here and  $V_{DS}$  falls to a very low value and when  $V_{DS}$  is very low, the capacitance between gate and drain is very high and this is the same, the variation is same as what we seen before. See, after sometime device is turned off. Same, there is a delay time, after sometime current starts falling and this is the fall time,  $t_f$ . Again I have not shown the rise in the drain voltage because it depends on the external circuit. So, this wave form is same as the previous one. See here, on and this is off.

Now, what are the major differences between a BJT and a MOSFET? So, let me summarize. BJT is a current controlled device, MOSFET is a voltage controlled device. BJT is a minority carrier device, therefore, it has a negative resistance coefficient, therefore, paralleling is difficult.

What about MOS? It is a majority carrier device, has a positive resistant coefficient, therefore, paralleling is easy. BJT has a secondary breakdown because it is a minority carrier device, negative resistance coefficient. MOSFET is a majority carrier device. So, there is no secondary breakdown. On state power loss in a BJT is low that is  $V_c$  sat into  $I_c$  is low. Power MOS, it is  $I_D$  squared into  $R_{DS}$  (ON) is higher than the on state losses of a BJT. Turn off time of a BJT is generally higher because of the storage time. MOSFET is a very fast device.

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So see, here are the major differences between a BJT and a MOSFET that I have summarized. It looks like, exact for on state voltage drop or on state power loss, MOSFET has an edge over the BJT.

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So, BJT has an excellent on state characteristics. The problem with that is a current controlled device. So, if you compare BJT and a MOSFET, they almost complement each other. Input power requirement for a MOSFET is very low, BJT has higher. It is a current controlled device. I told you that a small PT is required to drive another PT, power transistor.

Now, can we combine this both the devices, the advantages of both the devices and come out with the new device, what is known as IGBT. See here, insulated gate bipolar transistor, IGBT. It was developed in 1983 by Jayant Baliga, very popular device in power electronics, very popular. Prior to the advent of IGBT, BJT was used. It was very popular, may be till the 1990's or so, BJT is very popular. As IGBT started coming to the market, the popularity of the BJT started coming down. So, what is this IGBT? Insulated gate: almost same as the MOS. There is a SiO<sub>2</sub> layer, bi polar transistor, output is a BJT.

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Modify the structure	2		
P° layer forms the o	train.		
When +ve potentia	applied to	the gate	
& exceeds thresho	ld voltage	Source	Gate
n channel is forme	d → similar		
to MOS		6	5
⇒ Electron flow into	N' region	P*	
N <sup>-</sup> layer receives e	lectrons from	n	
source (N") & holes	from drain	(P*) *	

So, see this structure, almost the same as the MOS here, almost the same. You just added a P layer, a P plus layer and that forms the drain. So this layer, above this same as MOS, you have just added p plus layer, that forms the drain. Operation at the input stage is the same when the applied voltage between the gate and source is higher than the threshold value, N channel is formed, N channel is formed here.

So, electrons starts flowing form N plus to N minus region. When the positive voltage is applied to the drain and the source between drain and the source, this junction is forward biased and therefore, holes are injected into N minus zone. See, this was not there in the MOS. MOS, the flow of current only due to flow of electron. Whereas, here you have here input stage similar to a MOS, flow of electrons from N plus to N minus. Similarly, holes from P plus to N minus.

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So, what happens? Some electrons recombined with holes and remaining holes are collected at the sources. Now, having this P plus layer, what have we achieved? Now, this junction in principal can block a negative voltage. I will explain it sometime later, what exactly we need to do for IGBT to block a negative voltage.

Now, there is a P plus and N plus. So, in principal, it can block a negative voltage. What is the magnitude of negative voltage it can block? I will tell you some time later. See, you can observe one more thing, see, there was an anti parallel body diode in a MOS, this is this diode. Now, that diode is absent in IGBT. But then almost all the IGBT, they do have an inverse diode.

Now, this inverse diode is built in which is optimized to match the IGBT switching operation, almost similar to a MOS. MOS had a body diode but then we disabled it and separate a diode which was optimize to match the MOS characteristics, the switching characteristics was build in, whereas, IGBT does not have the body diode. In the later half of the course, we will find that this diode is required.

So in the market, most of the IGBT's, they do have an inverse diode and this is built in, whereas, in a MOS, it was inherently present. So, that is the difference.

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Now, coming to the VI characteristics, how do they look? They look similar to BJT. Only thing is, control parameter is gate to source voltage, almost similar to a BJT, a steep rise. So, during conduction  $R_{DS}$  is lower,  $R_{DS (ON)}$  is lower, I told you. See here, I just redrawn them, drain current verses  $V_{DS}$  for a MOS, for an IGBT.



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So,  $R_{DS (ON)}$  for IGBT is less compared to MOS. What is the reason? The reason for having low  $R_{DS (ON)}$  in the case of IGBT, I will tell you some time later. One more thing that had to be observed from the structure, see here, we had a drain which is P plus and N plus and N minus.

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Do we need to have these 2 N layers? What if there is no N plus layer? What will happen? The operation of IGBT will not get effected because there is N minus layer always there. But then, it will make a significant difference in reverse voltage blockage capability of the IGBT. If P plus and N plus are present, like, what I showed you in the beginning, both are heavily doped and when it is reverse biased or in other words, when I am connecting negative terminal to drain, the positive to source,  $J_1$  should block the negative voltage.

Now since, both of them are heavily doped, negative blocking voltage capability of this sort of a IGBT is low. The IGBT which has P plus N plus N minus layer is also known as punch through IGBT.

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See here, N plus layer between P plus and N minus drift layer is not essential for operation of IGBT. If both are present, in fact, if N plus layer and N minus layer, both of them are there, it is known as the punch through IGBT. So therefore, the punch through IGBT cannot block a very high negative voltage. It can block a very small negative voltage because both P plus and N plus which are adjacent, which form  $J_1$  junction, it has a very low reverse voltage blocking capability.

So, punch through IGBT has a low negative voltage blocking capability. So therefore, this is also known as non symmetrical IGBT, positive voltage blocking capability which is not equal to negative voltage blocking capability. Whereas, a non punch through IGBT, see the structure, it is P plus and N minus, non punch through, P plus and N minus structure. Now, this junction can block a high negative voltage because we have a lightly doped N junction or N layer. So, non punch through IGBT can block a high negative voltage. Therefore, it is also known as symmetrical IGBT.

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So, the structure of punch through, PT stands for punch through, looks like this. See here, P plus N plus N minus and again, now if I have only P plus, this is known as non punch through IGBT. This can block the negative voltage. This junction can block negative voltage, whereas this junction block can block a very small negative voltage. Hence, this is asymmetrical or non symmetrical, this is symmetrical IGBT. There are other differences also in punch through and non punch through IGBT's. I will tell you some time later.

Now, coming to the turn on and turn off of IGBT, the turn on of IGBT is approximately the same as that of a power MOS. The rate at which you charge the input capacitance or the rate at which you charge the gate to source capacitance, determine the turn on time. How about the turn off? MOS, there is only the majority carriers, there are no minority carriers. How about in IGBT? There was the MOS operation and there is or the flow of electrons from N plus to N minus. There is also a flow of holes from P plus to N minus. So, there are majority carriers, there are minority carriers also. So, in the turn off of the IGBT, there are 2 distinct intervals. What are they? I will show you.

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See this figure, the voltage variation of gate to source, same as that of a power MOS. The drain current starts falling very rapidly because at this point the channel that is formed between the drain and the source has disappeared.

So, MOSFET blocks quickly. I told you MOSFET is a very fast device, the moment the voltage between the gate and the source is less than the threshold, the channel disappears. MOSFET blocks quickly,  $I_D$  drops. This current, MOSFET current has dropped but then there are still minority carriers in N minus layer. There are minority carriers in N minus layer. They will take or they will take a longer time to recombine.

So therefore,  $I_{D}$  the drain current now falls relatively slowly. See the slope, there was a rapid flow of drain current. This is the MOSFET current and this is the BJT current. Because of the minority carriers in N minus layer and this current falls gradually what is something known as the tail current, almost all the minority carriers. Say, BJT that was the tail current, GTO is a tail current, even IGBT as a tail current. Why? because of the minority carriers, the holes in N minus layer.

So, we will see how to reduce the tail current, sometime later. So, I am not shown you the voltage variation,  $V_{DS}$ . It starts increasing somewhere at this point. So, during tail current period, even in the GTO or a BJT also, there was a high turn of power loss. Because, the voltage across drain to source as certain a reasonably a high value.

So, turn off losses will be high. How do you reduce this turn off losses or how do you reduce the tail current period or how do you make this tail current to fall rapidly? What did we do in GTO? We used anode short structure, that N plus layer in P layer which form the anode. By having that structure, GTO cannot block a negative voltage but then with N plus layer, it accelerated the recombination of the charges in N minus layer. This I told you while discussing a GTO.

So, if I compare a non punch through IGBT and a punch through IGBT, a punch through IGBT has N plus layer. So, compared to a non punch through IGBT, a punch through IGBT has a smaller tail current, almost similar to a GTO there.

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See here, we have N plus and N minus in punch through. So, this IGBT has a smaller tail current time. Now, it may not block a negative voltage. So, this is the price that you pay. Now, what about safe operating area for IGBT?

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It is the same as that of MOSFET. There are only 3 zones:  $I_{D,} T_{J max}$  and CD limit. There is no secondary break down zone as in the case of IGBT. So, IGBT is a device which has almost all the good qualities of BJT as well as a MOS, except the increase in turn of time. Now, because of the minority carriers, turn off is not as fast as a MOS. So, that is about the IGBT.

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I will just show you a module, a 75 ampere, 1200 volts dual IGBT. Dual, I mean, there are 2 IGBT's and this is a diode connected across it. The switching time of this diode is comparable with the IGBT itself. This is not a body diode, unlike in a MOS, remember. So, these 3 terminals are correspond to 1 2 3 and these 2, 1 and 2, 1 and 2, the control terminals, gate and source, gate and source. A common heat sink can mount on, a 75 ampere, 1200 volts IGBT.

This IGBT does require a driver circuit and that driver circuit should have the protection circuit also. Say, 1 way to protect a BJT from over current protection, I discussed in my last class. So, driver circuit also should have, in a BJT, it should able to supply a high current during starting. So, you require a separate driver circuit to control the IGBT.

There are something known as smart power modules. What are they? That module has the power module, the power devices plus the driver circuit plus the protection circuit, everything is built in. You do not need to use the discrete components to make a driver circuit and the protection circuit. Everything is built in, in the smart power modules. The protections like, over temperature protection, over current protection, over voltage protection, all these protections are built in, inside the module. So, just imagine or just think the reduction in the size that is possible using smart power modules.

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Smart power module or intelligent power module, these are the power terminals and these are the control terminals, control pins.

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And, this is for the heat sink module. What this intelligent power pack consists? See, I will show you.

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See, there are 3 legs, 1, 2 and 3. Each leg consists of 2 IGBTs and 2 diodes. Each IGBT rating is 75 ampere, 1200 volts plus the driver circuit for all 6 IGBT's, the protection circuit, over current protection, over temperature protection, over voltage protection. Just see the reduction in size that can be achieved by using the smart power module. It has 3 such modules. These are just the power module. It requires additional driver circuit and the protection circuit. Everything is built in this power pack.

So, these power modules, power packs, intelligent power packs are increasingly being used in modern power electronic equipments and that has resulted in a significant reduction in size of the power electronic equipment. So, one of the reasons for the progress in power electronics is due to the progress in power semi conductor technology. It is the heart and soul of power electronic equipment. So, with that I have come to an end of power semiconductors chapter.

What are the various power semiconductor devices that we discussed so for? Diodes, there are 2 types which are being used in power electronic equipment. One is rectifier diode, other one is a fast recovery diode; Rectifier diodes, where the frequency of operation is low and for high frequency application fast recovery diodes are being used.

It is an uncontrolled switch, a SCR and TRIAC, semi controlled switches. Why they can be turned on by applying a control signal? At the gate, having turned on the device, you cannot turn it off by applying a control signal at the gate. SCR has almost all the qualities of an ideal switch except that it cannot be turned off using a gate and it can block a negative voltage. A track which is nothing but or which is functionally equal to 2 thyristors connected back to back which is used in fan regulators.

Then we studied a GTO, gate turn off thyristor. So, it is possible to turn off a GTO by applying a control signal at the gate though the gain or the current, the gate current required to turn off GTO is high. A GTO is a high current device. There are again 2 types we studied. A symmetrical GTO

which can block both positive as well as negative voltage but then it has a longer tail current duration. To fasten the turn off process, we modified the structure what is known as the anode short structure. It cannot block the negative voltage. Then we studied BJT, bipolar junction transistor. It can block only positive voltage, it cannot block negative voltage because base emitter junction is heavily doped.

It is a current controlled device. The problem with power transistor is gain is low. But then, as the voltage rating increases and more over these transistors are operated in saturation, gain still falls. So therefore, we require a small power transistor to drive another high current power transistor. It has an excellent on state characteristics.  $V_c$  sat into  $I_c$  is very small. Then we discussed a MOSFET, ideal gate characteristics, in the sense, input power at the gate is approximately 0. Input impedance is very high, very fast device and majority carrier device, positive resistance coefficient, paralleling is very easy, no secondary break down but has one limitation.

What is that? On state power loss is high. Then we studied an IGBT. It is the device, has characteristics of MOS as well as a BJT. Input is a MOS, the power stage is a BJT. Gate power requirement is very small. But then, the turn off time of an IGBT is slightly higher compared to that of a MOS. That is because there are both majority as well as minority carriers.

So, this turn off time can be reduced by using a punch through IGBT. But then it cannot block a negative voltage. In non punch through IGBT, it can block a negative voltage. So, there are very few devices, it can block the negative voltage; a SCR, a symmetrical GTO and IGBT. Other devices cannot block a negative voltage. So, that is about power semiconductor devices.

From next class onwards, I will discuss the various power electronic circuits. The power semiconductor devices are used as switches and in our entire analysis, we will assume that these devices are ideal. We need to know the 2 basic laws to understand power electronics. They are; Kirchhoff's current law and Kirchhoff's voltage law.

So, we will start the course assuming that you all know these 2 laws. It is going to be very simple. I will keep the mathematical content to a very low value. I will use the graphical approach, mathematical approach is very important. So, if there is a circuit, you can always write a differential equation and you can solve. I will not take that route.

I will take the graphical approach, I will draw the wave form and I will use the basic properties limit of the various passive components, I will use the basic that is L and C. Average voltage across inductor should be 0, the average value of the current flowing through the capacitor is 0 at steady state. These are concepts that we will be using. So with that, I will conclude my today's lecture. From next lecture, I will start the power electronic circuits.

Thank you.