Power Electronics

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Lecture No - 8

Hello, in my last class we discussed the operation of bipolar junction transistor, a SCR, a TRIAC and a GTO, they are latching devices. The continuous gate drive is not required during on period whereas, a BJT requires a continuous based drive during the on time and in order to reduce the turn on time which is the sum of delay time plus the rise time, a high value of I_{BS} recommended and as the transistor turned on, in the sense after the t_{on}, this I_B is reduced automatically. See the wave form, looks something like this.

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A high value of I_B during on time after that it has reduced and this value is approximately 1.5 times this and second point that we discussed was a BJT should not be operated in saturation because if you operate in saturation, V_c may be very low but then the storage time increases and therefore, the total time required to turn off the device also increases and that limits the frequency of operations.

So therefore, the BJT is invariably operated in quasi saturation region. By operating the device in quasi saturation region, there will be a slight increase in V_{CE} and therefore device on straight

losses but then there is a significant reduction in the storage time and another point that we made was that if the transistor is operated in saturation, while turning off a high value of minus I_B should not be applied to the base. It should be a gradual increase towards minus I_B, something like this.

A positive I_B to minus, negative I_B, it should be gradual. How do I show the transistor always operates in quasi saturation region? Because load on the transistor can vary, load is invariably an independent variable whereas, the base drive is designed in such a way that the required current flows into the base for the rated current. Now, if the load on the transistor reduces, transistor may operate in saturation. So, how will you ensure the transistor always operates in quasi saturation Region? Using a Backer clamp it can be ensured that transistor always operates in quasi saturation region. So, this is the Backer clamp, by connecting a suitable number of diodes in series with $D_2 D_3$, you can clamp B_{CE} to a required value.

This D_1 generally operates like a control wall. It is because, see, V_C is trying to fall, in the sense, during saturation, V_C decreases. The moment V_C decreases below a certain value, D_1 turns on and when D_1 turns on, a part of I_B gets diverted. So, there is a reduction in the current flowing into the base. Now, as V_{CE} increases, D_1 turns off. So therefore, all the base current or I_B starts flowing into the base. So, D_1 functions like a control valve. It opens when this voltage falls below a certain value and it closes when this voltage increases.

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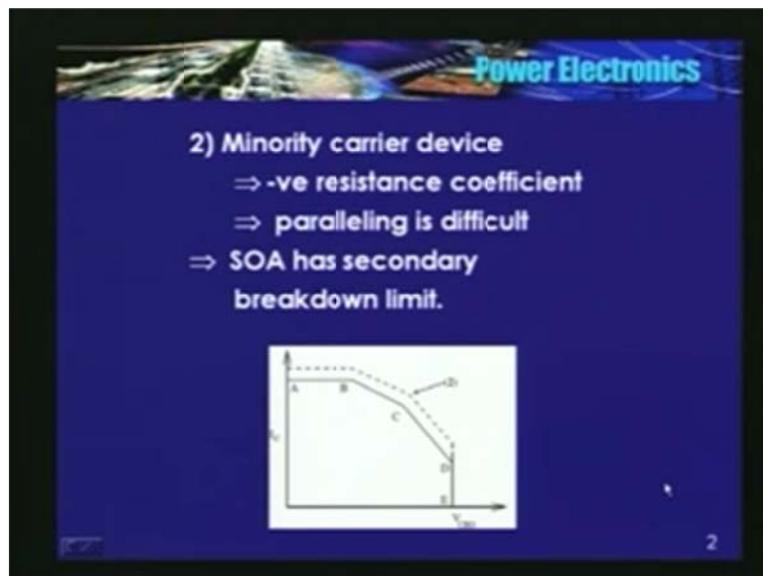
What is the other point that we discussed? Transistor is a minority carrier device. It has a negative resistance coefficient and therefore a paralleling is difficult and the safe operating area has a limit. This is governed by the secondary break down. See here, AB is the maximum current it can carry, BC is the maximum power that it can dissipate, CD is due to the secondary break down and DE is a maximum voltage it can withstand and I told you that if the transistor is on for a very short duration, the boundary of SOA expands, see, dotted line for a very low, a very short on time.

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I said BJT requires continuous base drive. In SCR, we had used a pulse transformer to isolate the control circuit from power circuit. SCR requires a just a sharp pulse but then we fed a large number of high frequency pulses and we used a pulse transformer to isolate them. Now, I told you that pulse transformer was like a differentiator because if I give a broad pulse to the primary of the pulse transformer, I will get a sharp pulse at the rising edge and another pulse at the falling edge because in this region a transformer may get saturated and if it gets saturated there is no voltage at the secondary. But then, this pulse may be sufficient to trigger a thyristor. Since, as the latching device, it do not require a continuous pulses.

BJT requires continuous gate drive and again there has to be an isolation between power circuit and control circuit. Now, which device shall we use? We can use what is known as an opto isolator. Opto isolator, see it is here, this dotted line (Refer Slide Time: 9:32) or whatever there is inside the dotted line is an opto isolator.

A diode may be a photo diode or some, when it is on, this transistor turns on. So, this is the control circuit, this side is the control circuit wherein, this side is the power circuit to the gate drive circuit and to the base. Now, as long as this diode is on, this transistor also is on. But then, what is the disadvantage? The moment I use a transistor, you require a biasing voltage, V_{CC} you require, a supply voltage you require, wherein this V_{CC} is not required in the case of a SCR.

Now, if there are large number of transistors in that circuit, your entire gate drive circuit may become bulky because as the number of opto couplers increases and each opto coupler, the secondary stage requires a supply. So, the overall ... circuit may become bulky.

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I will just show you the characteristics of a BU208D transistor, it was quite popular, you mean in 1990's or so. See the rating, V_{CEO} is 700 volts. See V_{EBO}, base emitter voltage is 10 volts whereas, V_{CEO} is 700 volts, collector current, 8 amperes and peak collector current is 15 amperes, may be for a very short duration.

I said base emitter junction in a BJT is highly doped. So, it cannot withstand reverse voltage. See, in the forward direction, it can withstand 700 volts whereas, in the reverse direction it can withstand a very low voltage because base emitter junction is very highly doped. See, V_C is sat, on straight collector emitter saturation voltage for I_C is equal to 4.5 amperes and base current of 2 amperes, it could be 1 volt.

So, the power losses V_{CE} is 1 into I_C 4.5 watts and some typical values of storage time, T_S and fall time, see, storage time is of the order of 7 micro second and fall time is of the order of 550 nano seconds.

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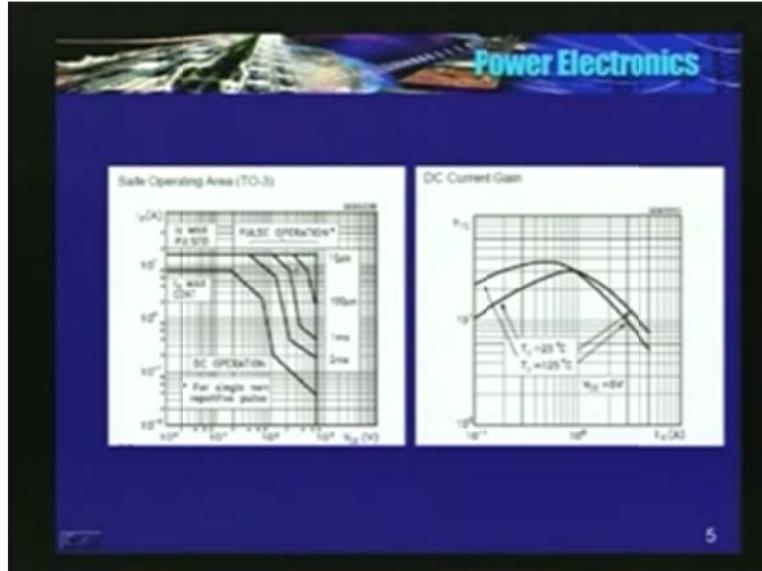
See, the safe operating area, I_C limit, power dissipation limit. See, this is for continuous and for very short duration the value increases and see the current gain, again it is not constant. It is a function of collector current and again the function of junction temperature also. So, at 25 degrees junction temperature, the variation is something like this and for 125 degrees.

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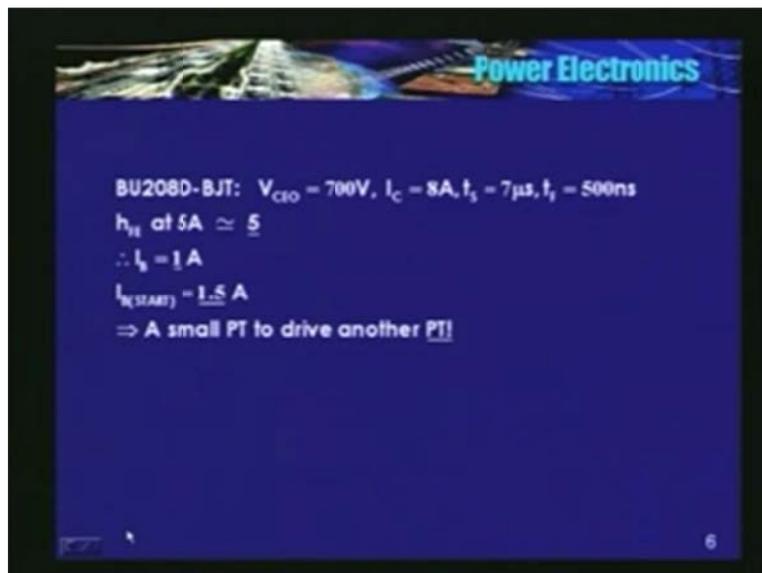
So, what is the problem with the bipolar junction transistor? Take for example, the transistor that I showed you just now, BU208D. V_{CEO} is of the order of 700 volts, I_C around 8 amperes and at 5 amperes HFV, the gain is 5 approximately. So, how much of base current that you require? It is 1 ampere.

Now, I told you that in order to reduce that on time, we have to supply a higher value of I_B. So, the base current during starting could be of the order of say 1.5 amperes. Now, this 1.5 amperes current, definitely TTL circuits cannot supply. So definitely, you need to use a small power transistor to supply a BU50 or BU208D transistor.

I will repeat, see, base current is of the order of 1.5 amperes. Now, which device can supply this much of current? Definitely, I need to use a small power transistor to drive a BU208D. So see just, that is what I made a sentence here, a small PT, a power transistor to drive another power transistor.

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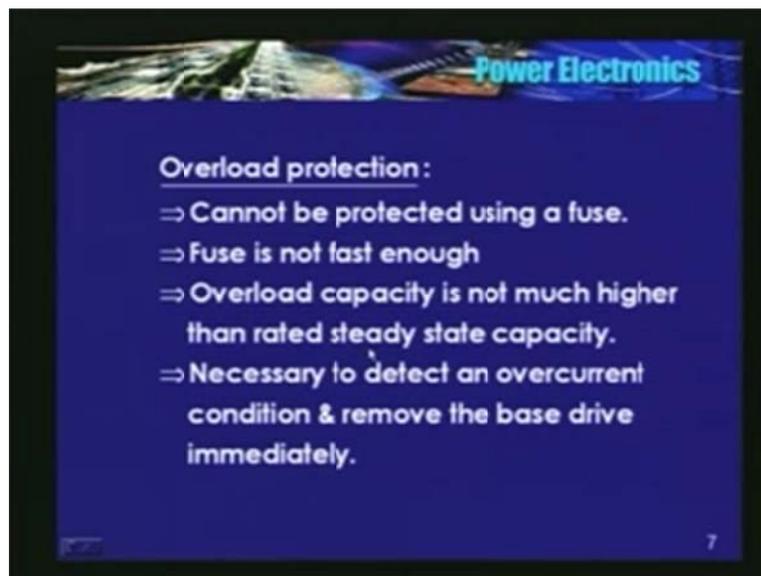
How do I protect the BJT from over load? How do we protect the equipments from over load, the electrical equipments? We use a fuse but then this fuse cannot protect the power semi conductor devices, these are not fast enough. Invariably, all most all the electro mechanical equipments, they have a higher over load capacity. Take for example induction machine, when you directly start online, it can carry 6 times the rated current. Say, BU208D transistor that I showed you just now, maximum current rating was, see, collector current value is 8 amperes and peak is for 15 amperes, you search for a very short duration.

So definitely, fuse cannot be used to protect a BJT and the over load capacity is not much higher than the rated steady state capacity. So therefore, it is necessary to detect an over current and remove the base drive immediately. So, the moment an over load situation is detected, transistor should be turned off. So, I have written here, it is necessary to detect an over current condition and remove the base drive immediately. Why? They do not have a higher over load capacity. It is not much higher than the rated steady state capacity. Now, how will you incorporate this?
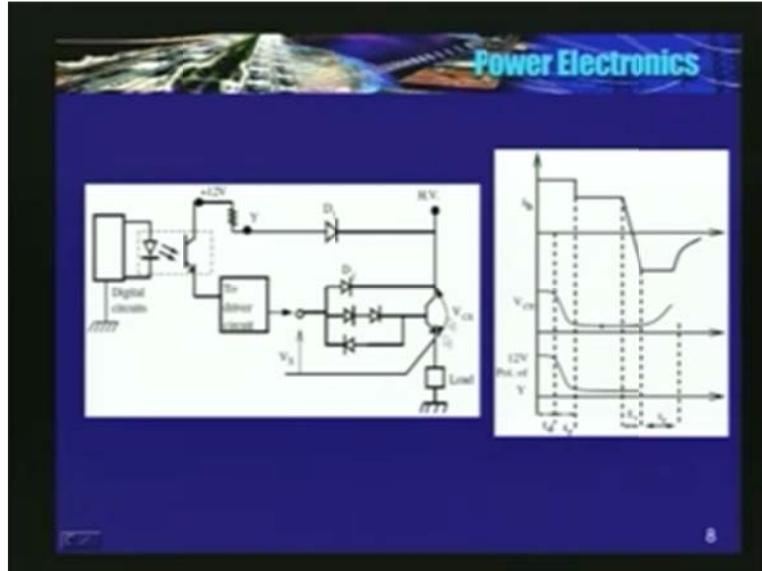
See, I have just shown a typical gate drive circuit. I have not given you the details, a Becker clamp which ensures the transistor always operates in quasi saturator region or at the required value, V_C is maintained at a required value, here are the digital circuits which generates the switching logic or switching signals to the transistor. Now, you need to isolate them. So, we have to use an opto isolator.

Assume that this power transistor is supplying a load and I have connected that load in the emitter, reasonably high voltage that depending upon the load requirement is connected to the collector and V_C should able to withstand this high voltage. So, here is a driver circuit. So, when the transistor is to be turned on, this diode turns on and therefore the transistor which is there in the opto isolator, turns on and this driver circuit supplies a positive I_B to the gate and I have used a plus 12 volts supply of this driver circuit. You may require a minus 12 also. I have not given you the all the details of the driver circuit, I just want to tell you how a BJT can be protected from overload condition.

This is the required I_B that is supplied to the gate and V_{CE} falls, Vc attains, Vc is the required value at, say, T_D plus T_R or after t_{on} time. Now, how do I protect the BJT from overload condition or in other words how do I detect the over load condition? During overload condition, the collector current increases, collector current increases above the rated value. So, what happens? Transistor starts operating or getting into active region. It tries to come out of saturation now because I_B that is flowing that is for a rated current. Now, current is higher than the rated.

So, as the transistor comes out of quasi saturation, V_{CE} increases. The Vce is high when the transistor is in blocking mode. V_{CE} falls to a very low value when the device is turned on and in the on period, it continues to remain at a very low value and in case if there is an overload, V_{CE} starts increasing and this situation or this condition should be detected and immediately transistor should be turned off.

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Now, how do you detect this overload condition? That can be detected by monitoring the potential at point y. The potential of point y when this diode is conducting is V_{CE} plus this drop. I will repeat, potential of y is V_{CE} plus the drop across dy that is when dy is conducting and what is V_{CE} when the device is on? It is Vx minus V_{D1}. So in case, potential of y increases above this value that V_{CE} plus V dy where Vce is Vx minus V_{D1}. It indicates that it is a fault condition or is an overload condition.

See, when the diode is off, what is the potential of Y? Potential of the Y is 12 volts because no current is flowing. Say, it is like this, potential of Y also will be just like this. It is 12 volts till the transistor is turned on, under normal condition, it is V_{CE} plus this drop, this normal condition. In case, if this increases, it is an overload condition. So therefore, by monitoring the voltage at point y, it can be inferred that whether the transistor is operating in quasi saturation or it is trying to come out of quasi saturation, can be inferred.

Let me tell you one thing, this comparison should be done only after say, t_{on}. See, if you have to apply positive I_v to the transistor, wait for some time, only then, voltage at point y or V_{CE} falls. So till this period, even if V_{CE} is high, no action should be taken. Action should be taken only when V_{CE} increases in this region. So, that is about protecting a BJT from overload condition. I just want to tell you about a floating ground. Now, what is a floating ground?

See in this circuit, all the control signals that applied to the BJT with respect to its emitter. So, this potential is at 12 volts with respect to emitter. Now, what is the potential of emitter? The potential of an emitter is equal to the potential of the collector that is equal to the high voltage when the transistor is on because when the transistor is on, V_{CE} drops to a very low value.

This potential is same as the emitter potential and in the circuit when the transistor is off, it is assumed that no current flows. I am neglecting the leakage current. So, potential of E is 0. So, I have a reference point in this circuit whose potential is keep on changing and depends on the conducting state of the transistor. I said, this potential is at 12 volts with respect to emitter and potential of this point itself is equal to a high voltage potential, this voltage when the transistor is on.

So, a precaution to be taken is that just because 12 volts is being used in drive circuit, one should not touch the components in the drive circuit because the potential itself is floating. Say, a collector is connected to 400 volts, DC supply. So, attending D_1 time the potential in the drive circuitry could be 400 volts or so because emitter potential itself is changing. Whereas, these digital circuits, there also supply voltages are there, say, plus 5, minus plus 5 or plus 12 depending upon the logic circuits that I used here.

This is the actual ground and this ground, they are not the same. This should not be connected because this is the entire power circuit and there is opto isolator to isolate the power circuit from the driver circuit and potential in this part is floating with respect to emitter. Yes, these are all may be, at 12 volts but then emitter potential itself is changing. So, that is about bipolar junction transistor. Now, let us discuss another device what is known as the Power MOSFET.

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See here metal oxide semiconductor field effect transistor, MOSFET. This was developed in 1978, 100 volt, 25 ampere power MOSFET. As of now in the market say, 200 volt 500 ampere MOSFET is available, manufactured by SEMIKRON or say 60 volts 100 ampere SEMIKRON MOSFET is available. So generally, MOSFETs are a low voltage, high current devices. So, that is why they are very popular in power electronic equipment which converts a DC to another DC, something known as DC to DC conversion. We will study some time later. These are very popular in DC to DC power conversion. These are really fast devices, very fast devices compared to a BJT.

BJT is a minority carrier device whereas, a MOS is a majority carrier device like, similar to BJT is a non latching device. See here, symbolically it can be represented in this manner, D stands for drain, G stands for gate and S stands for source. So, this potential is V_{GS}, gate to source. V_{DS}, drain to source, remember, it is a majority carrier device. Let us see the structure, how does it looks like?

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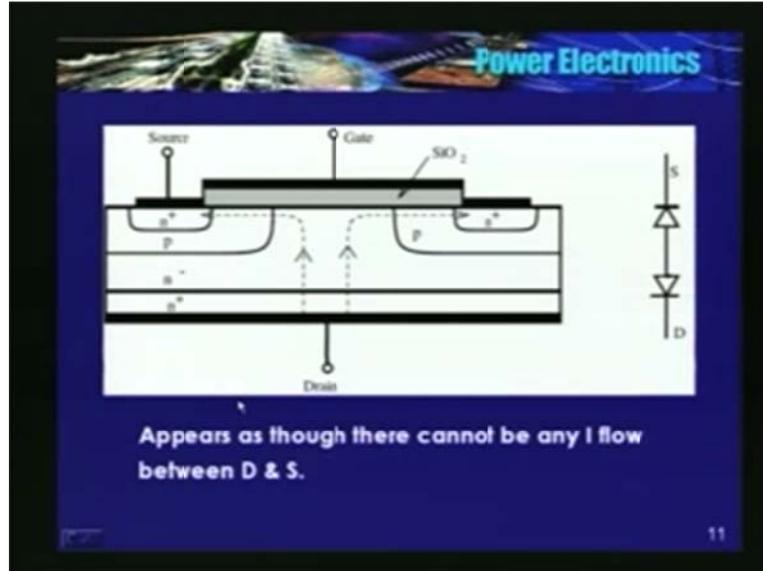
Drain, immediately there is a N plus layer and there is a N minus layer to block the forward voltage, there is a P layer and N plus layer, this is the source, here is a gate and in between the gate and the source there is silicon dioxide, SiO_2, SiO_2 which is an insulator. This is an insulator, so, in principle you cannot have any current flow between gate and source because there is an insulator in between and if at all the current flows, a very small current will flow. A MOSFET has very high input impedance and it is mainly a capacitive type, a very high input impedance. So, gate power requirement is very small.

So now, just see the structure, source and drain, source is S and drain is D here and see, here is a diode NP and again a PN. So, it appears as though there cannot be any flow of current between drain to source because at any given time, one of the diodes is reverse biased. If I connect source negative and make drain positive, this diode is reverse biased and vice versa. So, how does the current flows?

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See, gate is insulated from the rest of the device. So, if at all, if the current flows, it is in micro amperes. Again, no steady current, some sort of a displacement current, as in the case of a parallel plate capacitor. So, MOSFET is said to be in cut off when a gate to source voltage is less than a threshold value. I will repeat, MOSFET is not cut off when a gate to source voltage is less than a threshold value.

Now, what happens when the gate to source voltage is higher than the threshold value? The layer between the silicon, a small channel is formed just below the silicon layer. See, it converts silicon surface below the gate into an N type channel. I will show you in the figure.

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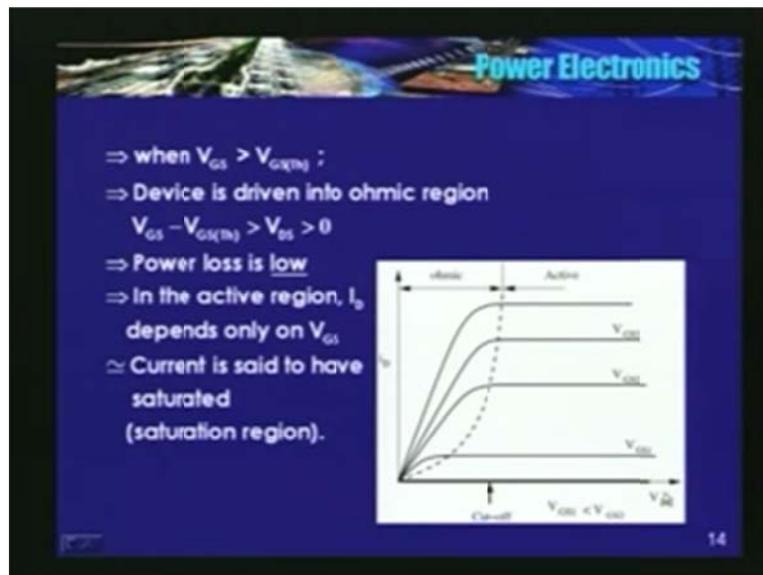When the gate to source voltage is higher than the threshold, a small channel below the silicon surface it forms. So, electron starts flowing in this manner or the current starts flowing in this manner. So, when this voltage increases above a threshold value, a small channel is formed below the silicon. So, electron starts flowing in this manner.

Now, this threshold value depends on the oxide layer, SiO_2 layer and it can be reduced by reducing the thickness. Now, when V_{GS}, the gate to source voltage is higher than the threshold value, device is driven into ohmic region. See, in a transistor also we had cut off, active and saturation. Even in MOSFET we have three regions; cut off, ohmic and active. See, I will show you.

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This is a cut off mode when V_{GS}, gate to source voltage is less than the threshold. See, this region is the ohmic region, also known as the linear region. See, these are the various plots for the various values of gate to source voltages, I_D versus the drained source voltage. So, as gate to source voltage increases, you have a higher value of I_D. The region between these two zones is almost linear, the characteristic is almost linear, hence the name ohmic.

Whereas, in active region, I_D's remains almost constant, independent of V_{DS}, the voltage between drain to source and depends only on V_{GS}. So, in active region, we can say that current is saturated. So, is also known as the saturation region. See, just the opposite, BJT. BJT, this is supposed to be active or linear region. This was saturation but region was not that broad. So, we are calling linear region as ohmic region, active as saturation.

When is in ohmic, the device is driven into ohmic region when gate to source voltage minus V_{GS} threshold is higher than V_{DS}, drain to source and is higher than 0. So, in the ohmic region, V_{DS} is low. So, how do I represent the MOSFET in ohmic zone or ohmic region? Characteristics are almost linear. Can I represent it by a register? Yes.

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In on state, the channel of the device behaves like a resistance, $R_{DS\,(ON)}$. It is the slope of V_{DS} or slope of V_{DS} versus I_D characteristics. This is R_{DS}. So therefore, what is the conduction power loss or power loss during conduction? It was equal to V_{CE} into I_C, in the case of transistor.

In case of a MOSFET, it is I_D squared the drain current multiplied by $R_{DS\,(ON)}$ and this loss is higher than V_{CE} into I_C, in the case of a BJT. V_C is SAT into I_C, in the case of a BJT. See, BJT requires a continuous base current. That is what I said a small power transistor is required to drive another power transistor. But then, it has a substantially lower voltage drop when that BJT is in conduction mode compared to a MOSFET. Now, see the structure again.

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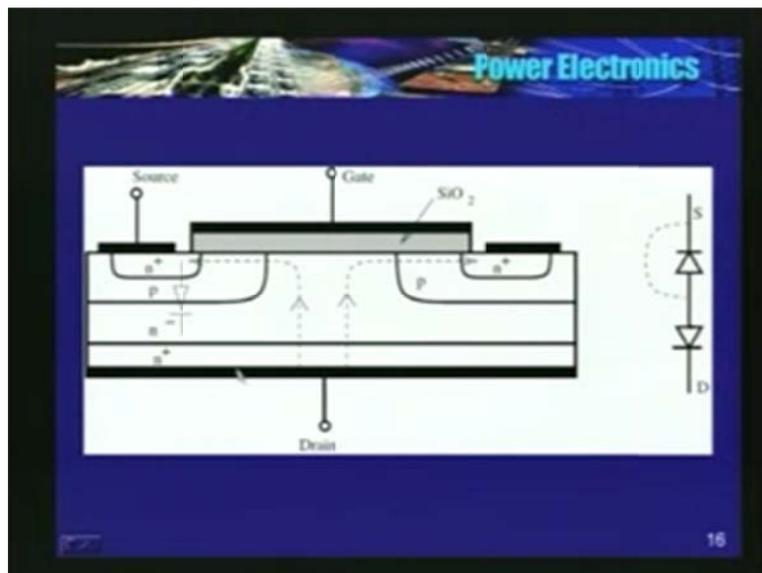
We have a NPN transistor. How do I or eliminate the effect of this transistor? What did I do here? I have shorted this N layer and P layer by a source. Now, the structure is something like this, base and emitter, they are shorted. But then, there is a diode. There is a diode in the reverse fashion. See, the current is flowing from drain to source. Even if I short this diode, there is a diode what is known as the body diode which is connected in the reverse fashion. The cathode is connected to drain, anode to the source.

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So, symbolically it will look something like this, this is a MOS and it has the body diode, this existence. So, MOS can block a positive voltage DS, D should be positive with respect to the source. You cannot make D negative S positive. Because, the moment you make, we have an uncontrolled element here, a diode. So, this cannot block a negative voltage. But then, it can carry the current in both directions, drain to source and source to drain. So positive current, MOSFET carries and negative current, the body diode. So, this diode has adequate current rating and switching speed.

I told you, MOSFET is a really fast device. It is a majority carrier device because when the gate threshold, gate to source voltage is higher than the threshold, N channel is found below the silicon surface and the electron starts flowing. There are no minority carriers. It is only a majority carrier device. It is a very fast device, this a body diode has an adequate current rating also has adequate switching speed.

But then, in certain application, power electronic application, if you require a very fast diode, the effect of body diode is eliminated by connecting a diode in series with the drain, by connecting a diode in this fashion. Now, this diode cannot carry the current. Direction of current is going to be in only 1 direction and a separate, a high frequency diode is connected in this. So, that is about the MOSFET structure.

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How does the safe operating area for MOSS look like? BJT we had I_C limit, V_{CE} limit, P_J limit or junction temperature limit and there is a fourth one was a secondary breakdown because of the local hot spots. It has negative temperature coefficient. So, there could be some local hot spots and that is the limit in the safe operating area.

A MOSFET is a majority carrier device. It has a positive temperature coefficient. So, paralleling is easy. Why? See, I have connected 2 devices in parallel, they have positive temperature coefficient, assume that temperature has increased. Therefore, the resistance increases. So, if the resistance increases, 2 devices in parallel, current that is flowing to the device comes down.

So, the current flowing through devices comes down. So, temperature reduces. So, paralleling of MOSS is easier because they have a positive temperature coefficient. Now, since it has a positive temperature coefficient, there is nothing like a secondary breakdown in MOSFET. So therefore, safe operating area, there are only 3 limits. They are AB is a drain current, maximum drain current, CD is the maximum voltage that device can block and BC is the maximum power dissipation. This is the imposed by $R_{DS\,(ON)}$.
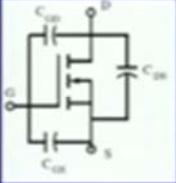
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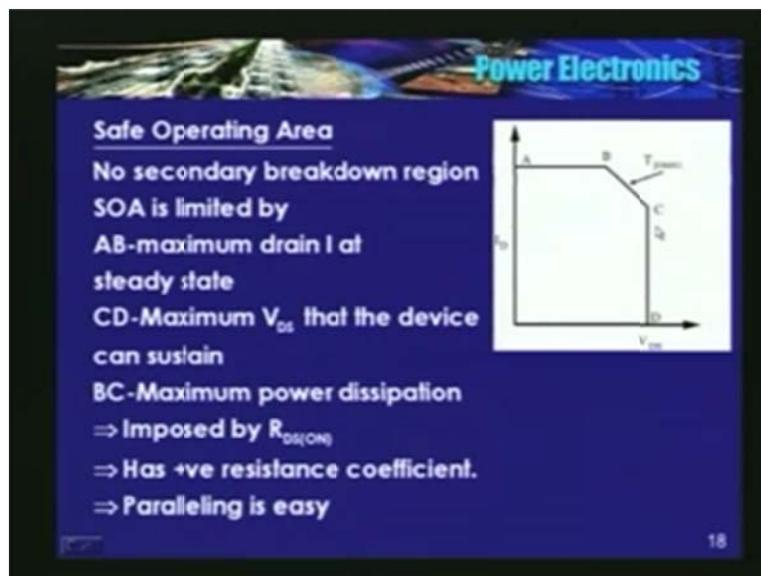
I told you that when the MOS is in the ohmic region or in the linear region, it can be represented by a register, the slope of the characteristics. So, I_D squared into R_{DS} is the on state power loss. So BC, this region, this region is imposed by $R_{DS\,(ON)}$.

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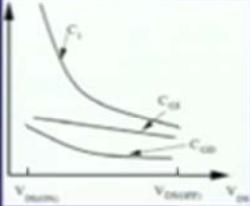

Now, come to the internal capacitance of the MOS, I told you that gate is insulated from source as well as the drain. It is insulated, so if I can apply a voltage, small leakage current can flow. In principle, I can represent it by a capacitor. So therefore, there are 3 types of capacitor. One is see in this one, 1 is gate to source C_{GS}, this capacitor C_{GS}. What is the dielectric for this capacitor? It is an oxide layer, isolating gate and source and this value is almost independent of the variations in V_{DS}, drain to source voltage. I will repeat, gate to source capacitance is almost independent of V_{DS}. How about other two capacitors? C_{GD} capacitors between gate to drain. It is a strong function of drain to source voltage.

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See here, gate to drain capacitance varies considerably with V_{DS}. So, this is the variation. For low values of V_{DS} or that happens when the device is on, this capacitance is high and if it is in the blocking mode, at that time V_{DS} is very high, this capacitance is very small. Whereas see, this gate to source remains approximately constant, independent of V_{DS}, whereas gate to drain, it has a high value when the device is on and it has a very low value when the device is off and the third one between a drain and source is of less important.

Now, the sum of capacitance between gate to drain and gate to source is known as the input impedance. Gate to drain and gate to source is the input capacitance and see the variation here, is the sum of these 2 and it is generally in terms, in pico Farads and this input capacitance plays a very important role while turning on the MOS and turning off the MOS. So, during turn on, you need to charge these 2 capacitors, gate to drain and gate to source.

The rate at which you charge this capacitors, determines the turn on time of the MOSFET. With that I will conclude my today's lecture. More, we will discuss in the next class.

Thank you.