Power Electronics

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Lecture - 7

Hello, in my last class we discussed about SCRs. It is a semi control switch. Why it is a semi control switch? Because, device can be turned on by applying a control signal at the gate but then you cannot turn it off by applying a control signal at the gate. It is a latching device. Why it is a latching device? Control signal at the gate can be withdrawn, once the current through the device is higher than the latching. It does not require a continuous gate drive. It allows conduction only when it is forward biased and it is in conduction mode. So, another device that we studied in the previous lecture was a track, functionally it is equivalent to 2 thyristors connected anti parallel. So, it is like this.

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Review:

TRIAC :→ Functionally equivalent to 2 thyristors connected anti-parallel.

Can be triggered by

MT_2 + ve, I_G +ve || W.R.T. MT_1

MT_2 - ve, I_G -ve || W.R.T. MT_1

⇒ $\frac{dv}{dt}$ rating < than that of SCR

There are 2 thyristors connected anti parallel and a common gate; functionally is equivalent. I told you that this device can be triggered by making MT_2 positive with respect to MT_1 and supplying a positive gate current with respect to MT_1. This condition, both positive, MT_2 is positive, I_G is positive with respect to MT_1, it can also be triggered by making MT_2 negative, I_G negative with respect to MT_1. So, the VI characteristics, they look like this, positive I_G and a negative I_G. So, what is the difference between the SCR and a TRIAC? The dv by dt rating for

track is less compared to that of a SCR. TRIAC has a less time to recover the blocking mode compared to a SCR. Why?

See in this circuit, ((Refer Slide Time: 3:42)) at any given time if this device is reverse biased, this gets forward biased. When this device is turning off, a negative voltage gets applied across it and this negative voltage forward biases this device and in case the rate of change of voltage is high, this device may turn on. So, these are some of the essential difference between a track and a SCR.

The next device that we studied was a GTO, it is again a high power device, a 6 KV, 6 kilo ampere device is available, is being manufactured by Mitsubishi. See here, 6 KV, 6 kilo amperes by Mitsubishi, it has being developed.

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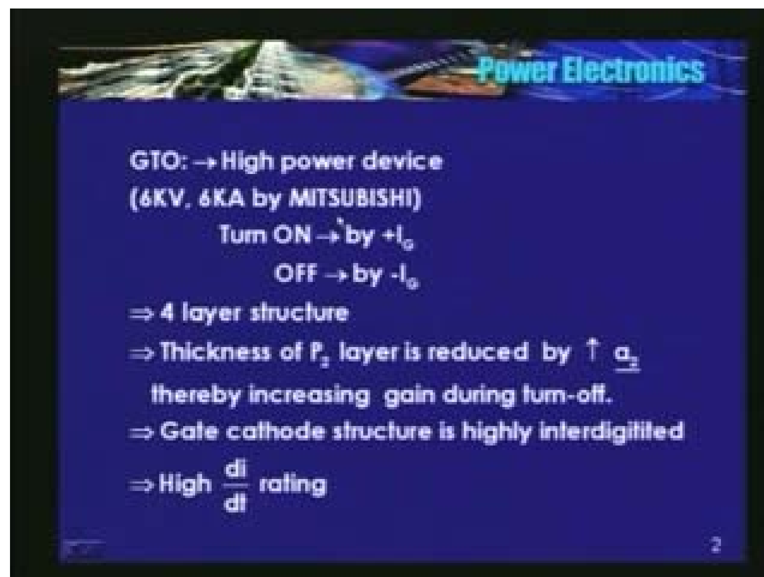

SCR and track, these are semi controlled switches, both, whereas, GTO is a fully controlled switch. You can turn on by positive I_G and you can turn off by negative I_G. GTO has 4 layer structures similar to SCR. What are the differences? I told you that thickness of P_2 layer is reduced in order to increase $alpha_2$, thereby, increase in the gain during turn off.

See, turn off gain is a function of $alpha_2$. It is $alpha_2$ divided by $alpha_1$ plus $alpha_2$ minus1. Now, the gain can be increased by increasing $alpha_2$. How do I increase $alpha_2$? By decreasing the thickness of P_2 that is why I told you in my last lecture. What is another essential difference between GTO and a track or GTO and a SCR?

In GTO, gate and cathode structures are highly inter digitated. It is something like this, highly inter digitated. So, the result is cathode periphery has increased and even the remote part of the

cathode is very near to the gate. That is what I told you, a high power GTO can be seen as a large number of small GTOs in parallel. So therefore, it has a very high di by dt rating. Because, of the highly gate cathode structure being highly inter digitated, a large area is available during conduction or at the instant of turn on, a large area is available.

So therefore, it has a very high di by dt rating. In other words, GTO can be brought into conduction at a much faster rate or a turn on snubber, a small inductor is required in series with the device compared to SCR. What is another feature that has to be taken into account while turn on? A gate current, a continuous gate current should be maintained in the on period. See, it is something like this.

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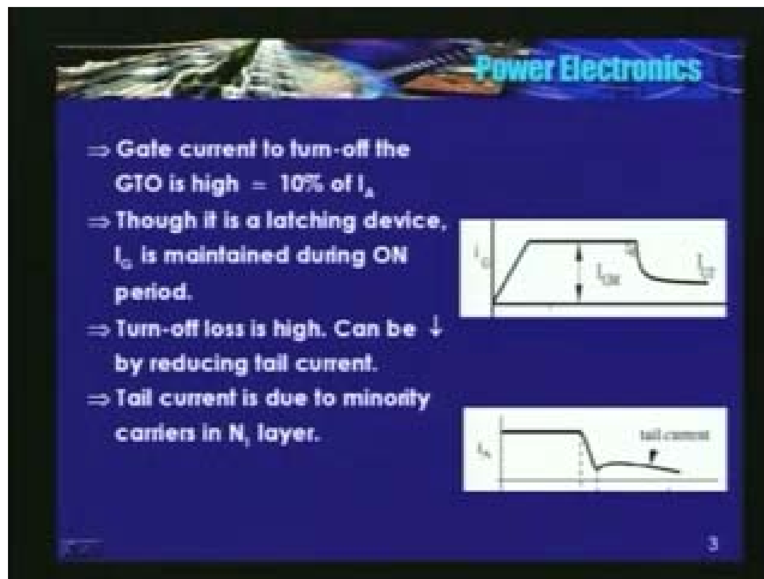

Having turned on the device completely, the gate current can be reduced but a small current should be maintained continuously because I told you, momentarily if I_A falls or the anode current falls, some of the cathode highlands may turn off and subsequently if the anode current increases, the entire area is not available for conduction. So, it may so happen that only a small area that is available, current is the same, so there will be a hot spots and device may fail.

Remember, though GTO can be turned off by applying a control signal at the gate, the turn off gain is small. So, a large current is required to turn off a conducting GTO. Turn off loss is also high. Why? It is because of the tail current. How do you reduce the turn off loss? Turn off loss can be reduced by reducing the duration for which the tail current falls.

We have seen, in the sense when the GTO is turning off, voltage across that is increasing but for substantial period tail current flows through the device. Therefore, turn off losses is high. See, like this, tail current, a very high dr by dt and this is a tail current period and during this period,

voltage across a device, as a result to quite a high value, there will be, turn off losses will be high. How will you reduce this tail current or what is a reason for this tail current? It is due to the minority carriers in N_1 layer.

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So, the duration of tail current can be reduced by penetrating this, a highly doped N layer in the P layer. See, we see N layer is penetrating at regular intervals in the P layer and it is directly in contact with N minus layer and because of this the tail current or the duration for which the tail current flows reduces. But then, this structure cannot block a negative voltage. This is also known as an anode short structure. Now, whereas this can block a negative voltage because of junction J_1„ whereas here, junction J_1 or N plus is directly in contact with N minus junction J_1. So, it cannot block negative voltage, whereas this device can block a negative voltage.

What is another point that we discussed? The inductance in the loop found by GTO and the turn off snubber should be very small, see this.

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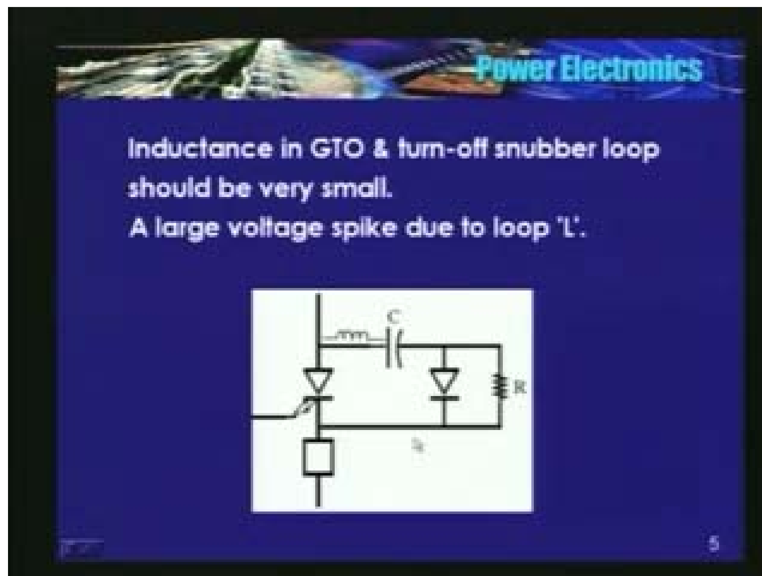

The loop inductance should be very small. Why? It is because of this loop inductance when you turn off GTO, the current does not get transfered to this snubber. So, there is going to be a large voltage spike. So, this inductance should be very small. In other words, snubber layout is very, I will show you a GTO manufactured by Toshiba.

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A 600 ampere device, gate terminal and we need to use 2 heat sinks. It is like, formed sandwiched in between 2 heat sinks, a 600 ampere GTO. So, that is about the GTO. So, we have studied SCR, track and GTO.

Fourth one, a BJT, bipolar junction transistor, I told you that it was developed in 1948 and in 1975 a 300 volt, 400 ampere giant transistor was developed by Toshiba. See here, in 1975 a 300 volt 400 ampere giant transistor by Toshiba.

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BJT (1948)

In 1975 ⇒ 300V, 400A, giant Transistor by Toshiba.
⇒ Power transistors are normally of NPN type.
⇒ N layer which forms the collector is thickest.
⇒ Reverse blocking capability is small.
⇒ Emitter is heavily doped to increase β.
⇒ Operated in quasi – saturation & cut-off

In saturation $I_c = \frac{V_{cc} - V_{CE(sat)}}{R} \neq \beta I_b$

Power transistors are normally of NPN type and the N layer which forms the collector is the thickest one, because that layer, the N layer has to block the voltage. Can you block the reverse voltage? Base emitter or emitter junction is highly doped, so therefore, the breakdown voltage or base emitter junction is very small. Therefore, reverse blocking capability is small. Invariably, BJT is in power electronic circuits are operated either in saturation not deep in saturation, just at the edge of the saturation and in cut off. Definitely, not inactive because in active power loss that is taking place the device is high.

Generally, for high voltage BJT, current gain is low and especially it is operated in saturation. See, in saturation, collector current no longer equal to beta into I_B where beta is gain when it is operating in active mode. In saturation, how to determine the collector current? I_C is equal to V_{CC} minus V_C is sat divided by RL.

See, in this circuit assume that this BJT is operating in saturation. I_C is V_{CC} minus, V_C is sat divided by R and it is not equal to beta into I_B where beta is the gain when it is operating in active mode or active reach.

First of all, high voltage BJT is current gain is low and it is operated in saturation. So, as the collector current increases, the base current requirement also increases. So, how do I overcome this limitation? Use a Darlington circuit. What is a Darlington circuit? See, it is shown here.

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2 transistors or more than 2 connected in this fashion. Now, what is a gain of this combination? I_C is the total current, I_{C1} is flowing through transistor 1 and I_{C2} is flowing through transistor 2. So, total I_C is I_{C1} plus I_{C2} and what is I_{C1}? It is $beta_1$ into $I_{B1.}$ Some I_{B1} is flowing into the base of transistor 1 and I am measuring some beta. Definitely, is not the same beta of the transistor when it is operating in active mode.

So, $beta_1$ into I_{B1} is $I_{C1.}$ Similarly, I_{C2} is some $beta_2$ into $I_{B2.}$ This is the base current, I_{B2} but then what is I_{B2}? I_{B2} is same as the emitter current of transistor 1, I_{E1} and what is a relationship between I_{E1} and I_{B1}? It is beta plus 1 into $I_{B1.}$ Now, you substitute this value in this equation. What do you get?

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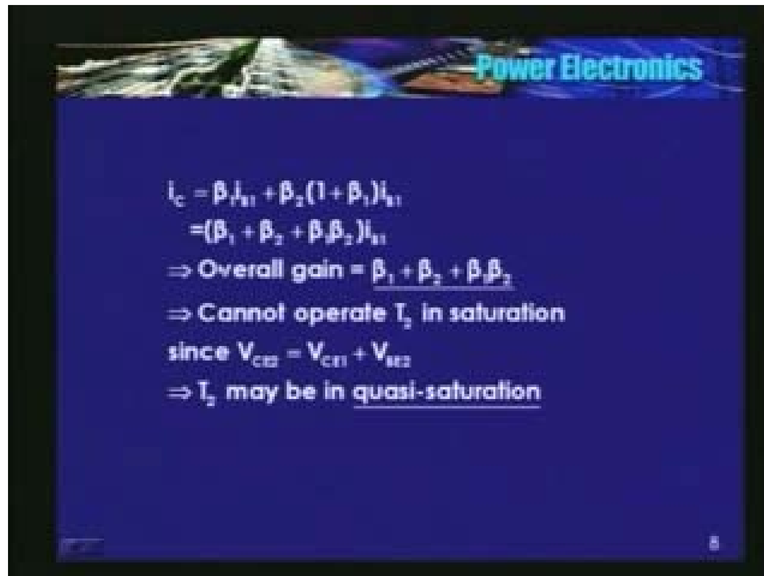

You will get, $beta_1$ plus $beta_2$ plus B_1 B_2 $beta_1$ plus $beta_2$ into I_{B1}. So, the overall gain here is $beta_1$ plus $beta_2$ plus $beta_1$ into $beta_2$. So therefore, for the same I_C, I require a very small base current that has to be supplied to transistor 1. But then, what is the disadvantage here? Can I operate T_2 in saturation? Answer is no. Why?

See, in this circuit, what is V_{CE2}? V_{CE2} is equal to V_{BE2} plus V_{CE1}. V_{BE2} plus V_{CE1} is equal to V_{E2}. I am assuming V_{B2} of the order of 0.7 volts, I am assuming and I am assuming that transistor T_1 is in saturation. So, V, a voltage across transistor 2, V_{CE2} equal to V_C is sat of transistor 1 plus V_{BE2}.

So therefore, it may not be possible to operate transistor 2 in saturation. So therefore, the loss is taking place in transistor, the final transistor or transistor 2 here, are high. So, that is the disadvantage. Now, how about the safe operating area of the device when it is in forward biased mode or when it is conduction mode? See it is here, on state safe operating area or forward biased safe operating area, FBSOA.

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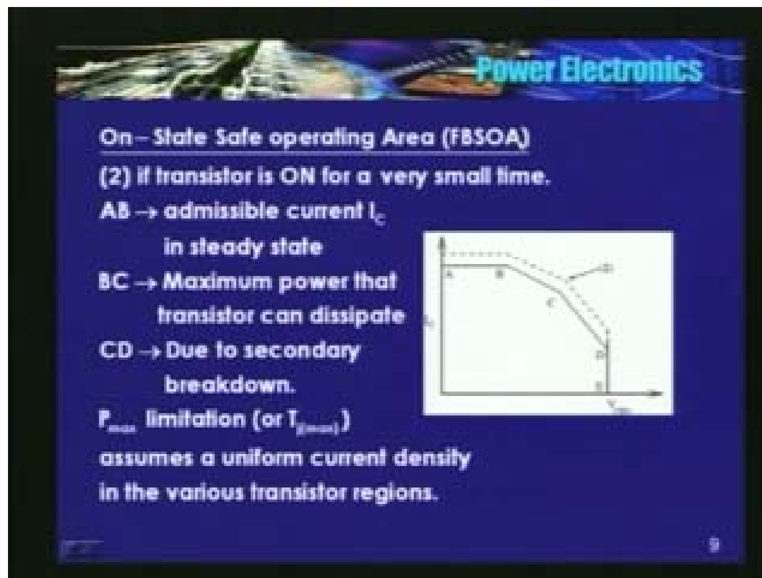

May be, in my second or third lecture while discussing the ideal switch, I said, we drew 3 limits. One is I_c current that is flowing through the device, voltage through the device, sorry, voltage across the device and another one is a power limit. But, if you see for a BJT, there are 4 limits, I_c verses $V_{CE.}$ So, if you see AB, it is an admissible current, I_C in study state. So, a device can carry this much of current in the voltage across it is, may be of this value.

Beyond that point, there is another boundary BC. It is the maximum power that the transistor can dissipate and CD is due to secondary breakdown. What do you mean by secondary breakdown? I will explain to you. BC is the maximum power that a device can dissipate. It assumes that a uniform current density in the various transistor regions. So, BC limit assumes that uniform current density throughout.

Let me tell you one thing, it just not possible to achieve this. Transistor is a minority carrier device. It has a negative resistance coefficient, it is a property. BJT has a negative minority carrier device. Therefore, it has a negative resistance coefficient. So in other words, as the temperature increases, resistance comes down.

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See in this, one way to explain or the reason for having a negative resistance coefficient is this, the minority carrier density in the transistor. The minority carrier density is proportional to the intrinsic current density and which increases exponentially with the temperature. Since, it is a, BJT is a minority carrier device, it has a negative resistance coefficient and it is because of this.

So, since it has negative resistance coefficient, paralleling 2 transistors is difficult. For that matter, any device which has a negative resistance coefficient, paralleling is difficult. Why it is difficult? See, I will just explain to you. I have connected 2 resistors in parallel. Assume that 1 of them has a negative resistance coefficient. Because of the temperature rise, R_1 has decreased by a small value, R_1 minus delta R_1. So, there is a slight decrease in the resistance. Now, this 2 are in parallel. So, smaller the resistance, higher is the current that it will carry.

So, current that is flowing through R_1 will increase. As the current in the R_1 increases, power dissipated in R_1 increases. Now, the power dissipated in R_1 increases, temperature increases. Now, if temperature increases, again there is a reduction in the resistance because it has negative resistance coefficient. So, there is going to be again a reduction in the total resistance of R_1. So, thereby, it starts carrying more current. So, it goes on building up and eventually it will fail.

So therefore, any device which has a negative resistance coefficient, paralleling is difficult. So, that is about the secondary breakdown and this is due to the minority carrier device and the last one is a DE. E is the maximum voltage that the device can sustain, DE. This is for a study state or continuous current and in case, if the transistor is on for a very short duration, the boundaries of SOA expand.

See here, this dotted for the device when it is on for very short duration. Because, if a device is on for very short duration, temperature rise or power dissipation limit can also be increased.

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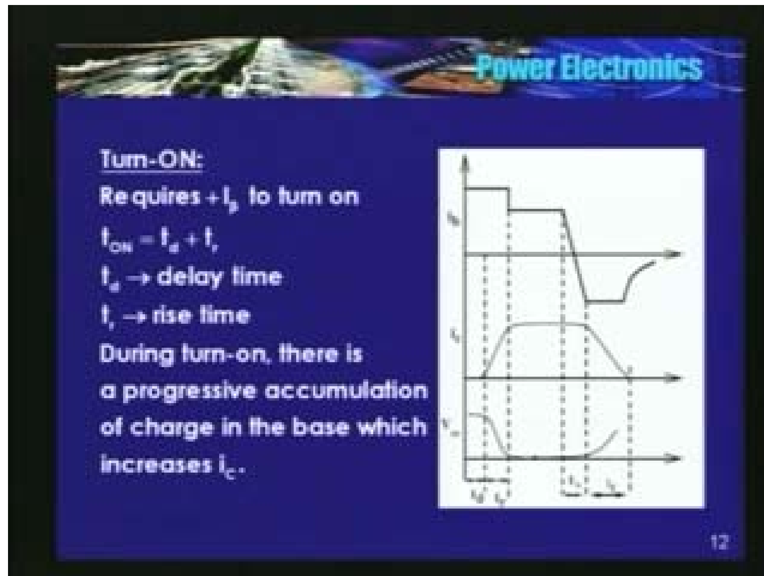

Now, coming to the turn of the BJT, all of us now, it requires a positive I_B to turn on. So, here are the wave forms. See, in the on period, there are 2 values of $I_{B.}$ I will tell you sometimes later the reason for this. A positive I_B has been applied to the base but then the collector current does not start increasing immediately. It takes some time what is known as the delay time.

During $t_{d,}$ though you have applied a positive $I_{B,}$ I_C is 0 and V_{CC} is the rated. After $t_{d,}$ I_C collector current starts increasing and the collector voltage starts falling and this increase in current is determined by the load circuit or the external circuit. So, the total on time is t_d plus $t_{r,}$ the delay time and the rise time. This total t_{on} time should be as small as possible. So, how do you reduce this t_{on}? t_{on} can be reduced by momentarily supplying a high current at the base.

So, that is the reason, at this point or during this period, during on period, a high current is flowing through the base, into the base. This value is approximately, 1.5 times this value but then why I_B should be reduced after t_{on}? Why cannot you maintain the same I_B? If you maintain the same $I_{B,}$ transistor may go into, deep into saturation. So, that has to be avoided. Why that has to be avoided? We will study in the turn off process.

So, when the device is turned on, if you see, V_{CE} has dropped down to a very low value. Of course, definitely not equal to 0. It is V_{CE} sat, a good power transistor, this value could be of the order of 2volts. So, on state power loss is V_{CE} sat multiplied by $I_{C.}$ It is an on state power loss. So, it is mentioned here.

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$t_d \rightarrow$ delay time.
$t_r \rightarrow$ should be very small
In order to reduce t_{ON}, supply $I_B = 1.5 I_{B(required)}$
$\Rightarrow$ Transistor is operated in quasi saturation mode.
On state loss = $V_{CE(sat)} * I_C$

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In order to reduce the t_{on} period, supply the base current equal to 1.5 times the required or the study state I_B.

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Turn – off :
$t = t_s + t_f$
$t_s \rightarrow$ Storage time
= delay between the change of base current & the instant when I_C starts ↓.
$\Rightarrow$ Limits the upper frequency of operation
$t_f \rightarrow$ Fall time of I_C
Storage time : If transistor is in saturation/quasi saturation, width of base region ↑
$\Rightarrow$ Equivalent to as if a part of collector is transformed to base. I_C remains constant.

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Now, coming to turn off, there are or t_{off} consists of t_s what is known as storage time plus the fall time of I_C. Similar to GTO, during storage time, though the gate signal or gate current has becomes negative, I_c remains approximately same. So in other words, the t_s, the storage time is the delay between the change of base current from positive to negative and the instant when I_c

starts reducing, higher the t_s, higher is the total turn off time. So, as the t_{off} time increases, you may have to come down on the upper frequency of operation.

So now, let us study the operation of a transistor when it is in saturation. When the transistor is in saturation or in quasi-saturation, the width of the base region increases, say, I just show, you see in this figure.

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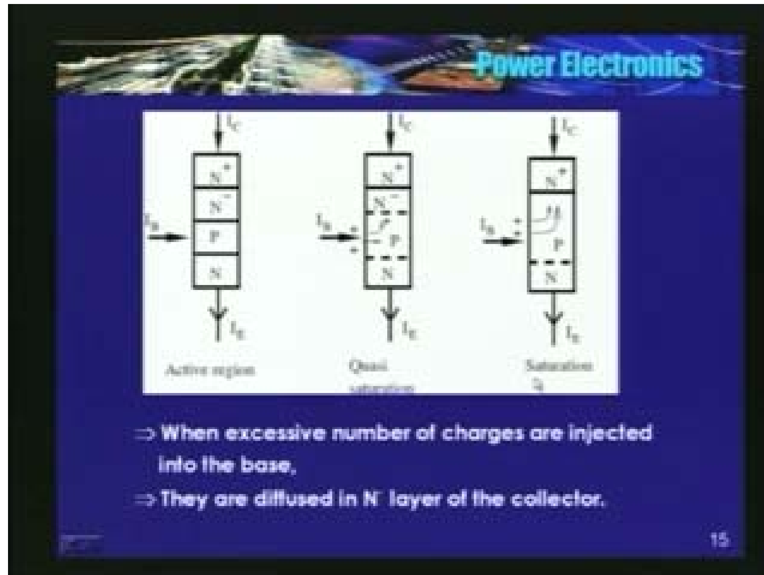

This is a normal transistor in active region. N P under N layer, this N minus is lightly doped and N plus is highly doped and this thickness will determine the maximum voltage that it can block. So, as I_B increases, the thickness of N minus layer decreases. See in this figure, this layer decreases because you are injecting a large number of charges into the base and they get diffused into N minus layer. This is a quasi-saturation region.

Now, thickness of N minus layer is reducing. It is a highly resistive layer, the thickness is reducing. Therefore, the voltage drop across the transistor, V_{CE} also falls. As I_B is increased further, this N minus layer completely disappears and this region or this mode of operation is known as saturation mode. Devices completely saturated or highly saturated. See, the explanation is given here.

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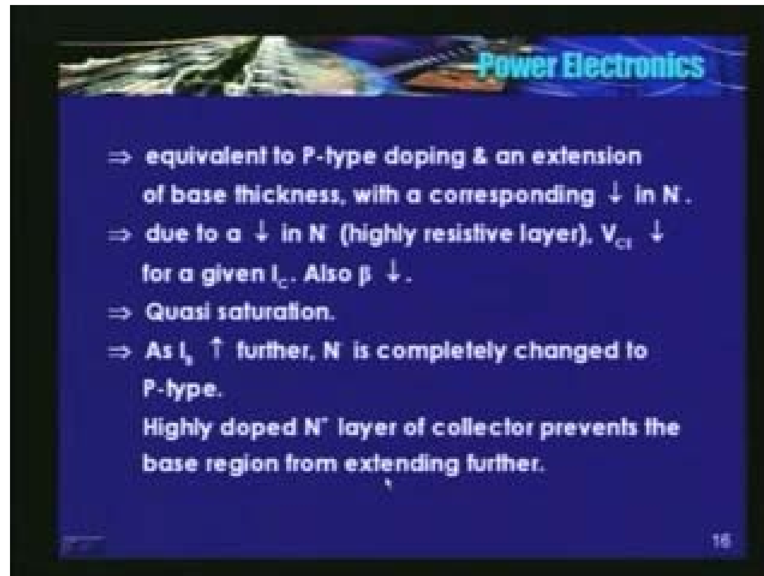

Saturation is equivalent to the P-type doping and an extension of base thickness with a corresponding decrease in N minus. It is this figure wherein, there is a reduction in the N minus layer. It is equivalent to P-type doping and an extension of base thickness with the corresponding decrease in N minus layer. Now, due to this decrease in N minus, because lightly doped, N minus, minus indicates the doping level is low, is a highly resistive layer.

So, V_{CE} drops for a given I_C and this we know, as the transistor saturates, gain comes down and as I_B is increased further, N_1 is completely changed to P-type and this highly doped N plus layer of the collector prevents the base region from extending further. It cannot, the base region does not extend further.

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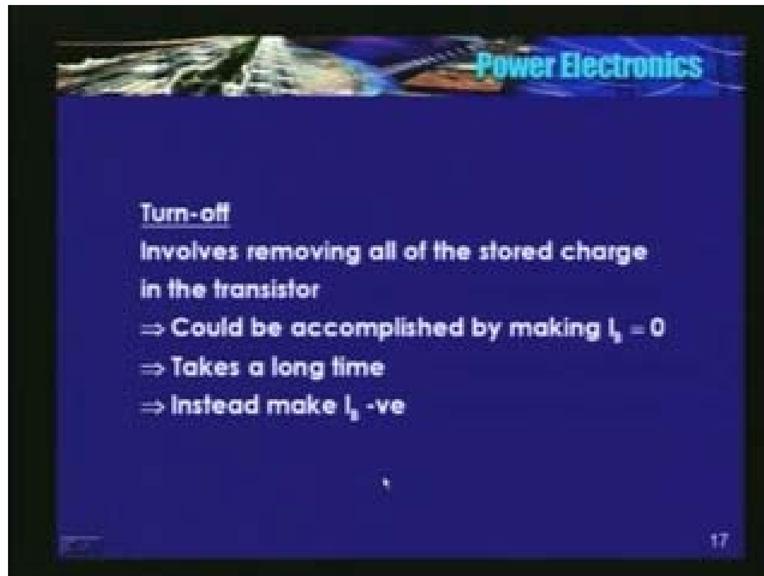

So, how do I turn off the transistor? It involves the removing of all the stored charge in the transistor. See, during turn on there is a progressive increase of charges into the base. Now, the turn off is removing all the stored charges from the base or from the transistor. Now, this can be accomplished by making I_B is equal to 0.

Just open the base terminal I_B is equal to 0. Transistor will turn off but then it takes a long time. Now instead, you make I_B negative, a negative base drive. Invariably, a BJT is turned off by applying a negative I_B.

How much I_B should be flowing out of the base to turn off the transistor? See, to turn on the transistor, we supplied a high pulse of current to reduce the on time and transistor is operated in all most in the saturation region. In other words, it is just entering the saturation region.

Now, you want to turn it off, what should be the value of I_B? Remember, prior to turn off if the transistor is in over saturated region, in other words if the transistor is operating deep into saturation, a large I_B should not be applied. A high value of minus I_B should not be applied to turn it off. Why? If you apply a large value of minus I_B in the base, it will result into the rapid evacuation of carriers from the base.

There is going to be rapid evacuation of the charges from the base. Therefore, the base emitter junction becomes cut off but then holes in the collector region requires certain time to recombine and let me tell you one thing, this I_B minus I_B has negligible effect on this time. By supplying a minus I_B, rapid evacuation of the carriers from the base has taken place, the base emitter junction has becomes cut off now, but then those whole switches are there in the collector region, they require a certain time to recombine and minus I_B has negligible effect on this time.

So therefore, the times are instant when the base emitter junction has become cut off. Till this process gets completed, this is equivalent to diode in the reverse recovery mode. See here, from the time base emitter junction is in cut off and base collector current continuous to flow that is due to the holes, base collector.

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The operation is equivalent to a diode during t_{rr} or reverse recovery time and this is also known as the current tail. Invariably, during this period, V_C is already attained a reasonably high value, almost similar to a GTO. We had current tail there because of the minority carriers in N minus.

So, during tail current tail period, V_C is high. So therefore, losses that are taking place in the device will increase. So, if the losses in the device increase, you could have something known as thermal run away because of the negative resistance coefficient.

So therefore, if the device is operated in saturation, I_B should be gradually increased in a negative direction, something like this. High value of I_B to reduce the on time or t_{on} at study state and it is a gradual increase in the negative direction. A constant value then afterwards current, this is I_B, gradually decreased in the negative direction. Now, how do you ensure that transistor does not get into saturation?

So, there is trade of, if the transistor gets deep into saturation, V_{CE} is low. So therefore, total losses that are taking place in the device are low but then as it is driven into saturation, storage time increases. So, you have to come down on the frequency of operation, natural frequency or the switching frequency of the device.

Now, instead of operating the device into deep into saturation, operate somewhere at the edge what is known as the quasi saturation. How will you ensure this? There is a network what is known as the anti saturation network is also known as the Baker clamp which ensures transistor is always operated in quasi saturation. See, here is the network.

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This is the power BJT and this network D_1 D_2 D_3 D_4. I will explain to you the function of each diode. See, the advantage of operating the transistor in quasi saturation is that V_{CE} increases slightly but then the storage time reduces significantly. There is a great reduction in t_s, the storage time.

Now, with this anti saturation network, what is the value of V_{CE}? V_{CE} gives the measure of the saturation level or degree of saturation of the transistor. See here now V_{CE}, this voltage is equal to V_{BE} plus V_{D1}, sorry V_{D2} plus V_{D3}. These 2 diode drops minus this drop.

So, V_{BE} plus these 2 diodes drops minus this diode. It is V_{CE}. So now, V_{CE} is maintained at assuming that all the diodes have same voltage drop when they are conducting. Now, V_{CE} is maintained at V_{BE} plus V_{D1}, voltage drop across 1 diode. Now, by connecting more number of diodes in this part, you can increase V_{CE}. I have just connected 2.

So, by connecting additional diodes in series with D_2 or D_3, V_{CE} can be increased. Now, how this network prevents transistor getting into saturation, this is one way of analyzing. How does this circuit work?

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Assume Transistor is off.
+ve I_B applied at point x
Till $V_{CE} = V_x - V_{D1}$
D_1 is off.
All I_B will flow through
D_2 & D_3 & into the base.

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Assume that transistor is off, entire V_{CC} appears across the device and I want to turn on the transistor, as positive I_B is being applied to this circuit. See in this circuit, I have connected, I have used the Baker clamp, a transistor and there is a small load, a simple circuit to explain the principle. So, a positive I_B is applied at point x, this transistor is off, in other words, potential of C with respect to the ground is same as $V_{CC,}$ there is no current here.

This is at Vx, definitely this voltage is very low. So, D_1 is reverse biased, cathode potential is same as V_{CC} and anode potential is a potential of x and Vx is very small. So, all the current starts flowing through D_2 and D_3 and to the base. Transistor turns on, therefore, V_{CE} falls. Now, in order to reduce the $t_{on,}$ I said that 1.5 times I_B should be supplied.

So, V_{CE} falls when this V_{CE} is equal to Vx minus V_{D1} or Vx minus 0.7 volts. I am assuming that voltage drop across D_1 is 0.7. We will see what sort of diode is D_1 and what could be the voltage drop across it, sometime later.

As of now, I will assume that voltage drop across D_1 when it is conducting is 0.7 volts. So, when V_{CE} is Vx minus 0.7, D_1 starts conducting. So, when D_1 starts conducting, a part of I_B starts flowing through $D_{1,}$ a part of I_B starts flowing there. So therefore, there is a reduction in current that is flowing into the base. I will repeat, initially D_1 was off, transistor is off, V_{CE} or the collector potential is very high, may be is equal to $V_{CC.}$ All the current flows through D_1 and sorry, all the current flows through D_2 and D_3 and into the base.

As transistor turns on, V_{CE} falls and when V_{CE} is equal to Vx minus, this drop, voltage drop across $D_{1,}$ D_1 turns on a part of the current starts flowing through diode D_1 and this junction. So, there is going to be an automatic reduction of current flowing into D_2 and $D_{3.}$ Say second case, a

load has varied, see invariably, the base of circuit is designed in such a way that it supplies the required current for a full load and load or the load that the transistor was supplying is reduced. In other words, I_C has come down. Now, if I supply the same $I_{B,}$ transistor will go into saturation. That is what I showed you, those 3 figures, active quasi saturation and saturation. As the charges are pumped into the base are increases, N_1 layer reduces.

Now, the load has reduced. If I maintain the same $I_{B,}$ transistor is entering into saturation, V_{CE} falls. But then V_{CE} in this circuit cannot fall below a value which is equal to Vx minus $V_{D1.}$ See, in this circuit at any given time, VCE is clamped at Vx minus $V_{D1.}$ So, even the load has come down, if the load has come down, same I_B will not flow.

See, transistor is trying to get into go into saturation, V_C is trying to fall, the moment V_C is trying to fall, D_1 turns on. It diverts some of the base current. So, base current gets diverted and therefore, this transistor cannot enter the saturation. So, that is all this Baker clamp works. Why do you require D_4? D_4 is to supply a negative $I_{B.}$ Negative $I_{B,}$ D_1 sorry, D_2 D_3 for a positive I_B and D_4 is for negative $I_{B.}$

All these current ratings, D_1 D_2 D_3 D_4 current ratings are small, the maximum they carry, see this is a base drive current it has to carry but then voltage ratings of these diodes are different. D_2 D_3 D_4 these are low voltage, low current diodes, whereas, D_1 should be a high voltage diode. It should be a high voltage diode because when the transistor is off, cathode potential is at same, at $V_{CC.}$

So, D_1 has to block the entire $V_{CC.}$ So, D_1 is a high voltage, low current diode, whereas these D_2 D_3 D_4 are low voltage, low current diodes. So, with this I conclude my today's lecture.

Thank you.