Power Electronics

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Lecture - 6

Hello, in my last class we discussed the need for snubber circuits, the turn on snubber and turn off snubber. These circuits are required to protect the device against dr by dt and the voltage spike across the SCR. How did we limit dr by dt? We connected a small inductor in series with the thyristor. Now, we know that the current through the inductor cannot change instantaneously and how do we limit the voltage spike across the SCR? We use a RC network.

The second point that we discussed was a high frequency pulse pattern is recommended to trigger the thyristor, large number of high frequency pulses. How do we transmit these signals from the control circuit to the gate? We use a pulse transformer. See here, this is the pulse transformer.

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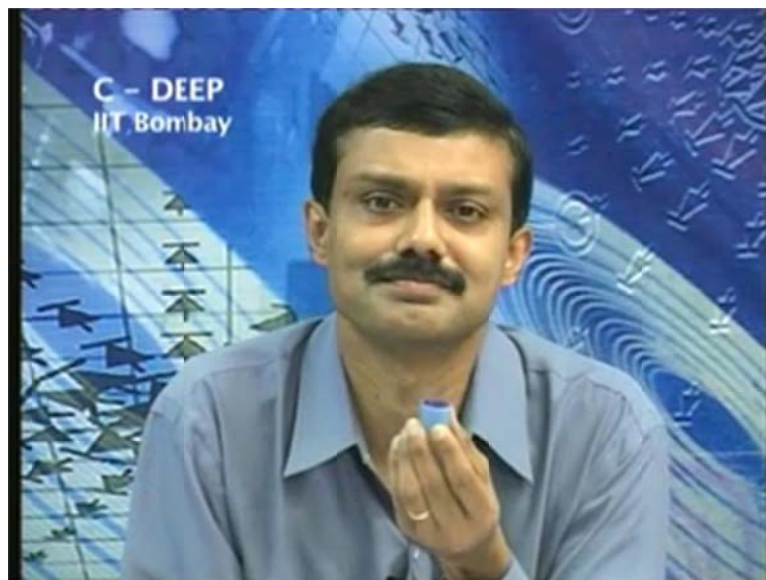
It is a special type of transformer. Why it is a special type? The signals or the frequency of the signals that is transmitting from one side to the another side is very high. The principle of operation of this transformer is same as that of a 50 hertz transformer. Only the type of core is different. See, in a 50 hertz transformer, we use a laminated core whereas a high frequency transformer, ferrite core is used.
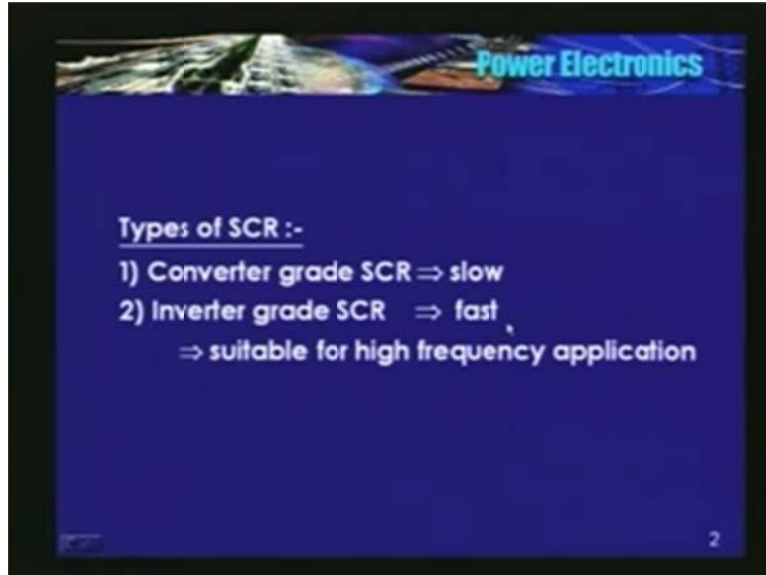
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Ferrite core, of course this is a bigger ferrite core, a solid ferrite core, these are suitable for high frequency application. So, there are 4 terminals, primary winding and the secondary winding. On top it is written, 1 is to 1, it implies that the number of turns in the primary winding is same as the number of turns in the secondary winding. So, this is a pulse transformer used to isolate the power circuit from the control circuit.

Now, what are the different types of SCR's? We had different types of diodes. Similarly there are different types of SCR's also. One of them is see here, the converter grade SCR. These are slow devices, they are used in the circuit wherein the frequency could be 50 hertz and the second one is the inverter grade SCR. So, these are fast devices, fast devices so suitable for high frequency application. So, here is the module that has two thyristors.

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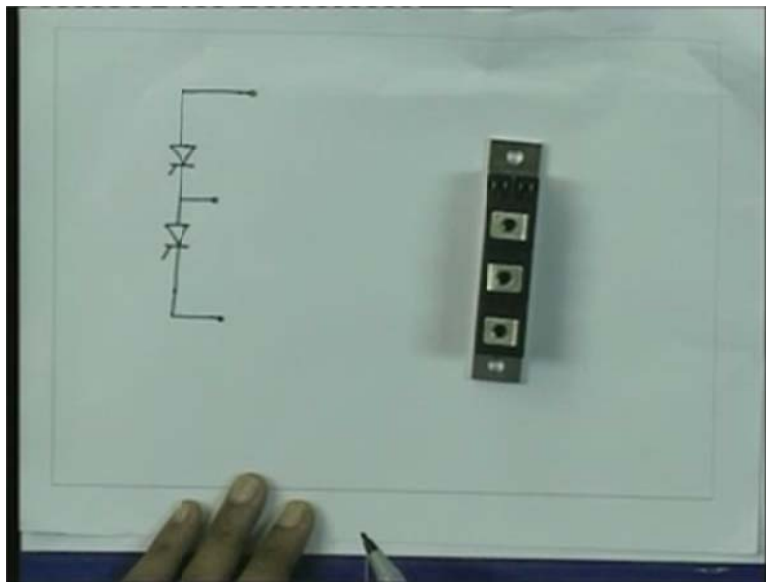
Inverter grade thyristor, the rating of each thyristor is 45 ampere and the voltage rating is 1200 volts. 2 thyristors, see they are connected in this fashion. See, these are the 2 thyristors, 3 terminals, 3 power terminals have been brought out, anode of one, a common point and the cathode of another. See, these 2 terminals for supplying the gate signal, cathode and gate, see here cathode and gate. See the contact area, this anode, cathode so generally the load current flows.

So, see the surface area that is available whereas, see the surface area that is available for gate and cathode. A small current is flowing from the gate and it is mounted on a heat sink. See, how elegant it looks.

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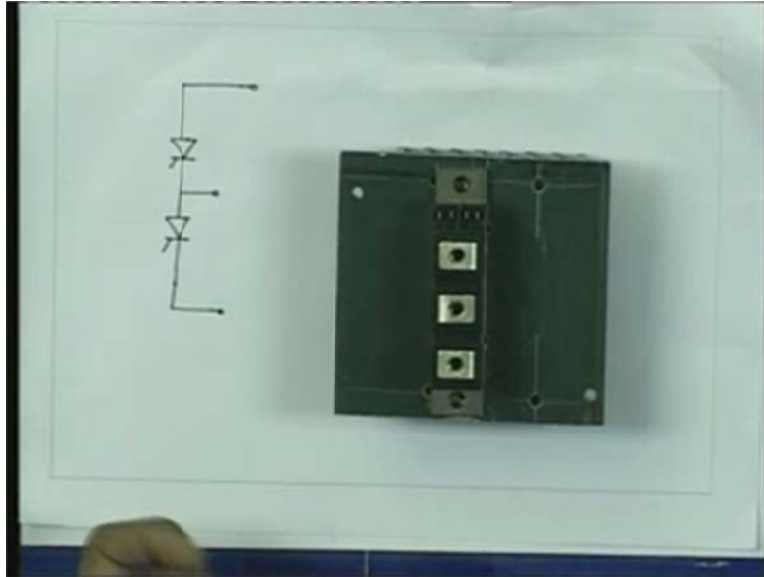
So, that is why I told you in my introductive lecture that the one of the main reason for the popularity of power electronics is the advances in power semiconductor technology. So, the rating of this thyristor is given here, I copied from, I downloaded this data sheet from their site.

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See, 46F. F stands for first 0 8 dot dot till 13. This stands for the various voltage ratings. See, if it is only 0 8, the voltage rating is 800 volts. If it is 13, the voltage rating is 1300 volts. See, repetitive peak, forward off state and reverse voltages. These are the various voltages. See, the RMS current rating, 120 amperes whereas, the average on state current is 45 amperes. See, the surge current rating, 1300 amperes. I explained to you, what is surge current or when it flows, 1300 amperes and another important parameter, I squared t current, squared time rating is required to determine the fuse. 8450 amperes squared s.

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See, the critical rate of rise of on state current, di by dt critical is 120 ampere for micro second. See, the gate trigger current I_{GT} 150 milli amperes. So therefore, just see the gain average current, rating is 45 amperes. Surge current is 1300 amperes, gate current is 150 milli amperes. See, the gate trigger voltage 1.4 volts, holding current 250 milli amperes, latching current 1000 milli amperes. See, I told you that latching current is higher than the holding current. So, these are the some of the important parameters of the thyristor.
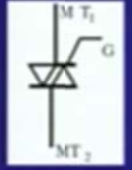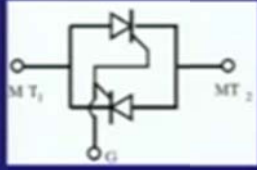
So, that is about the conventional thyristor which conducts when it is forward biased. When it is reverse biased, it does not conduct. What if input is AC? Output is also AC. Like, you know fan regulators, see, I have a 50 hertz AC supply, 230 volts and there is a regulator to regulate the voltage applied to the machine or voltage applied to the fan to vary the speed. Fan is again a single phase AC machine. So, it requires an AC supply. I have an input AC, output is also AC. So definitely, I need to connect 2 thyristors in anti parallel. Now, instead of connecting 2 thyristors separately in anti parallel, there is a device available what is known as the triac. A triac was developed in 1964 by general electric.

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It has a complicated structure but then functionally it is equivalent to 2 thyristors connected anti parallel. See, here is the connection, I have 1 thyristor, thyristor 2, gates are tied together G and I am calling this terminals as MT_1 and this as MT_2. See, I cannot call anode and cathode because anode of one is tied to cathode of another thyristor. So, there are 2 equivalent thyristor connected in anti parallel. So, now it is going to be a bidirectional device. Remember, it is a bidirectional device, there are 2 power terminals but then there is only 1 gate terminal.

So therefore, how do I trigger? A triac can be triggered by see here, making MT_2 positive with respect to MT_1 and supplying a positive gate current with respect to MT_1. See, I will repeat, MT_2 should be positive with respect to MT_1 and a positive gate current with respect to MT. It can also be triggered when MT_2 is negative with respect to MT_1 and by a negative current, negative gate current with respect to MT_1.

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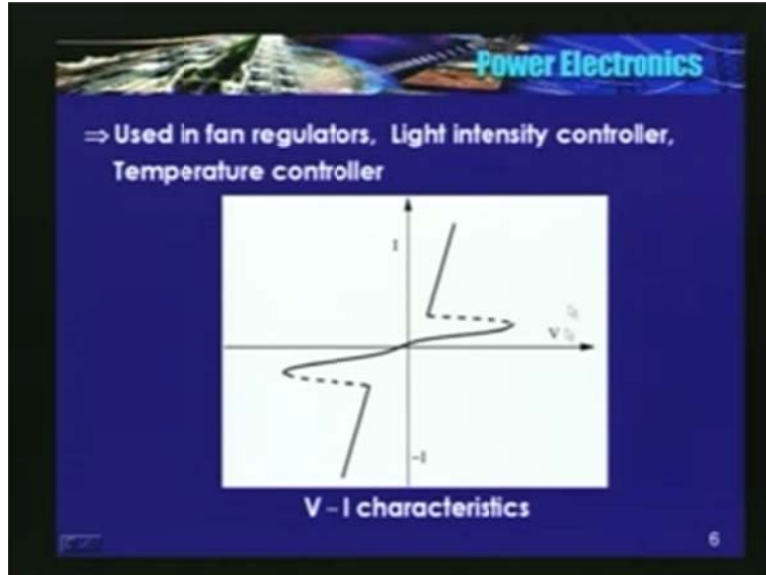
So, here are the characteristics. 2 thyristors connected in anti parallel, say thyristor 1 and this could be thyristor 2. These are the VI characteristics, negative resistance, regional unstable conduction, forward blocking, forward blocking mode for another thyristor, conduction mode for the same thyristor. So, these are the VI characteristics. This triacs are very popular in fan regulators. I told you, I showed you a very elegant fan regulator, just the knob is brought out everything is mounted inside a switch board.

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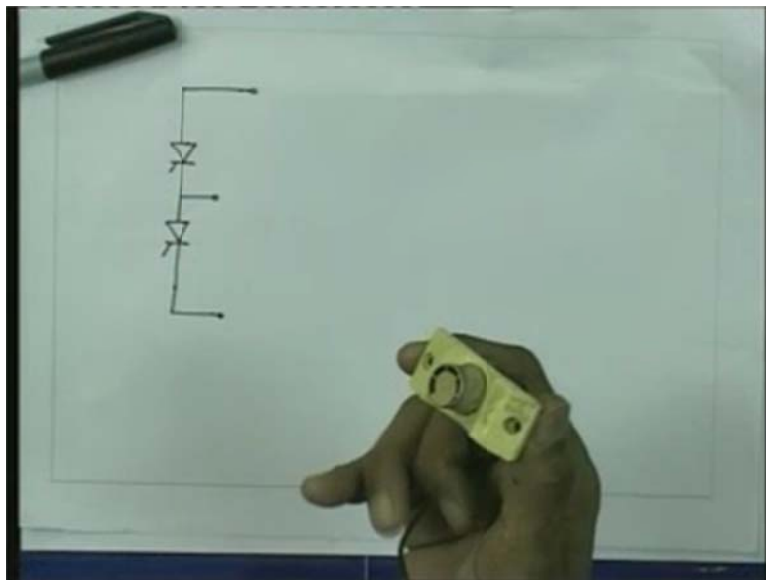
So, there is no power dissipation. That is why it is so small and I told you, this is a power semi conductor device, has three legs. MT_1 MT_2 and gate, this are nothing but a triac. This is a triac,

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this is a triac. So, triacs are also used in light intensity control, room temperature control but then what is a limitation of a triac? See, I am just showing you the turn off characteristic of a thyristor.

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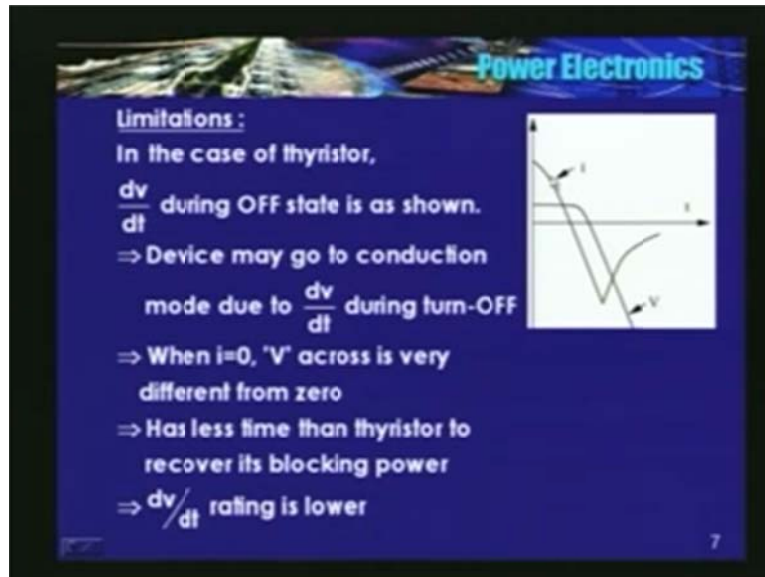
The current has reversed, it has attained a peak value, the reverse recovery current and at this point J_1 and J_2, J_1 and J_3 have attained the voltage blocking capability. So therefore, a negative voltage is applied across the thyristor and this happens, this current decays at a very fast rate. So, this is the turn off characteristics that we studied for the thyristor. So, when this current has becoming 0, the voltage across it is very different from 0.
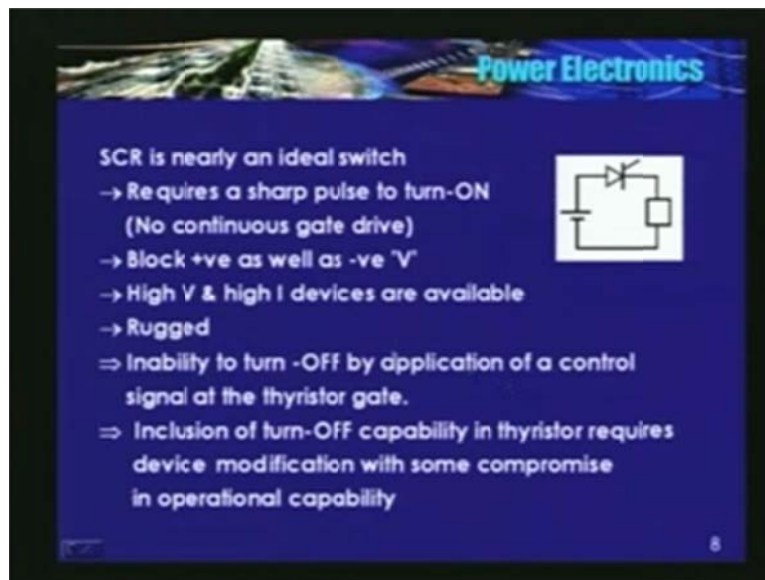
Now, this is for 1 thyristor, the turn off characteristics. When it is turning off there is a high voltage appearing across the entire combination across the triac. So, there is another thyristor connected in anti parallel. Now, if this dv by dt is high, it may trigger another thyristor when this current has become 0.

See, this apprehension was not there when in the case of thyristor because there is only 1 device. It has to block in the reverse direction as long as has voltage across it is less than the reverse breakdown voltage. But then in a triac, there are 2 thyristor, the triac is equivalent to 2 thyristor connected back to back. So, when a reverse voltage is being applied to 1 of them, the forward voltage appears across another thyristor. So, the another thyristor may get triggered because of this dv by dt or in other words, triac has a less time than a thyristor to recover its blocking power.

See, I have written here, it has less time than the thyristor to recover its blocking power or the dv by dt rating is less for the triac. So, now let me sum up the thyristor. It is nearly an ideal switch. Why it is an ideal switch? It requires just a sharp pulse to turn on. If 45 ampere thyristor, average current rating, maximum gate current is 150 milli amperes that is required only during this switching or turn on period. When the current is higher than the latching, you can withdraw the gate signal.

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So, the gate power requirement is very small compared to the power rating of the thyristor. It can block both positive as well as negative voltage. The rating of this thyristor is 1200 volts forward as well as reverse, also high voltage, high current devices are available in the market. The forth point, device is very rugged, sturdy but then what is the limitation? It has 1 limitation. It cannot be turned off by the application for control signal at the thyristor gate. It cannot turn it off by applying a negative gate current through the gate. So see here, I have summed all the properties of the thyristor.

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So, this is the limitation, inability to turn off by application of a control signal at the thyristor gate. To turn off the thyristor, current flowing through it should be reduced to a value which is less than the holding current. Till then it continues to conduct.

So, how do I make this device which is capable of turning off through gate? Can I do some modifications? Answer is yes. So, there is a device what is known as the gate turn off thyristor, GTO which is capable of turning on as well as turning off through gate. By applying a control signal, we can turn off as well as turn on a GTO. See here, a gate turn off thyristor, GTO.

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A small power GTO was developed by GE, general electric in 1961 and in 1981, a 2.5 kv, 1 kilo ampere GTOs developed by Hitachi and Toshiba. It can be turned on by positive I_G and can be turned off by negative I_G and here are the 2 symbolic representations of the GTO, the same. Anode cathode structure is the same, across here are 2 arrows, positive I_G negative I_G. So, these are the 2 symbols used to represent a GTO.

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What is the structure? In what way it is structurally different from a thyristor? It has 4 layers similar to SCR, $P_1 N_1 P_2 N_2$. Then, in what way it is different? How it is being turned off by

applying a negative I_G to the gate? We will see. See here $P_1 N_1 P_2 N_2$, one of the difference is thickness of P_2 is less in the case of a GTO. Why, I will tell you some time later.

The second difference is N_2 layer is removed by itching in place where gate contacts are situated. I will show you a 3D picture and it will be very clear, see here.

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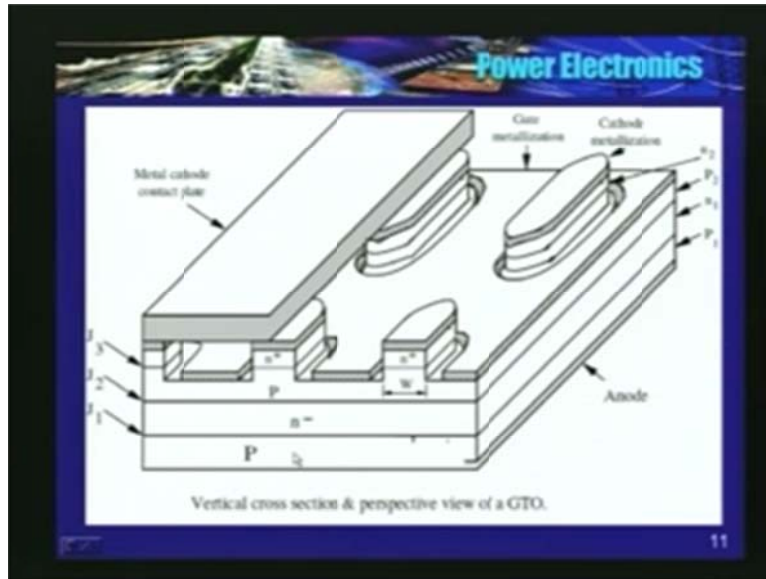
See, we have P or $P_1 N_1 P_2$. Now, N_2 is in small places, small islands of N_2 are found, see here. There is 1 here, see here, again a separate N_2 layer, a small island of N_2 layer. See, this minus indicates the doping level is very low and the plus indicates doping level is very high. So, it is similar to SCR, N_2 layer is highly doped, N_1 layer is very lightly doped.

So, there are large numbers of small islands of cathode or in other words, what I can say is see, there are large number of GTO's. See here, $P_1 N_1 P_2 N_2$, $P_1 N_1 P_2 N_2$ see here also $P_1 N_1 P_2 N_2$ and all the cathodes of these GTO's are connected to a common heat sink and that forms a main cathode. So, what you can say is a GTO can be seen as a large number of small GTO's in parallel, as if there is a GTO here or another GTO here, another GTO here. One GTO can be seen as a large number of GTO's connected in parallel. Why parallel?

Anode is same, cathode is also same, all the cathodes are connected to 1 heat sink and that heat sink forms the main cathode and another difference between a GTO and a SCR is in a GTO gate and cathode structures are highly inter digitized. What do you mean by highly inter digitized? It is something like this, this is inter digitization, this could be inter digitization. So, what is the advantage of doing like a inter digitization? The advantage is that now the cathode periphery has increased, also the distance between the gate and a cathode is very small. If this is gate and this is cathode, this is inter digitization, cathode periphery has increased the distance between the cathode and gate has reduced.

What is the advantage of this inter digitization? I will tell you some time later. Now, you just see the structure again. I have a P layer, it is equivalent to P_1 in SCR. Junction J_1, N layer lightly doped, junction J_2 and J_3. So, when it is reverse biased, J_1 should block the voltage because though J_3 is also reverse biased, the reverse blocking voltage of J_3 is very small similar to SCR and when is forward biased J_2 blocks the voltage.

Now, there is another structure. See here, variant a N plus layer in other words, a highly doped N layer penetrates this P_1 layer and it is directly in contact with the N minus layer or the N_1 layer.
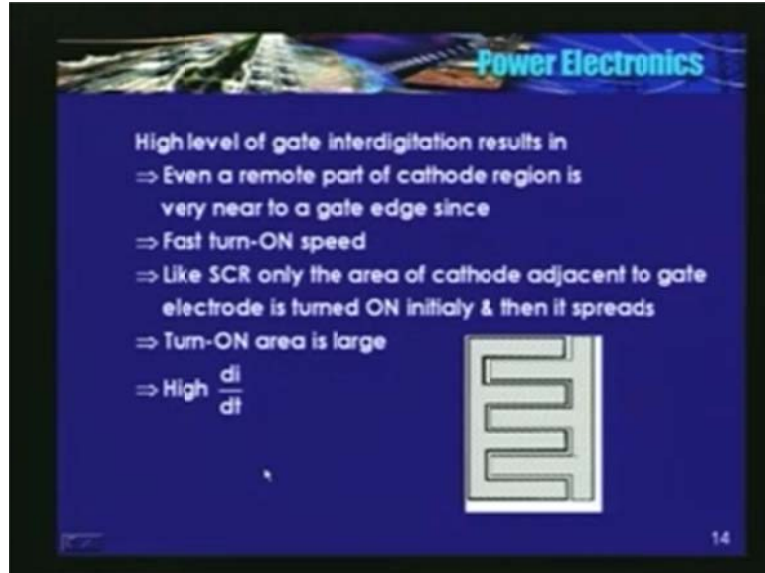
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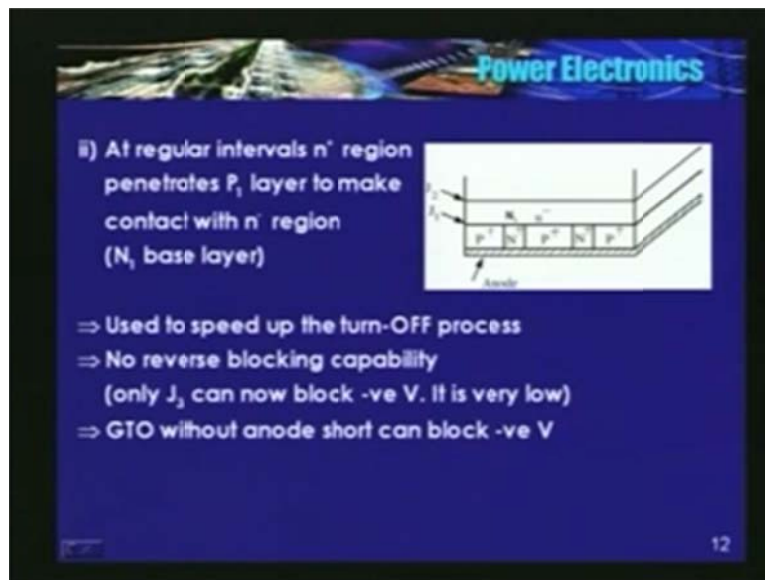
See here in this figure, this N plus layer penetrates at regular intervals and it is directly in contact with N_1 or N minus layer. So, in other words there is a direct shot between the anode and J_1 when it is reverse biased. See, when it is reverse bias, entire voltage as we blocked by J_1 because we had a P structure. Now, because of this N plus which is in directly in contact with anode and N_1, now J_1 cannot block the negative voltage, the only 1 junction that can block the negative voltage is J_3.

The reverse voltage blocking capability is very small. So in other words, this structure cannot block negative voltage or a anode short structure cannot block negative voltage. So, this GTO is also known as a symmetrical GTO. Why it can block only positive voltage? It is because of junction J_2 and it cannot block the negative voltage. If at all, if it can block is a very small voltage that is because of J_3, another advantage of doing this modification is that it speeds up the turn off process. Now, how it speeds up the turn off process? I will tell you while doing the turn off of a GTO. See in this, a 3D figure shown, here is same thing P_1 or P plus highly doped N plus N minus P.

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Now, coming to the inter digitization, I told you, the remote part of a cathode is very near to the gate. In SCR, why did we limit dr by dt during turn on? It is because the area that is available for conduction is very small when you turn on the device. It is a area of the cathode adjacent to the gate electrode is available and afterwards the conduction spreads to the other parts. Now, what happens in the GTO because of this inter digitization? Even the remote part of the cathode is very near to the gate. So in other words, a large area is available during the turn on period or at the instant of turn on, a large area is available. So therefore, you can have a very high dr by dt during turn on.

Since the dr by dt is very large, GTO can be brought into conduction at a much faster rate compared to SCR. This is because of inter digitization. Even the remote part of the cathode is very near to the gate, large area is available, so you can have a very high dr by dt. So, if I can have a very high dr by dt, I can or turn on time of the GTO reduces.

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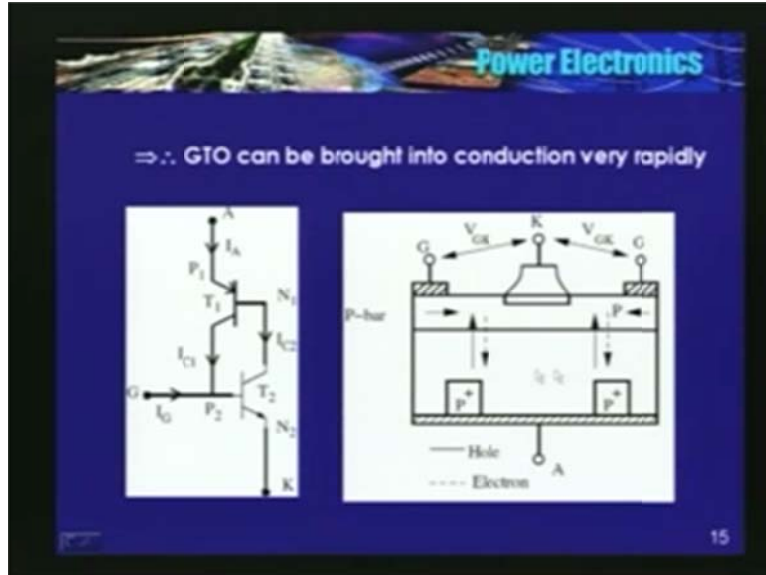
See, in a 3D it looks something like this, I have chosen a anode short structure. So, these are the gates, the cathode, the direction of holes, the direction of electric. So, GTO can be brought into conduction very rapidly that is because of a very high dr by dt is possible.

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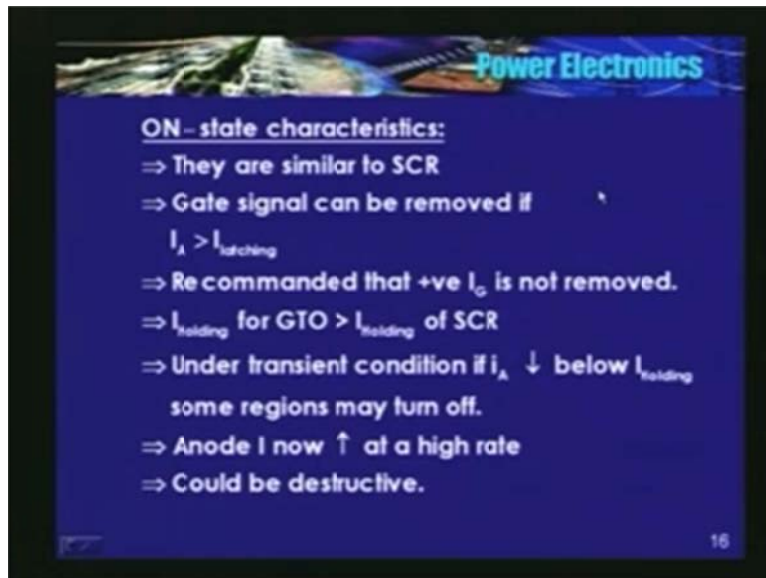
Now, coming to the turn on characteristics, they are similar to an SCR. There is no much difference between the SCR characteristics and the GTO characteristics. It is a latching device, in the sense, in principle, gate signal can be withdrawn once the anode current is higher than the latching current. But it is recommended that a positive I_G is maintained throughout during the conduction period. Why? It is because of this reason, I told you one of the limitations or one of

the difference between the GTO and SCR is that holding current for a GTO is much higher compared to a SCR. Holding current of a GTO is higher compared to SCR.

Now, assume that am doing some disturbance, anode current has dipped momentarily. Since the anode current had dipped momentarily, some of parts of the GTO might turn off and now again the current, anode current increases very rapidly, the area that is available for conduction is very small. So therefore, there could be some hot spots and because of this localized heating, a GTO may get damaged. So therefore, it is recommended that during conduction period, a positive I_G is maintained throughout. But then, you do not need to maintain the same magnitude of the gate current.

So, what is being done is a high pulse of gate current is provided during turn on, so that the turn on time can be reduced and after sometime you can reduce this gate current. See the wave form, looks something like this.

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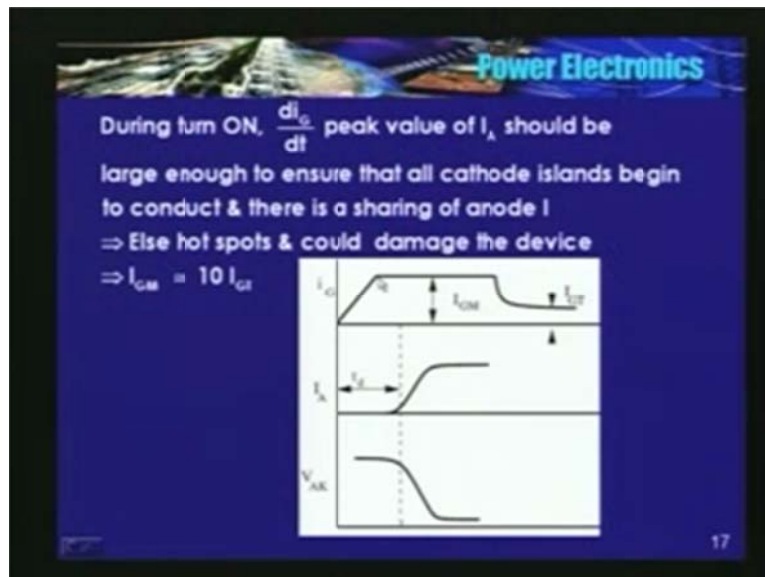
A high gate current, so anode current has attained a study value after some time t_d what is known as the delay time. The voltage across the device also reduced to its saturation value. So, after sometime you can reduce the gate current to I_{GT}. So, this value is approximately 10% of this peak value.

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So, that is about the turn on of the GTO. Now, coming to the turn off of a GTO, so even in the case of a thyristor when the thyristor is on, both T_1 and T_2 are in saturation. That is why the voltage drops to a very low value, could be of the order of 1.5 volts or so. So, T_1 and T_2 are in saturation. Now, you want to turn off the GTO, so first thing that has to be done is you have to bring that T_2 out of saturation. See in this figure, this is T_1, PNP transistors and this is T_2, NPN transistors, both are in saturation.

Now, device has to be turned off. How do I turn it off? You have to bring this transistor out of saturation. How do I bring this transistor out of saturation? I have to reduce the base current. Now, let us see what is the relationship between the anode current and the gate current that has flowing out of the gate terminal.

See, this expression that we have derived for the SCR is still valid here. The total saturation current is given by alpha$_2$ into I_G plus I_{CBO} is a sum of I_{CO1} and I_{CO2} divided by 1 minus alpha$_1$ plus alpha$_2$. Wherein, alpha$_1$ and alpha$_2$ are common base current gains. We have already defined them for the SCR. When SCR is in on state, we have reduced the gate current to a very small value. So, in on state, I can neglect this term, I_A can be given by I_{CBO} divided by 1 minus alpha$_1$ plus alpha$_2$.

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See here, this is the current that has to be turned off. See, in the previous equation, I_A becomes 0 when the numerator becomes 0. So, when can you make this numerator zero? When, I_{CBO} is equal to minus of alpha$_2$ into I_G, see here. So, the relationship is I_G is equal to minus of I_{CBO} divided by alpha$_2$. So, if I want to find out the gain or the relationship between the anode current and the gate, it comes like this, I_A divided by I_G is equal to alpha$_2$ divided by alpha$_1$ plus alpha$_2$ minus 1.

How do I improve this gain? In other words, how do I make this gain as high as possible? Alpha$_2$ should be as high as possible. What is alpha$_2$? It is a gain of $N_1 P_2 N_2$ transistor. See here, alpha$_2$ for this transistor, this is $N_1 P_2 N_2$. How do I make alpha$_2$ as high as possible? One way is to make the thickness of P_2 layer less. P_2 layer should be very thin. See, that is one of the difference between a SCR and a GTO, I told you the first difference that I told you, layer of P_2 is less compared to a SCR and second is increase in doping level in N_2, thereby increasing the value of alpha$_2$.

Now, how to turn off a GTO? What happens exactly during the turn off process? I_G has reversed, I_G is flowing out of the gate, I_G is connected to P_2. See here, I_G is P_2, now I_G is flowing out of the gate terminal, so holes are extracted from P_2.

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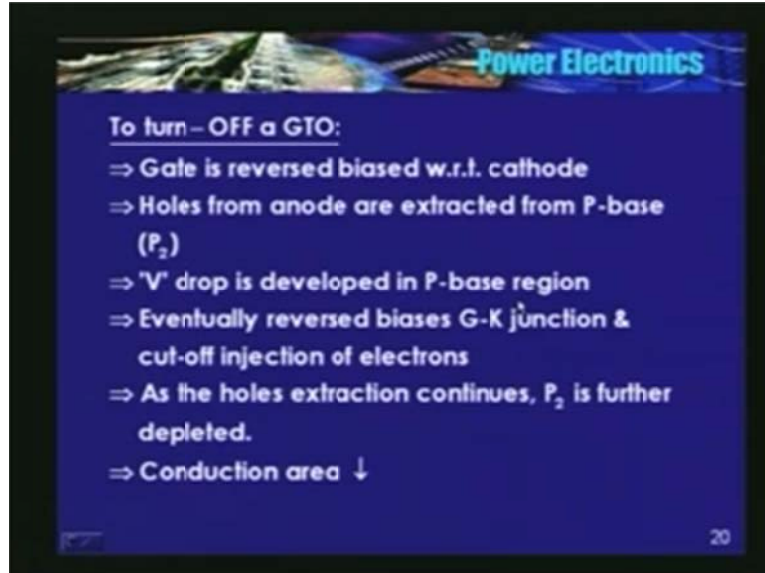
So, as these extractions take place, the voltage drop is developed in the P_2 region. I will tell you holes or holes from the anode are extracted from the P base. So, during this process, voltage drop is applied in P_2 base region and eventually this voltage, reverse biases your gate and cathode junction and both goes into cut off. But then, entire turn off process is not completed as yet. As the holes extraction continues, P_2 is further depleted. See, first is gate cathode junction gets reverse biased but then I_G is still flowing out. So, P_2 gets further depleted. What happens? Conduction area drops. Now, the current may be flowing in the remote parts of the anode or far away from the gate.

Now, it may so happen that the current density in those parts may increase and if this happens there would be a localize heating and device may fail. So, this has to be avoided. See, the figure that showing the turn off process, it is something like this.

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All the holes are diverted towards the gate. The P_2 gets further depleted, now anode current tries to flow through the area which is far away from the gate area. There is a reduction in the area that is available, it may form or in that area, the current density may increase localize heating, eventually device may fail.

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Now, the turn off of a GTO is greatly influenced by the turn off circuit. Unfortunately, turn off gain of a GTO is very low. Turn off gain is very low, could be of the order of say, 6 to 15, generally.

So therefore, if anode current is 100 amperes, by the way GTO is a high current device, high voltage device. So, if anode current is around 100 amperes, gain is of the order of say, 6 to 15. So, gate current that is flowing out of the terminal is 10 amperes and it is fortunately for a very short duration. So, as the gate current starts flowing out of the terminal, for some time anode current remains constant. So, this period is known as the storage time. See in this figure.

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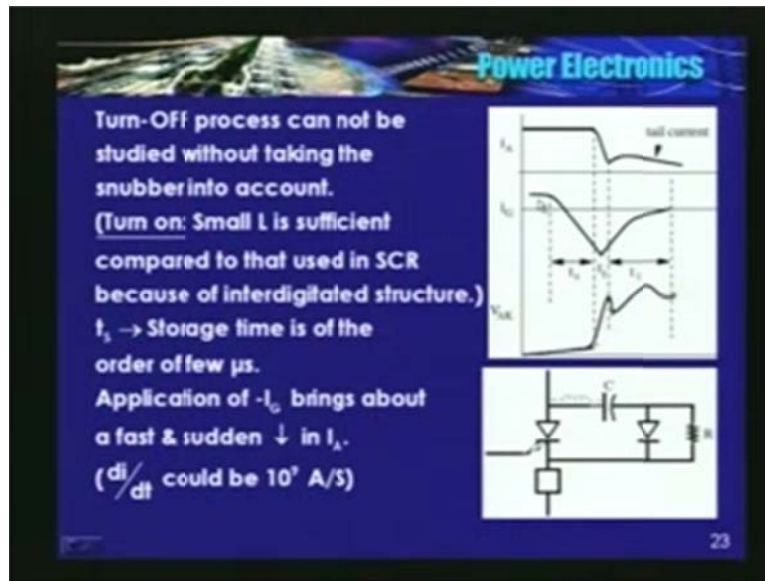
At steady state, gate current has been, we have to reduce the gate current to a very low value. Somewhere at this point, it desire to turn off the GTO. So, I_G reverses, though I_G has reversed, I_A still remains constant for t_s duration. So, this is known as storage time. During storage time, anode current remains approximately constant and this period t_s can last for a few microseconds.

Now, what happens after t_s? This process has to be studied by taking a snubber into account. There has to be a snubber circuit to turn off a GTO. I told you, di by dt rating of a GTO is very high. So, you can use a very small inductor in series with a GTO. We have connected an inductor in series with thyristor to limit di by dt during turn off. Similarly, to limit di by dt, we require a very small inductor. So, the rating of di by dt, even now ... there has to be a turn off snubber, a RC circuit looks like this, something like this.

Now, there is a diode, it has its own turn on time and I have shown a small inductor what is known as loop inductance, in dotted lines. There is a very small inductor in dotted lines. You wanted to turn off the thyristor, so I_G has reversed, for some time I_A remains constant and from t_s onwards, anode current falls at a very fast rate.

Now, because of this loop inductance and because of this diode, turn on time of the diode, this current, anode current cannot starts flowing through the snubber circuit immediately and because of this there is going to be a voltage spike because of the inductance which is there in other parts of the circuit.

If this inductance 0 and turn on time is very small, then may be, immediately this anode current finds a path, the capacitor. Now, because of this inductor and diode, this current gets choked and therefore because of this a large di by dt, this spike appears across the GTO. It could be dangerous, in the sense that device may fail because of this spike.

So therefore, the snubber circuit layout is very important. The loop inductance, the inductance that I have shown in the dotted line should be as small as possible. Snubber circuit layout is very critical in the case of GTO. So, the anode current has fallen to a very low value. So, the end of t_f is known as the fall time and this is very small and from there onwards a current what is known as the tail current, starts flowing through this snubber circuit.

Now, the voltage across the GTO is limited by the dv by dt, it is determined by the dv by dt. Now, what is this tail current? This tail current, that period I_k is equal to zero, cathode current is zero and the gate current is same as the anode current. So, this tail current is corresponding to the free charges, they exist in N_1 layer. The current due to the free charges which exists in N_1 which is nothing but the blocking layer, lightly doped layer. These carriers are numerous and they require a finite time to recombine.

See, the problem here is as the voltage rating increases N_1 layer, the thickness of the N_1 layer increases. As the thickness of N_1 layer increases, time taken for these carriers to recombine also increases. So in other words, the tail current period increases with the blocking voltage capability of the GTO. So, what is the consequence of having a higher fall time or sorry, higher tail time? See, voltage across the device started increasing, current in the device is still finite, the tail current, voltage is a reasonably high value it has attained, so therefore, the losses that are taking place device are high. So, turn off losses in a GTO, they are significant. So, how do I reduce the turn off losses? So, one way to reduce is to reduce the fall or tail current duration. How to reduce the tail current duration? This dt has to be reduced.

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Having decided on the voltage rating, N_1 layer, thickness of N_1 layer gets decided and the tail current depends on the thickness of N_1. Is there a way out? Yes. Why did we do anode shorting? I said one of the advantages of anode shorting is to reduce the turn off time. How does it do? What it does is, see this.

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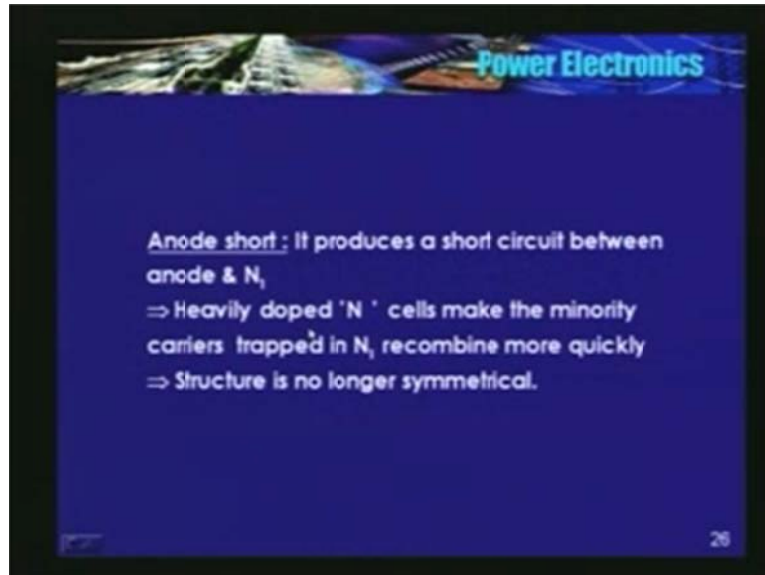
Those anode shorting N layers are highly doped. They were all where N plus, they are highly doped. What they do is this heavily doped N cells, they make the minority carriers trapped in N_1, recombine more quickly.

So this highly doped N cells, they helped the minority carriers trapped in N_1, recombine more quickly. So therefore, your fall or sorry, tail current time reduces. Sorry, it is a tail current time reduces but then devices no longer symmetrical. Now, it can block only the positive voltage. Negative voltage it cannot block. So, with this I will conclude my today's lecture.

Thank you.