Power Electronics

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Lecture - 5

Hello, in my last class I discussed the diode and silicon controlled rectifier, SCR or thyristor. The two important parameters for diode that are to be used in high frequency circuits are; one is reverse recovery time, t_{rr} and the reverse recovery charge or the peak of the reverse recovery current. Now, what is reverse recovery time? It is a time between the negative 0 crossing of the current to 25% of the peak of the reverse recovery current.

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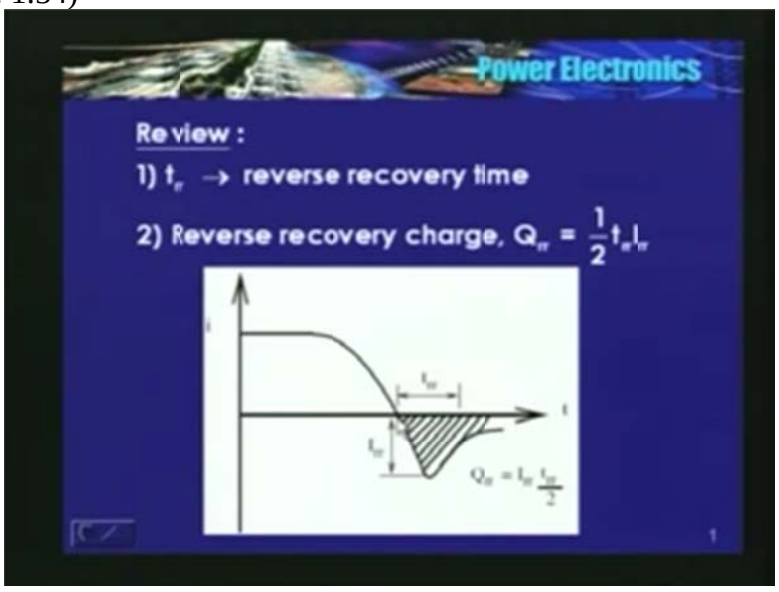

See, it is here, it is t_{rr} the time between the negative 0 crossing to say 25% of $i_{rr,}$ peak rr and reverse recovery charge is the area, the shaded area here. We are considering, we are assuming that this is the triangle area of the triangle i_{rr} into t_{rr} divided by 2. Remember, diode does not turn off when the current become 0 from positive value. It will become 0, it continues in the negative path also. So, t_{rr} is an indication of the maximum frequency at which the diode can operate.

Now coming to SCR, the silicon controlled rectifier is a minority carrier device. There are 4 layers P_1 N_1 P $_2$ $N_{2.}$ P_1 is anode, N_2 is cathode and P_2 is gate. So, there are 3 junctions; $J_{1,}$ $J_{2,}$ J_3 and N_3 is a very thin layer highly doped, P_2 is slightly thicker also the doping level is less compared to $N_{2.}$ N_1 is the thickest among all the 4, doping level is minimum there and p_1 is same as $P_{2.}$ So, therefore J_3 or the reverse voltage that j_3 can block is very small. I will repeat, the reverse voltage that junction J_3 can block is very small. So, when the device is forward biased, in other words B_{AK} is positive, junction J_1 and J_3 are forward biased and J_2 is reverse biased.

Yesterday I showed you the SCR characteristics. There are 3 zones in the forward bias mode, one is forward blocking mode, V_{AK} is positive, I_G or device current is very small. It is stable.

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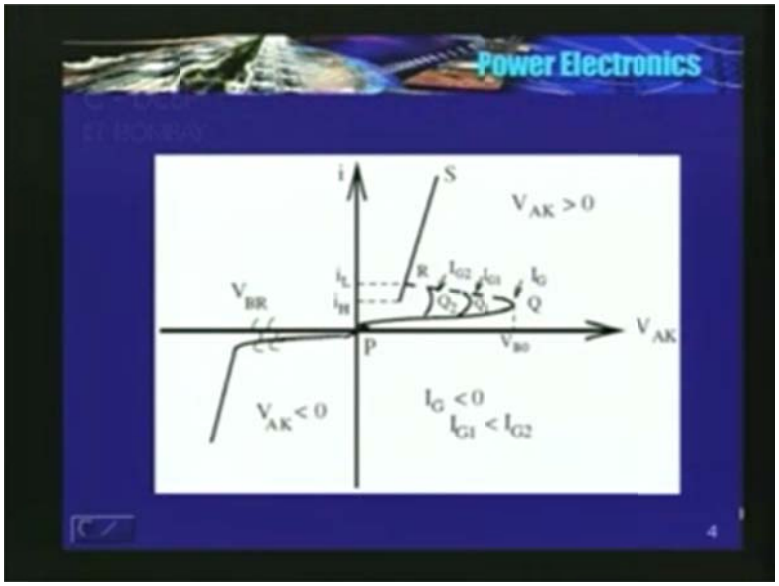

See here, from p to q is a forward blocking mode, a very small current that is flowing is a leakage current. So, if I_G is 0 and if the applied voltage is higher than the break down voltage of junction J_2 that is V_{BO} appears across junction J_2, J_1 and J_2 are, J_1 and J_3 are forward biased. Device goes into conduction mode. Which path it takes? It takes QR, it is unstable because it is a negative resistance zone. Having gone into conduction mode, current is limited by the load. Current is determined by the load. So, again it is a stable mode of operation, forward blocking mode is a forward, again a stable mode of operation. So, I told you that is a finite I_G or as I_G increases the break down voltage of junction J_2 goes on reducing. In other words, you can reduce the voltage at which device goes into conduction mode by supplying the gate current. So, that is about when the device is forward biased or the operation in the first quadrant. What happens when the device is reverse biased?

The applied voltage should be less than $V_{BR.}$ In the reverse bias mode, junction J_1 and j_3 are reverse biased, j_2 is forward biased. Reverse voltage that a junction J_3 can block is very small. Therefore, the entire reverse voltage appears across junction $J_{1.}$ So, the V_{BR} is an indication of the break down voltage of junction $J_{1.}$ So, in any circuit the V_{BR} or maximum reverse voltage that appears across the thyristor should be less than the V_{BR} rating of the SCR.

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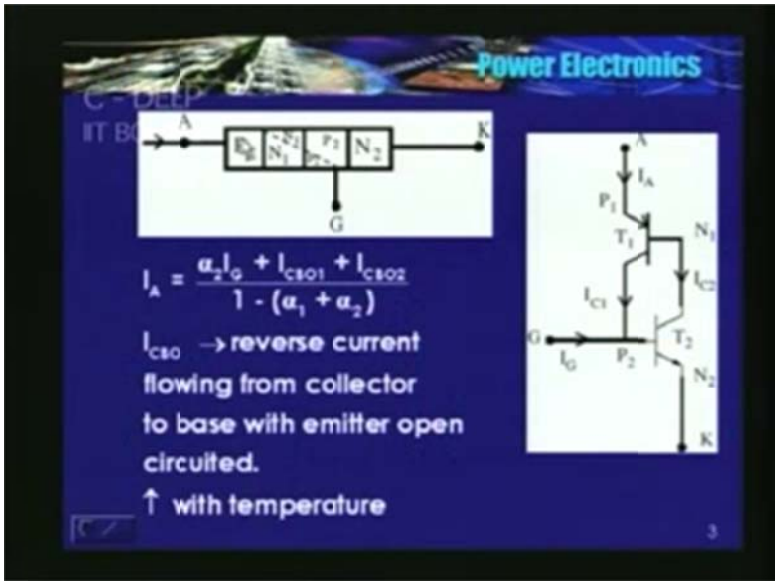

Now I started explaining two transistor analogy, I said there are two transistors $P_1N_1P_2$ and N_1P_2 N_2 then we derived the expression for I_A anode current in terms of gate current and the leakage currents I_{CBO1} and $I_{CBO2.}$ What is I_{CBO1}? It is a reverse current flowing from collector to base with emitter open circuited. This aspects, we have studied in transistor course. I_{CBO} is the reverse current flowing from collector to base with emitter open circuited. Remember, it is very strong function of temperature, it increases with temperature, it could approximately be doubled for every 10 degree rise in the temperature.

See, I_{CBO1} increases with the temperature. What are $alpha_1$ and $alpha_2$? They are common base current gain approximately equal to I_C divided by $I_{E.}$ $Alpha_1$ increases with $I_{E.}$ So, what happens for a transistor T_1? $Alpha_1$ increases with $I_{A.}$ Why I_A? I_A is nothing but the emitter current of transistor $T_{1.}$

Similarly, $alpha_2$ increases with the cathode current of the thyristor. Why cathode current of the thyristor? It is an emitter current of transistor $T_{2.}$ What is the relationship between anode current and cathode current of the thyristor? Cathode current is the sum of anode current plus the gate current. Yesterday we have derived that equation.

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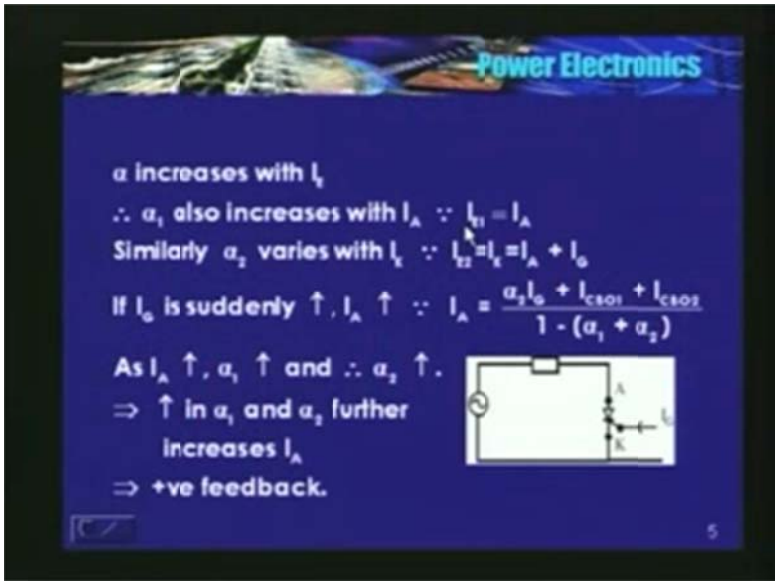

See here, I_{E1} the emitter current of transistor T_1 is anode current itself. $I_{E2,}$ the emitter current of transistor T_2 is a cathode current that is sum of I_A plus $I_{G.}$ This we have derived yesterday. Now, what happens with a finite I_G? A pulse of current is applied to the gate circuit. If I_G increases I_A also increases. Here is the expression, I_A is equal to alpha$_2$ into I_G plus I_{CBO1} plus I_{CBO2} by one minus alpha$_1$ plus alpha$_2$. So if I_G increases suddenly, I_A increases. Now, if I_A increases, alpha$_1$ increases. I will repeat, I said alpha increases with $I_{E,}$ the emitter current. The emitter current for upper transistor is nothing but the anode current $I_{A.}$ I told you that if I_G increases I_A increases, this is from the expression that we have derived yesterday. So therefore, if I_A increases alpha$_1$ increases. If I_A increases alpha$_2$ also increases because the emitter current of transistor T_2 is a sum of I_A plus $I_{G.}$ So, if this current increases alpha$_2$ also will increase. So, increase in alpha$_1$ and alpha$_2$ will further increase $I_{A.}$

See this is this expression. Since I_G increases suddenly, that increases $I_{A.}$ Now, since I_A is increased, alpha$_1$ increases and therefore alpha$_2$ increases. So, that results in again increase in I_A because both alpha$_1$ plus alpha$_2$, they have increased, denominator decreases. Therefore, I_A increases. This is some sort of a positive feedback. So initially, because I_G is increased, I_A increases. I_A increase will result in increase of alpha$_1$ and alpha$_2$. That again increases $I_{A.}$ Some sort of a positive feedback, you would have studied in your control theory class. Only may be in oscillators, we use this positive feedback. Almost all the other systems, we use negative feedback to stabilize it.

So therefore, due to the positive feedback, a small I_G will result in a large I_A here, the anode current. So, when alpha$_1$ plus alpha$_2$ approaches 1, because the equation says I_A becomes infinity, of course that equation is not valid when alpha$_1$ plus alpha$_2$ equal to 1, because the maximum value of anode current is determined by the load. Hence, a small $I_{G,}$ a gate current results in large anode current here.

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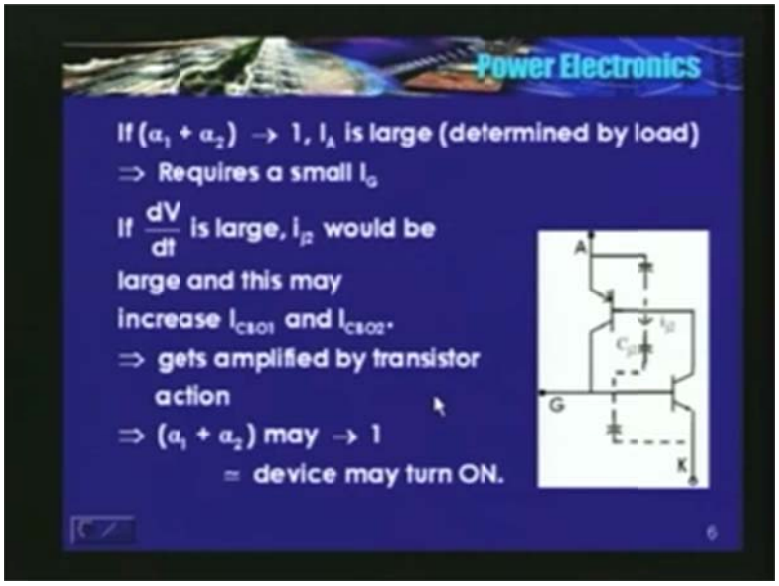

So, this is one of the ways to trigger the thyristor. What is the condition? If there is a finite I_G to trigger the thyristor, I_G should be present till the current through the device is equal to or higher than the latching current.

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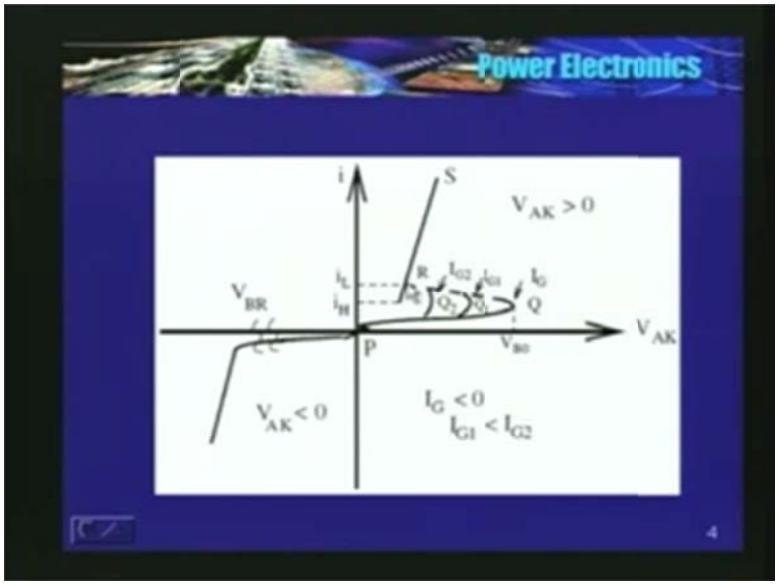

See here, the latching current, this is the latching current, I_L. Having gone into conduction mode, gate has no control. To turn off the thyristor, the device current should be reduced to a value which is less than the holding current and holding current is always less than the latching current. It is like this, without holding, how can you latch? So, this is the way to remember. Now, what happens if there is a large dv by dt across the device?

You are forward biased the device, a large positive dv by dt is appearing across it, so just see this figure (00:16:22), transistor analogy. Now, there are junction capacitors, there is one capacitor between emitter and base of T_1 base and again collector of T_1 and so on. Now, if there is a large dv by dt, I_{j2} will increase. I_{j2} will increase because of this dv by dt and because of this capacitor $C_{j2,}$ I_{j2} will increase

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Now, this will result in the higher leakage current I_{CBO1} and I_{CBO2} and this current gets amplified by transistor action. Now, if they get amplified by transistor action and if $alpha_1$ plus $alpha_2$ approach 1, device will turn on. So, it is not only a positive I_G will trigger the thyristor, in case, if you apply a large dv by dt, a positive dv by dt across the device, it will go into conduction mode without $I_{G.}$ That is because of the junction capacitors.

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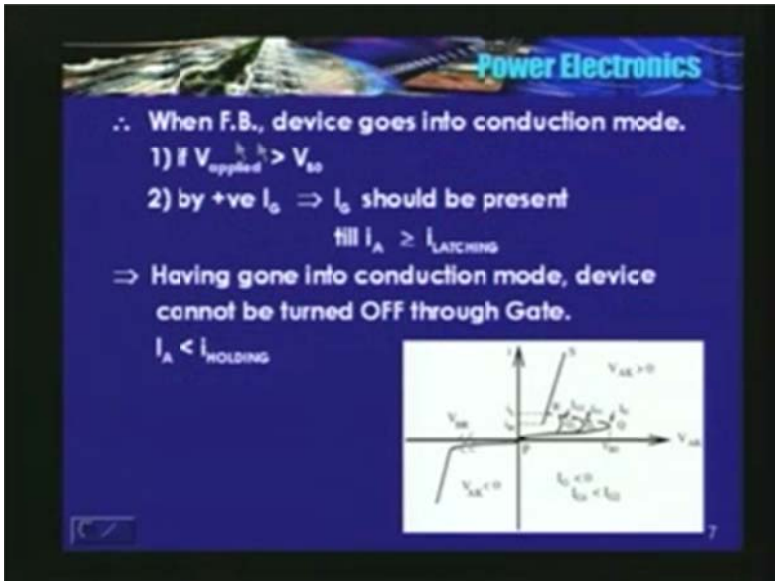

So for summarizing, when the device is forward biased, device goes into conduction mode if applied voltage is higher than the forward break over $V_{BO,}$ if there is no gate current $I_{G.}$ By, positive I_G also you can trigger the device. But I_G should be present till the anode current is higher than the latching current. The third way to trigger the thyristor is a large dv by dt applying across the device. This is another way of triggering the thyristor also or thyristor main to conduction mode because of the temperature effect.

I told you that I_{CBO1} and $I_{CBO2,}$ these are the strong function of the temperature. They double for, they approximately double for every 10 degree rise in temperature. So if they increase, this will result in increase in $alpha_1$ and $alpha_2$ and in case, $alpha_1$ plus $alpha_2$ approach 1, I_A increases and device again goes into conduction mode. There is yet another way of triggering the thyristor, by direct light radiation.

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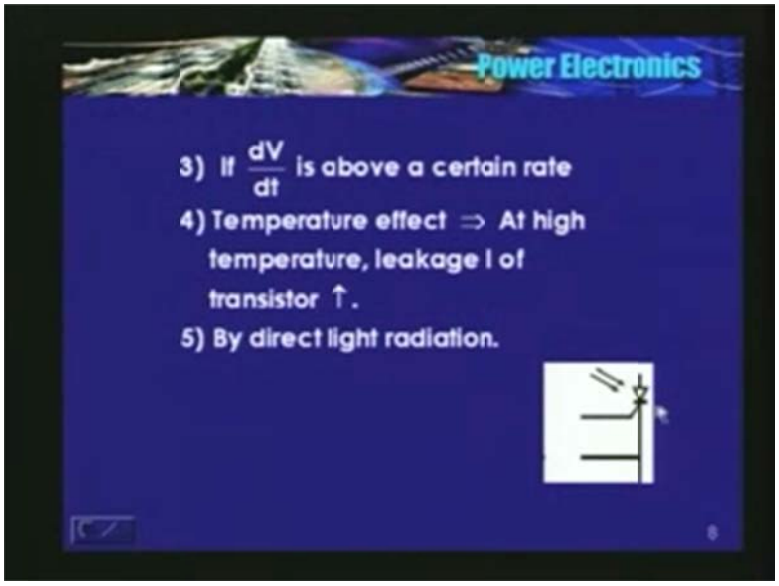

See here, I am radiating light in the junction, to this junction light is being radiated. Definitely, that will increase a junction temperature, leakage currents will increase, they get amplified and thyristor goes into conduction mode. So this method, the last one is used in high voltage applications because as the voltage level increases, it may be difficult to pass the gate current through the conventional wires, lead wires.

So, you trigger the thyristor by the direct light radiation, this is used in high voltage dc transmission, HVDC. What exactly the HVDC is? We will see sometime later. So, one of the ways or thyristors are triggered by direct light radiation HVDC systems. So, that is about various ways of triggering the thyristor or thyristor goes into conduction mode if 1 of the 5 conditions are … (00:21:18)

Now, what about the switching characteristics? In the forward blocking mode, when I_G starts flowing, immediately device will not start conducting. There is a finite time delay before device current builds up, what is known as the delay time, t_d. See here, somewhere at this point, a gate pulse is applied.

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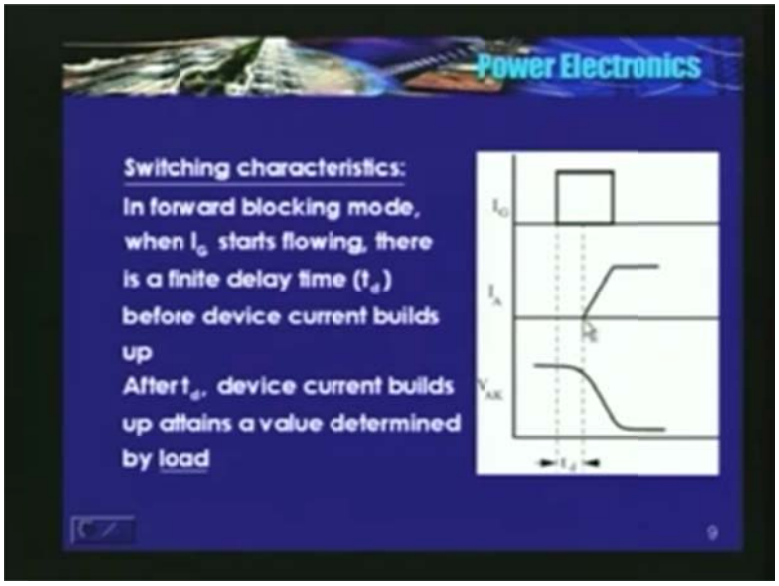

See, there is a finite time, only after which the anode current starts increasing. Again this current, increase in current is determined by the load, this nearby dt and attains a value given by, not determined by the load. Again here voltage V_{AK} starts decreasing and attains a very low value which is approximately say 1.5 to 2 volts.

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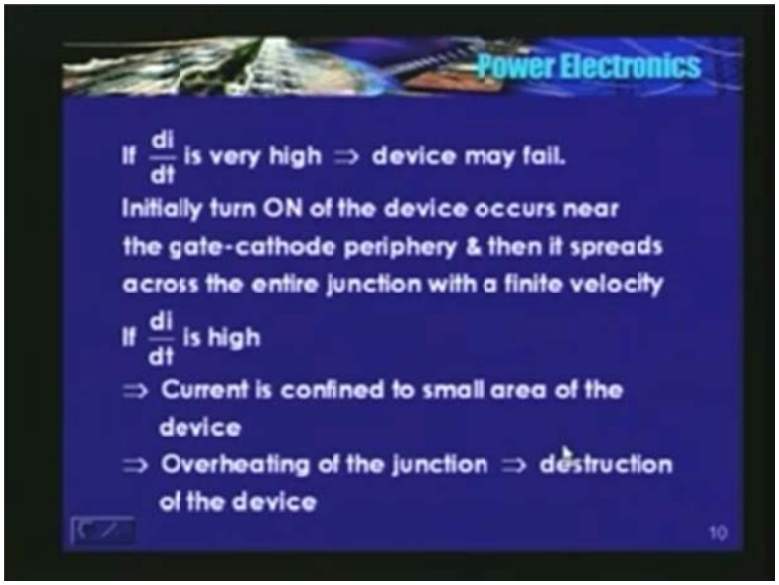

Now, what happens if rate of rise in current is very high? If di by dt is very high, device may fail. Why it will fail? See, during the initial turn on that occurs, the initial turn on occurs near the gate cathode periphery. Initially the device was blocking, now it starts conducting and it is confined to near gate cathode periphery and it slowly spreads with a finite velocity to the entire junction.

Now in case, di by dt is very high, I told you the conduction is confined to a very small area, gate cathode periphery in the beginning, current is increasing at a very fast rate, so definitely there will be hot spots or over heating of the junction. So, if there are hot spots or over heating of the junction, it may, device may get damaged. So remember, see it is here, I have written. Initial turn on the device occurs near the gate cathode periphery. Before the turn on, device is blocking and then it spreads with the finite velocity across the entire junction.

Now di by dt is high, there is a very small area that is available, current is confined to a small area, so definitely there will be hot spots or over heating of the junction and therefore the junction or the device will fail. So therefore, during turn on, di by dt has to be controlled. How to control this di by dt? We will see some time later. Now what happens once the device has gone into conduction mode? J_1 and J_2 were, sorry J_1 and J_3 were forward biased, J_2 was blocking, now there is the junction J_2 breaks down, now it is highly saturated with minority carriers. Remember, I will repeat, J_2 is saturated with minority carriers. See, it has a very special effect, the reverse recovery current in a diode and because of minority carriers, they require a finite time to recombine or to get neutralized. Definitely, similar effect will be there in the thyristor. I will discuss it sometime later. Now, since J_2 is highly saturated with minority carriers, gate as no further control. That is the reason I have been saying that having gone into condition mode, you can withdraw the gate.

In fact, one should withdraw the gate signal because if the gate current is continuously flowing, it has no control but then it will amount to power dissipation in the junction J_3 and because of temperature arise, it may fail. Of course, it has a maximum power dissipation capability. So that is about the conduction mode.

Now, how do you turn off the device? For turning it off, one has to reduce or current through the device should be reduced below the holding value. Now, if the input is AC, beyond pi, voltage will become negative. Input voltage becomes negative. So, there are chances of current also reducing and becoming 0. If the input is DC, having triggered the thyristor and gone into condition mode, how will you turn off the device?

So, device can be turned off by temporarily applying a negative voltage with other L and C elements or in other words you have to reverse, you have to apply a reverse voltage across the device. What happens? I_A starts decreasing, becomes 0, it continues to conduct in a negative direction, all most same thing that are happened in the diode.

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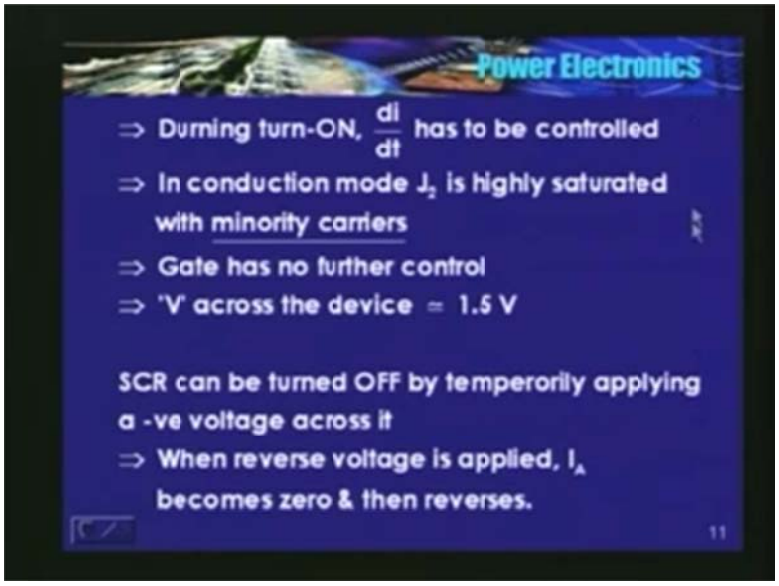

See here, whatever you can take down this explanation, this is about the turn on process. J_2 is highly saturated with minority carriers, gate has no control. Then, SCR cannot be turned off or can be turned off by temporarily applying a negative voltage using or in addition to L and C may be or only L, it depends.

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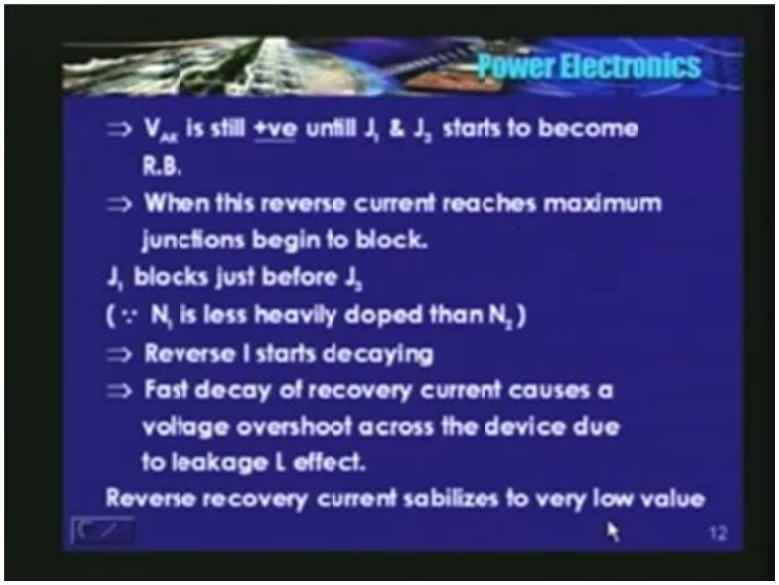

Now, V_{AK} is still positive, till junction J_1 J_3 starts to become reverse biased. Now, when the reverse current has reached a peak, something known as $I_{RR,}$ you have seen in a diode, when this reverse current which is a peak, junctions begin to block both J_1 and $J_{3,}$ they begin to block. Then, first J_1 blocks and then $J_{3,}$ I will repeat, when the peak, when the reverse current has

attained a peak, negative peak, both junctions, they begin to block. J_1 blocks just before J_3. Why J_1 blocks just before J_3? Junction J_3 or N_3 is highly doped, where J_1 is between P_1 and N_1 and N_1 is less heavily doped compared to N_2. So, J_1 blocks first, then J_3 blocks.

When this happens, reversed currents starts decaying. Now, this fast decaying current, a reverse current, will cause a voltage over shoot across the device due to the leakage conductance effect. See, I will repeat that the reverse currents starts decaying towards 0 now and this fast decay of recovery current causes a voltage over shoot, L di by dt effect across the device due to the leakage inductance effect that due to the stray inductance and this reverse recovery current, I said decays and it attains a very low value. This process is almost the same as the diode. There we had only one junction, here we have two junctions.

By the way, J_2 is still forward biased because there were large numbers of minority carriers. That is the reason, gate as no control having gone into conduction mode that is what I told you. Now, they require a finite time to recombine or to get neutralized and this takes considerable amount of time. See this part is for not there. See, I will explain to you with the figure.

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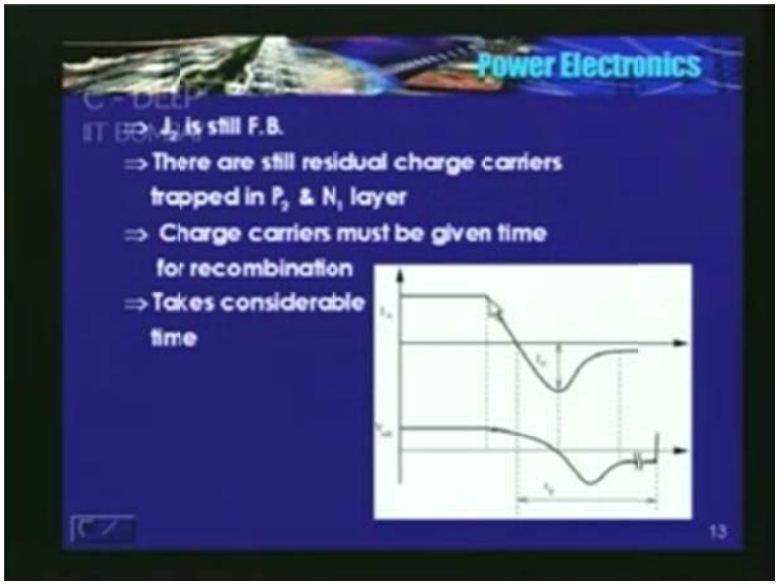

Anode current starts decreasing, V_{AK} is still positive, it becomes 0, V_{AK} starts falling. This, I_{RR}, the negative current or the reverse current attains a peak value of I_{RR} and this value is much higher compared to that for diode and once J_1 and J_3 have blocked, this current starts decaying fast and it attains a low value but then junction J_2 is still forward biased. There are still residual charge carriers in that junction. They take a considerable amount of time.

So, therefore SCR should not be forward biased or positive voltage should not appear across the thyristor till junction J_2 has attained the blocking mode, forward blocking mode. J_1 and J_3, they were attained the blocking mode, J_2 is still forward biased because there are minority carriers, they have to recombine, it takes considered amount of time. Till this occurs or till this processes is completed, positive dv by dt should not be applied across the thyristor because J_2 as not

attained a blocking mode and in case if you apply a positive dv by dt device will go into conduction mode. So see, this is time period t_q. What exactly t_q I will define. See, at this point I have broken, this just indicates that this is a break because this time could be significant and from there I am not, positive voltage or SCR, a positive voltage appears across the thyristor.

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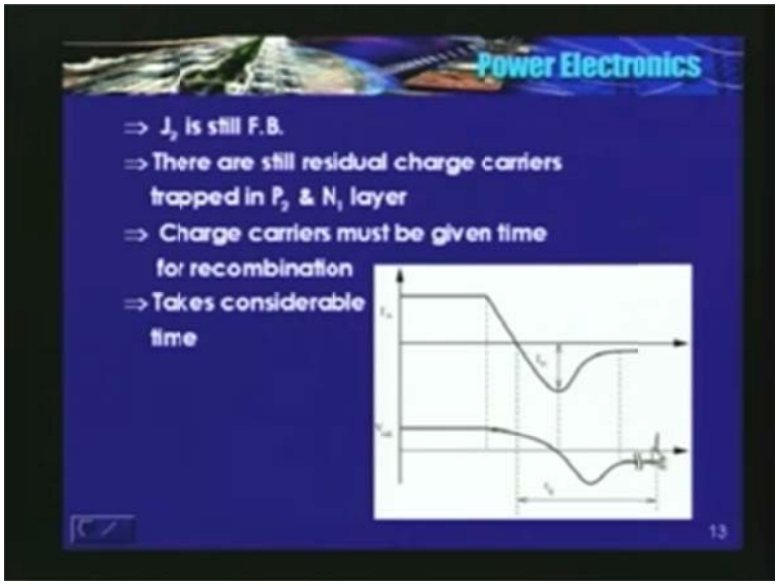

Now, what is t_q? It is a minimum time interval between on state, I_A current becomes 0. See here, I_A current, the anode current has become 0 and the instant when thyristor is capable of withstanding forward voltage, without turning on. See the instant of current becoming 0 and it is capable of withstanding forward voltage without turning on. In case, dv by dt becomes positive here and it becomes if the SCR is getting forward biased somewhere here, it will turn on because J_3 is not attaining the blocking mode. So, this has to be ensured.

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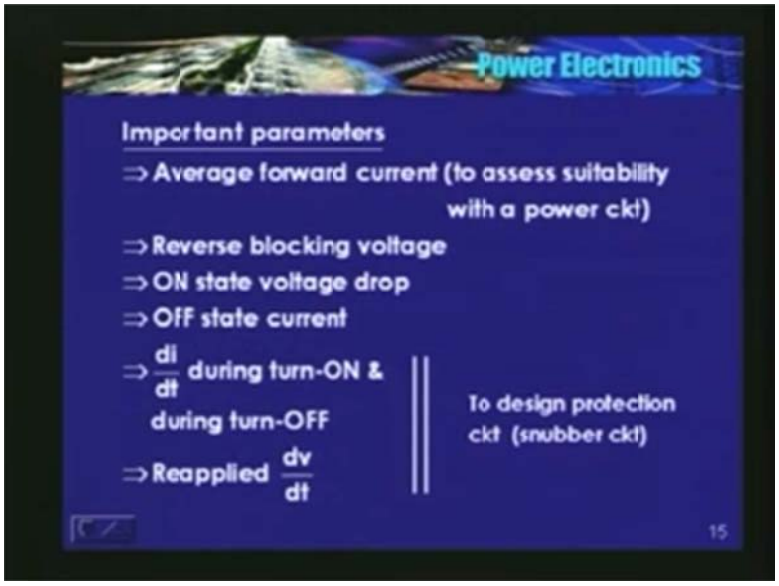

Now, what are the important parameters with the thyristor? Similar to diode, average forward current to assess its suitability with the power circuit, same thing as in the case of diode, reverse blocking voltage same like diode, constant voltage drop to determine the heat sinks, di by dt during turn on and during turn off. Why during turn off? You have to apply a negative voltage, you have to reverse bias it, only you are or in other words, forcibly you have to apply negative voltage across the thyristor to turn it off. Somehow, you have to reduce that current if it happens naturally, it is fine. It may happen naturally sometime, it we will see. In certain applications current may go, become 0 and thyristor will turn off its own and if the input is DC, you have to turn it off forcibly.

Again, another important parameter is reapplied dv by dt. See here, these are the average forward current, reverse blocking voltage to assess the suitability with a power circuit, on state voltage drop, off state current. Again these 2 to calculate the heat sinks or to determine the heat sinks sides. di by dt turn on or during turn on and during turn off and reapplied dv by dt. These 2 are required to design protection circuit, what is known as a snubber circuit. I will come to that sometime later. Snubber circuit which protects the device against di by dt and dv by dt, how I will explain to you.

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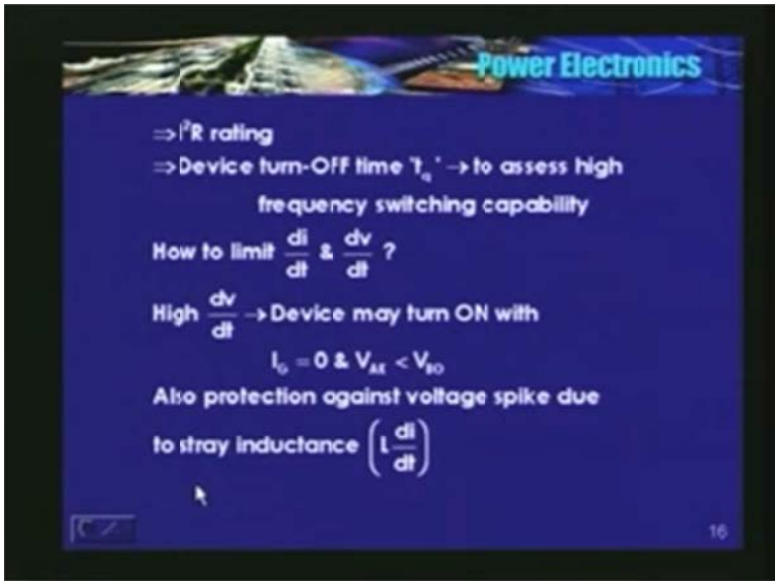

I square R rating similar to diode and again device turn off time t_q to assess high frequency switching capability, the important parameter. Now, how do I limit di by dt and dv by dt? I had explained to you that because of the J_2 junction capacitance if there is a large dv by dt, device will go into conduction mode. Also, voltage across the thyristor should not exceed its rate or in other words device should be protected if there is a spurious spike that could happen whenever if there is a di by dt and there is always some strained attains.

See I will repeat, there is always some strained attains in the circuit and if there is di by dt, L di by dt is a voltage spike that may appear across the thyristor. So, in addition to the normal supply a large voltage spike could damage the thyristor because all that devices, there is a voltage limit, there is a current limit and there is a power limit. I have told you that at any given time operating point should lie within SOA, safe operating area.

So, how do I address these two issues or which passive element will I use to suppress or to control the rate of change of voltage? Naturally use a capacitor. Can I directly use the capacitor? No, you use a resister and a capacitor. See, the other day I told you that resister should be avoided for higher frequency. Here it may be required, no choice.

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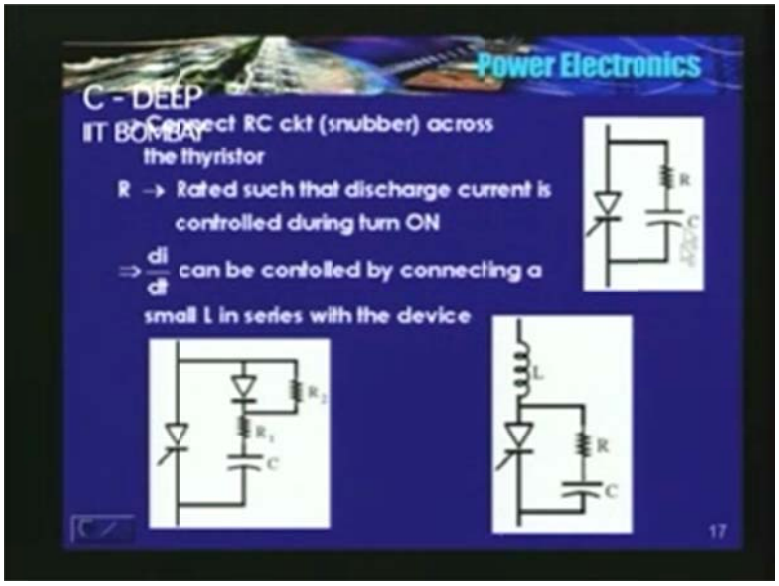

So, one way to control dv by dt is to have a RC snubber, snubber circuit. Now, it does not allow, we know that capacitor does not allow instantaneous voltage change. So, what happens? When you turn it off, whatever the current that was flowing, it starts flowing through this circuit. Assume that initially the thyristor is on, so voltage across this is as slow as 1.5 or 2 volts. A current was flowing through the device determined by the load, now you want to turn it off. Now, what happens? All the current that was flowing, starts getting diverted here and capacitor starts charging. Capacitor voltage will increase and that voltage is nothing but voltage across the thyristor.

So, by controlling or by choosing suitable value of R and C, you can control the rate of rise of voltage across the thyristor. See, there are other combinations also. See here, I have used a diode and 2 resistors. Why am I using 2 resistors and a diode here? Now, what happens in this circuit? Now, when you turn on the device again, whatever the charge stored in the capacitor, it will be transferred to the load. In other words, capacitor has to discharge. So, capacitor will discharge in this way. Now, if there is no resistor or if the resistor is very small, what happens is the discharging current in addition to the others, current will flow through the SCR.

See, in addition to the load current and this could be the reverse recovery current of other devices, again it depends on the circuit configuration that capacitor discharge current also device has to carry. So, R should be rated such that discharged current is controlled during turn on, discharge current should be controlled during turn on.

So in this combination, what happens is only R_1 comes in series during the charging of the capacitor or during the turn off time, during the turn off time because R_2 is bypassed by this diode. So, current starts flowing through D_1 $R_1$and C, during charging or during turn off time of SCR and during turn on, capacitor R_1 R_2 and maybe, you would like to reduce the current that is flowing during turn on, because we have to control di by dt anyway. So, this is, this or this is considered as the turn off snubbers.

Now, how do I control di by dt? Now, should not allow a fast rising current through the device. Which passive element will I use? Definitely, we need to use an inductor, a small inductor you connect it in series as shown in this figure. This will not allow a fast rising current. So these two, L and RC will protect the device against di by dt as well as dv by dt.

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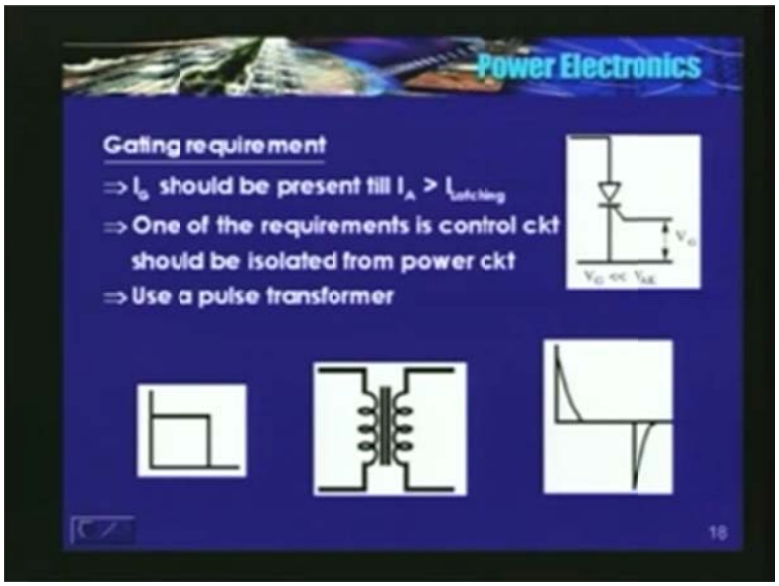

How about the gating requirement? I will just briefly touch up on these issues. Similarly, there are various types of snubbers or protective circuits. Now, I_G should be present till the anode current is higher than the latching current that is essential. I told you that anode and cathode, they come in series with the load and gate is, gate control element is the gate element, a gate control signal is applied, gate and the cathode terminal. The voltage that is required is very small.

So, if you see in this circuit $V_{AK,}$ not during conduction, not during on time, this could be very high and this is very low, please V_{AK} is not during the on time, the voltage that is appearing across the thyristor, the forward blocking mode or when it is reverse biased, its completely determined by the other circuit here, power circuit.

So definitely, we need to isolate the control circuit from the power circuit. This is one of those features, you isolate the control circuit from the power circuit. Now, how do I isolate the control circuit from the power circuit? One way to use is what is known as a transformer. The transformer that is used in gate drive circuit is known as the pulse transformer. Why it is a pulse transformer? It has to just pass the pulses.

See here, I have just shown a transformer here. If I give this sort of a wave form to the primary of the transformer, what happens? Transformer is nothing but a differentiator. So, I will get only a pulse at the rising edge and at the falling edge. After all, this works as a differentiator. There is d phi by dt and there is d phi by dt. So, there is only during d phi by, if the d phi by dt is there only, there is a voltage induced here.

It so happens that transformer may get saturated in this region and if transformers get saturated in this region there is no d phi by dt and therefore no voltage. So, I assume that transformer gets saturated in this region. So, there is a sharp pulse here and there is another sharp pulse here. But then, SCR requires a gate pulse till the current through the device is higher than the latching. So, even if I keep a broad pulse here, at the output I get just 2 sharp pluses.

Now, how do I address this issue? I have to provide isolation. In order to provide isolation, I need to use the transformer. Transformer is nothing but a differentiator. Through a dc, I get a sharp pulse here and a negative sharp pulse at the falling edge. So, even if there is a broad pulse, I get 2 sharp pulses. So, that was the negative sharp pulse that should be blocked because J_3 has a very low reverse break down voltage. So, I have to block negative gate pulse and I have just sharp pulse in the positive. So, what is being done is instead of having 1 broad pulse, you have series of pulses and use this circuit.

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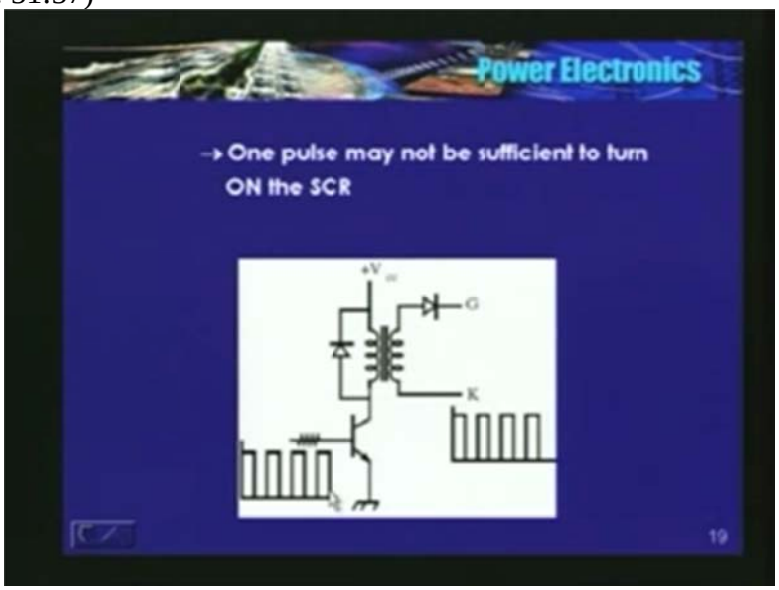

There is a pulse transformer, this pulses are applied to the base of the transistor. These are very narrow pulses, they are very small pulses. So, I am assuming that transformer will not get saturated. So, they are reproduced in the secondary, same pulses. See, transformer is an inductive circuit. Transistor is on during this period and is off during this period. When the transistor is on, current are flowing through the transformer.

So, inductive circuit, current, you cannot break the inductive circuit but then when you open the switch at this point, you have to provide a path for the magnetizing current that is flowing, that was flowing during this period. So, you connect a transistor across the inductor. See, generally a small resistor is also, people connect here. I am not connect a resister because I am assuming that winding has some resistance and in addition you may connect some load resistance in the emitter circuit or in the collective circuit, it all depends on $V_{CC,}$ the resistance of the winding and the frequency of this pulses. I told you, there will be negative spike in the secondary at the falling edge of the signal. So, I am using this diode to block that negative spike. Only apply a large

number of series pulses. We require large number of series pulses because if the load is highly inductive, with one pulse thyristor may not turn on.

See, there are various types of loads and gating requirement depends strongly on the type of loads. It does not depend only on thyristor. After all, current through the device, is determined by the load. So, gating requirement also varies with the load. So invariably, a high frequency gating pulses are used to trigger the thyristor in general. But then, in our entire analysis, we will assume that 1 sharp pulse will trigger the thyristor.

See I will repeat, gating requirement is a strong function of load because anode current is determined by the load and gate pulses should be there till I_A is equal to I latching. So invariably, high frequency gate pulses are applied, but then for our analysis, we will assume that a sharp pulse is sufficient to trigger the thyristor. So, with that I conclude today's lecture. More on this, we will see in our next class.

Thank you.