

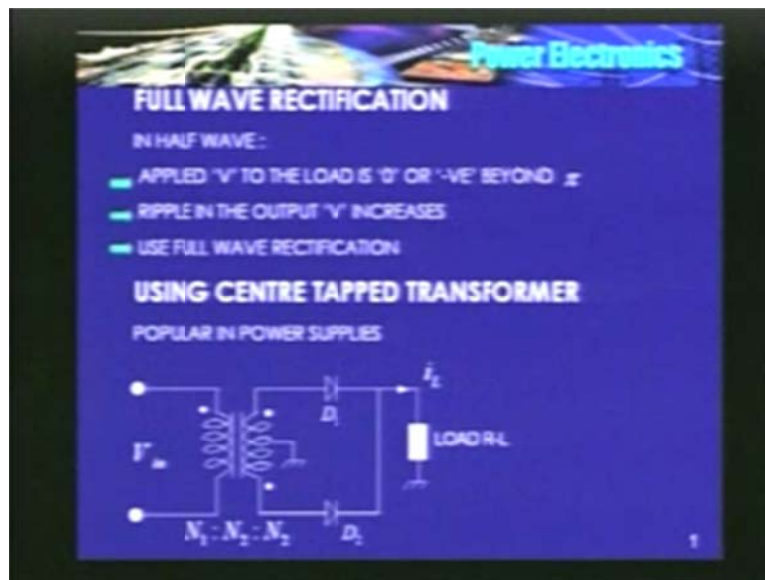
Power Electronics
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Lecture No - 11

Hello, in the last class we discussed half wave uncontrolled rectification. What are our observations? There was 1 diode in between the source and the load. We found that, as the load inductance increases, the duration for which the diode conducts also increases. But then, voltage applied to the load becomes negative.

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Therefore, the rate at which the current decays will so increase. Instead, if we connected diode across the load, beyond π , this diode connected across the load which is also known as freewheeling diode starts conducting. Now, the voltage applied to the load becomes 0. Current decays slowly.

What was the third point that we discussed? When the diode is on, the load voltage is the same as the source voltage. It is independent of type of load. You can have a RL or RLE, whatever may be the type of load, load voltage is same as the source voltage and when the diode is off, the load voltage **is**, depends on the type of load. If it is a passive load, voltage is 0 and if it is an active load, in the sense, if there is a battery, RLE type of load, voltage applied to the load is now E.

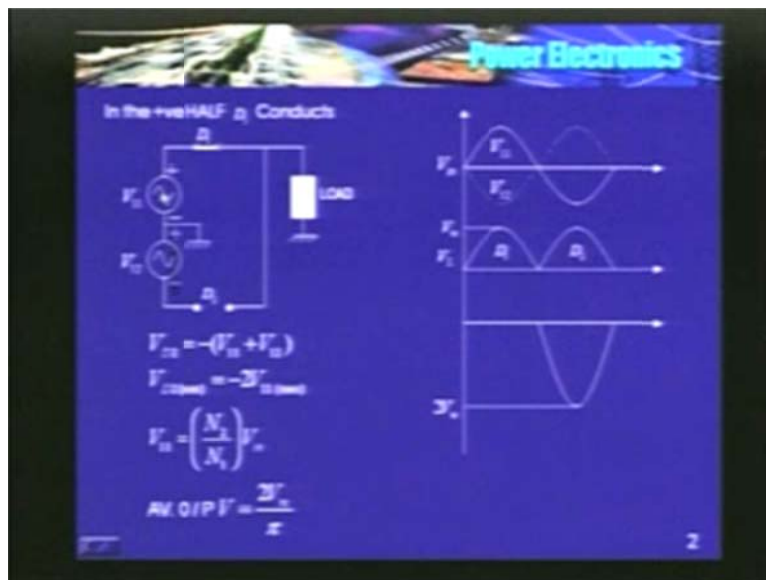
The 4th important point that we found was, if the current is discontinues and if there is a RLE type of load, diode starts conducting when the instantaneous value of the input voltage is equal to E. In other words, α is $\sin^{-1} E / V_m$ and if the load current is continuous,

diode starts conducting at the positive 0 crossing. I will repeat, if the current is continuous, diode starts conducting at the positive 0 crossing. It is independent of type of load, even if you have E there, it does not matter. It is because of $L \frac{di}{dt}$, voltage across the inductor changes and that voltage forward biases the diode.

So in half wave rectification, applied voltage to the load is either 0 or negative, beyond π . Other than, whatever 2 point that we discussed, there is a reduction in output voltage, also the increase in the current decay, ripple in the output voltage increases. So instead, we will see what happens in the full wave rectification.

A very popular pass circuit which is used in power supplies using a centre top transformer with primary number of turns N_1 N_2 and here N_2 , 2 diodes, cathodes are tied together and the load is connected between the common point and the ground, this point and this point is same.

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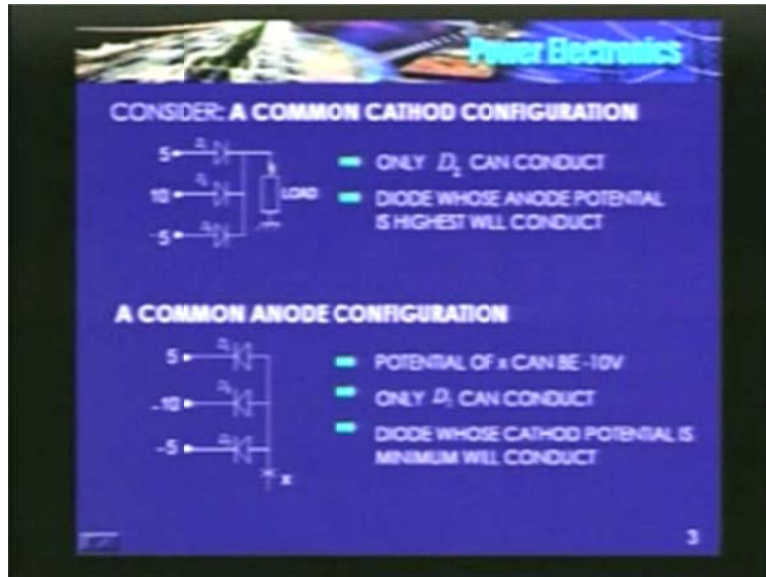


When the instantaneous, when this point is positive ... this is also positive, this also will be positive. So in the positive half, D_1 conducts and in the negative half, D_2 conducts. So, what is the equivalent circuit when D_1 conducts? V_{11} is the voltage induced in the upper half of the transformer. In the, V_{12} is the voltage induced in the lower half of the - secondary of the transformer. When the D_1 conducts, since the cathodes are tied together, this point gets connected to the cathode of D_2 . So, what is the voltage that is appearing across D_2 ? Of course, KVL last hold good, it is minus of V_{11} plus V_{12} .

So, what is the maximum voltage that is appearing across the load? It is minus $2 V_{11}$ max where V_{11} is N_2 by N_1 into V_m or the peak, twice the peak of the secondary voltage that is appearing across the load. Diode should be able to with stand twice the V_m . Average output voltage is given by $2V_m$ by π . Remember, in half wave rectification it is V_m by π .

Now there is an increase in the voltage, $2V_m$ by π . I am not going to discuss about the RMS value, ripple value. I have told you the procedure how to find out, you follow the same procedure. Let me repeat, I will use minimum number of differential equations. Most of the time I will use a graphical approach; writing a differential equation, solving, I think anyone can do it.

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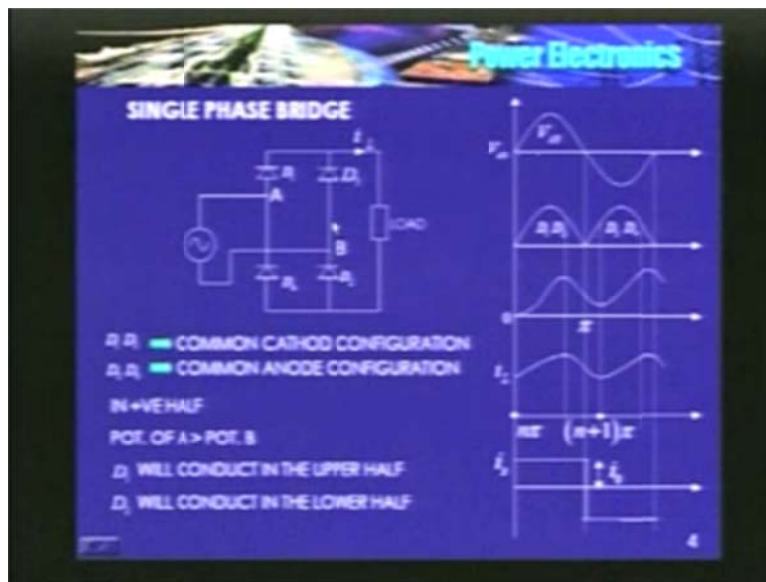
Now, consider a common cathode configuration. What do you mean by common cathode configuration? I have large number of diodes whose cathodes are connected together and there is load here and I have given various potentials to the anodes. Now, which one of them will conduct? There is a plus 5 volts, plus 10, minus 5. We know that we cannot have a situation where in a positive voltage appearing across the load, sorry, appearing across the diode. The moment the voltage across it is 0.7, it conducts.

Assume that D_1 conducts. If D_1 conducts, cathode potential becomes 4.3 and if I consider it to be an ideal, it becomes 5. Then, what happens to D_2 ? Anode potential is 10 volts, cathode is ten 5. So, voltage appear voltage across the diode is 5 volts, you cannot have that situation. So therefore, D_1 cannot conduct. Only D_2 can conduct because if D_2 conducts, cathode potential becomes 9.3 or so or 10 itself. D_1 gets reverse biased, cathode is 10, anode is 5. Similarly D_3 , cathode is 10, anode is minus 5. So, what is the conclusion here? In a common cathode configuration, diode whose anode potential is maximum, will conduct.

I will repeat, in a common cathode configuration, diode whose anode potential is maximum, will conduct. What happens in common anode configuration? I have again a large number of diodes, anodes are tied together and cathode has various potentials. I am not going to talk about where this point is connected, let us not worry now. What happens, which diode conducts here? Let us assume that D_1 conducts. If D_1 conducts, potential of X is 5 volts or may be 5.7. If potential of this is potential of X is 5.7, cathode potential of D_2 is 10; in that case, D_2 is reverse biased, D_2 cannot conduct. But then, what happens to D_3 ?

Anode potential is 5.7, cathode potential is 5, the potential difference across it is approximately 10.7 volts. You cannot have that situation. Therefore, D_1 cannot conduct. Let us see what happens if D_3 conducts. If D_3 conducts, voltage potential of X is either minus 5 or minus 4.3, if I assume 0.7 volts across the diode. If potential of X is 4.3, D_2 is reverse biased, minus 4.3 minus 10. D_1 is also sorry D_2 is reverse biased even D_1 is also reverse biased, minus 4.3 plus 5. So therefore, in common anode configuration, diode whose cathode potential is minimum, will conduct. So I will repeat, diode whose cathode potential is minimum, will conduct in common anode configuration. So, you need to remember these 2 points.

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Single phase bridge, very popular. There are 2 diodes; D_1 and D_3 form a common cathode configuration, D_4 and D_2 form a common anode configuration. In the positive half, potential of A is higher than potential of B. So therefore, D_1 starts conducting and in the lower half, D_2 starts conducting. so voltage apply when D_1 and D_2 starts conducting, voltage applied to the load is same as the input voltage.

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EQUIVALENT CIRCUIT

$$V_m \sin \omega t = R i + L \frac{di}{dt}$$

$$i = \frac{V_m}{Z} \left[\sin(\omega t - \phi) + \sin \phi e^{-x} \right]$$

$$i = i_{\max} \quad x/2 < \omega t < x$$

$$v_L = R i_{\max} \quad \therefore L \frac{di}{dt} = 0$$

At $\omega t = x$, D_1 & D_2 starts conducting.
 +ve V is applied to the load.
 At steady state if load is highly L , i_L becomes almost constant.
 Whenever Diode conducts source $I =$ Load I

This is the equivalent circuit, source D_1 , load D_2 , back to source. V_i is equal to V_0 , the circuit equation is $V_m \sin \omega t = R i + L \frac{di}{dt}$. Solution, we have already discussed. i reaches a peak value in between $\pi/2$ and π . At that instant, instantaneous value of the input voltage is $R i_{\max}$, because $L \frac{di}{dt}$ when i is equal to i_{\max} is 0. At ωt is equal to π , potential of B becomes higher than potential of A.

So, what happens? D_3 starts conducting. The moment D_3 starts conducting, cathode potential of D_3 is same as the potential of B, assuming the diode to be ideal. In that situation, a negative voltage appears across D_1 , because potential of A is less than potential of B in the negative half and **anode**, cathode potential of D_1 is the potential of B. So therefore, a negative voltage appears across D_1 , diode turns off. Same thing happens in the lower half also. Therefore, in the negative half; D_3 , load, D_4 , back to source. This is the equivalent circuit.

In the positive half, current reaches maximum somewhere in between $\pi/2$ to π , it starts decreasing depending upon the load parameters is continuous to decrease and again it starts increasing in the negative half cycle and the instant when the current starts increasing, that instant the KVL is V_i is equal to i_{\min} into R . I will repeat, at this instant, V_i should be equal to i_{\min} into R . Whereas here, it is V_i is equal to i_{\max} into R .

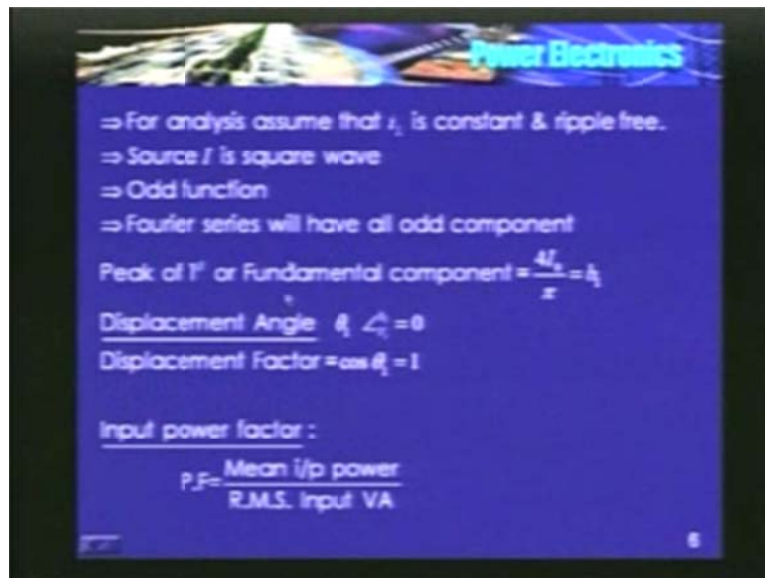
In both these points, $L \frac{di}{dt}$ is 0. So therefore, current continuous to decrease till V_i is equal to $R i_{\min}$. Beyond that point, current again starts increasing and after sometime a steady state is reached and depending upon the load parameters, the load is highly inductive, current increases, decreases and attains a steady value.

So, at steady state if the load is highly inductive, I can assume that load current becomes almost constant. When the diodes are on, the source current is same as the load current. Input voltage may be a sinusoid; since, the load is highly inductive, we assume that I_L becomes almost constant. Therefore, source current will not be a sinusoid. If I assume that source current is

constant and ripple free, the source current is a square wave form, is a constant till 0 to π or $n\pi$ to $n\pi + \pi$ and it is minus I_0 from $n\pi + \pi$ to $n\pi + 2\pi$. This I_0 is the magnitude of the load current, constant I_0 .

Source is a sinusoid, input voltage is a sinusoid, whereas, the current is the rectangular wave. So, what are the various parameters that have to be defined now?

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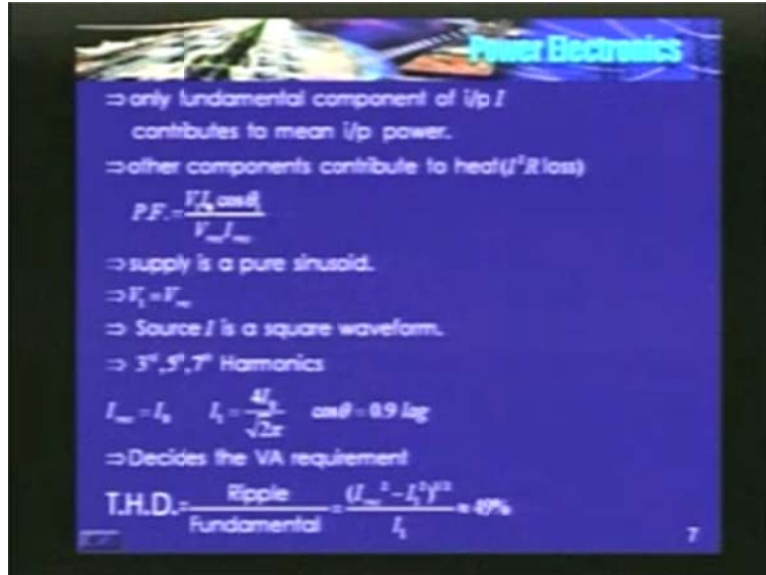


It is an odd function, so if I write the Fourier series will have all odd components. What is the peak of the fundamental? It is given by $4 I_0$ by π . It is the magnitude of the fundamental or the magnitude of the first component. In other sense, $4 I_0$ by π into $\sin \omega t$, that is the magnitude. It has third harmonic component, fifth, seventh, all odd harmonics are present. Now, what is a displacement angle? It is the angle between the fundamental component of the input voltage and the fundamental component of the source current.

It is the fundamental component of the input voltage and the fundamental component of the source current. If I plot the fundamental component of source current, it looks like this; whose frequency is the same as the input voltage. You will find that these 2 voltages and the fundamental component of the source current are in phase. In other words, displacement angle is 0.

What is the displacement factor? It is the cause of the displacement angle. In other words, it is 1, unity. What is the input power factor? It is defined as mean input power divided by RMS input VA. We know that, it is only the fundamental component of the input voltage and the input current that are responsible for power transfer. I will repeat, it is the fundamental component of the input voltage and the current are responsible for power transfer. The higher frequency components, the all other R components will give rise to additional $i^2 R$ heating. They do not contribute to power transfer, they contribute only to additional $i^2 R$ losses.

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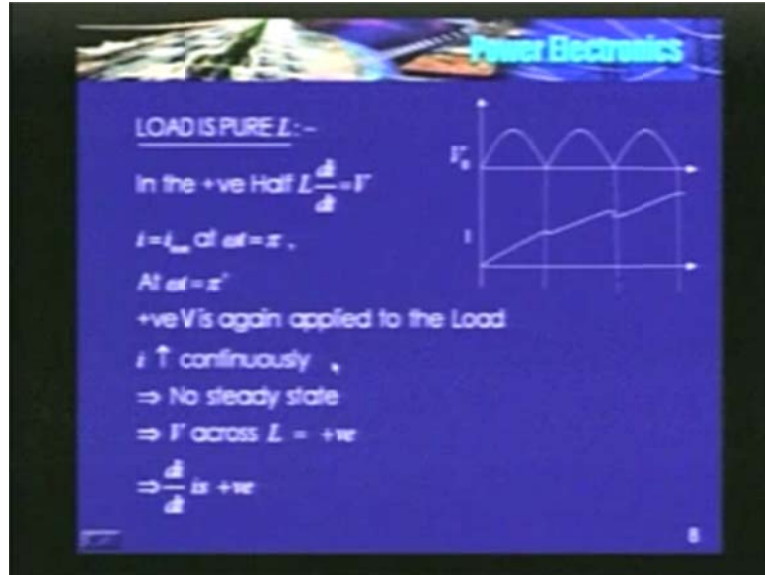
So, input power is given by $V_1 I_1 \cos$ of the angle between V_1 and I_1 . Both V_1 and I_1 are RMS values. RMS values **RMS values** of the fundamental component of the ... and I_1 is the RMS value of the fundamental component of the input current, V_1 . Since, we had assumed that voltage is a pure sinusoid, V_1 is equal to V_{RMS} itself. Source current is a square waveform. The third, fifth, seventh all harmonics are there. **We have assumed to be** we have assumed that load is highly inductive, that load current remains constant whose magnitude is I_0 , so the RMS value of the source current is I_0 itself.

RMS value of the fundamental component is given by this equation - $4 I_0$ by square root of 2 by pi. So therefore, if you substitute all these values in this equation, power factor becomes 0.9, it is lagging. Remember almost all the power electronic circuits, power factor is lagging. So this factor decides the volt ampere requirement. The size of the equipment that is required to feed a load depends on VA requirement and not on just on power.

What is the total harmonic distortion? It is given by, we have defined already it is a ripple divided by the fundamental component. This we have already defined I_{RMS} square minus I_1 square. The square root divided by the fundamental component, it is as high as 49%. Let us see sometime later in the course, how exactly to reduce this total harmonic distortion. This 49% is the ripple content. It gives rise to only additional $I^2 R$ heating in the load. It also affect the source side, we will see sometime later, the effects.

What happens if the load is purely inductive? In the half wave rectification when the load is purely inductive, diode conducted for the entire 2π radians, average voltage across the load becomes 0, current reaches peak at ωt is equal to π and becomes minimum at ωt is equal to 2π . What happens in the full wave rectification?

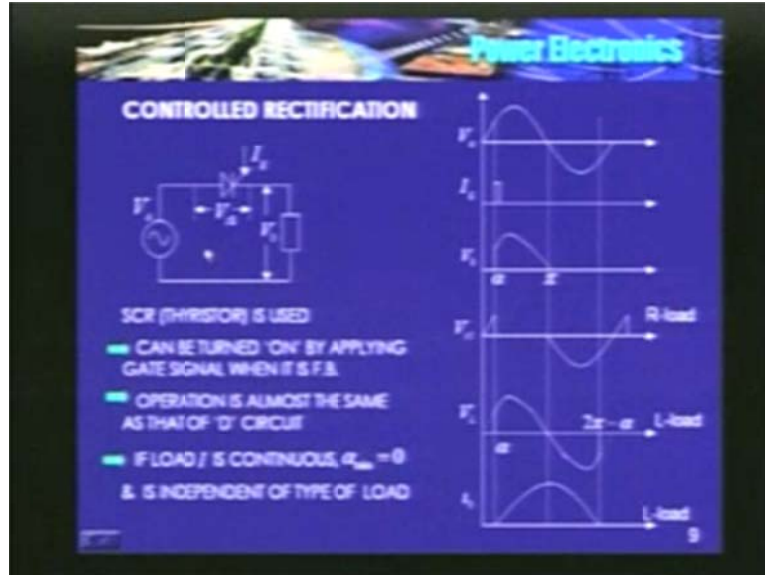
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Current starts from 0, sorry, it is not linear, it increases, reaches a peak at ωt is equal to π , again at ωt is equal to π plus, a positive voltage is appearing across the load. In positive voltage appearing across the load, it implies that di by dt has to be positive because, $L di$ by dt is equal to V , so left hand right hand side is positive, so di by dt has to be positive. So, current again starts increasing. Whereas in half wave rectification from π to 2π voltage appearing across the load was negative that is why di by dt becomes negative.

Whereas in full wave rectification, it is positive voltage appearing across the load beyond π , so, current again starts increasing. Here, it is not linear ... so on and so current goes on increasing till, either a diode has to fail or the source has to fail or something has to fail. There is no steady state here, because $L di$ by dt is always positive. If $L di$ by dt is positive, di by dt is positive, current goes on increasing, no steady state. So far we discussed about uncontrolled rectification, full wave as well as half wave. Now, we will go in for a controlled rectification. I need to use a 3 element device.

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So, we have already discussed about SCR - anode, cathode and the gate. So, we can turn on the SCR when it is forward biased by applying a positive gate signal with respect to the cathode; that we have already studied. So when the device is on, circuit behavior is same as that of the diode circuit, that is almost the same, there is no much difference. There could be some difference in the wave form. So, we will see.

So in the positive half, I am assuming the load to be passive, somewhere in between 0 to pi I am triggering, alpha is a trigger angle, finite I_g is flowing, SCR turns off, turns on. The moment that SCR turns on, SCR is triggered somewhere at this instant. Input voltage is the same as the load voltage. So, the instantaneous value of the input voltage is the same as the load voltage. So, load voltage jumps to this value, this follows the input till the current becomes 0. If the load is purely resistive, current becomes 0 at ωt is equal to pi, SCR turns off. Till you trigger it again, in the positive half, SCR is off. So, what is the voltage appearing across the SCR?

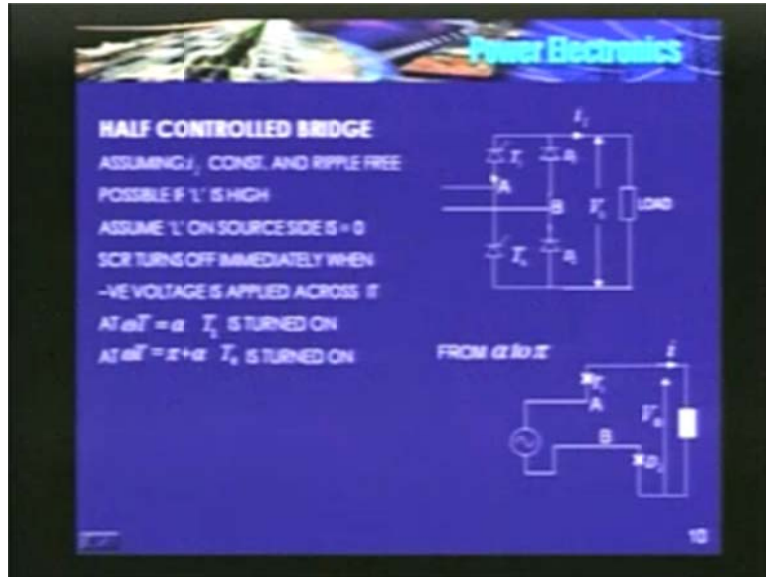
It is triggered only at alpha. So, ωt is equal to 0 to alpha. It is in the forward blocking mode, it is forward biased, a positive voltage is appearing, but then there is no gate signal. So, it cannot conduct. This is V_i , at ωt is equal to pi, it becomes 0. Input voltage is also becoming negative, voltage across it is also becomes negative, till 2π and cycle continues. This is for the purely resistive load. Average value we can determine by integrating this wave form.

What happens if the load is a purely inductive? Again, we have to trigger the SCR at alpha. We know that average voltage across the inductor is 0 here or should be 0. Purely inductive, circuit equation is; when the SCR is on, V_i is equal to $L \frac{di}{dt}$. Instantaneous value of the input voltage is 0 at ωt is equal to pi, current starts increasing, reaches a peak and starts decreasing. So, this area is positive $L \frac{di}{dt}$.

Average, I said average voltage across inductor should be 0. So, if it has started conducting at alpha or if the in the positive half the duration is pi minus alpha, so it has to be equal to, even in the negative half, pi minus alpha. So, SCR turns off at 2π minus alpha. So, that average voltage

across the inductor becomes 0. Positive $L \frac{di}{dt}$, negative $L \frac{di}{dt}$, current charge is decreasing at π and becomes 0 at $2\pi - \alpha$. So, this is the difference between controlled rectification and uncontrolled rectification.

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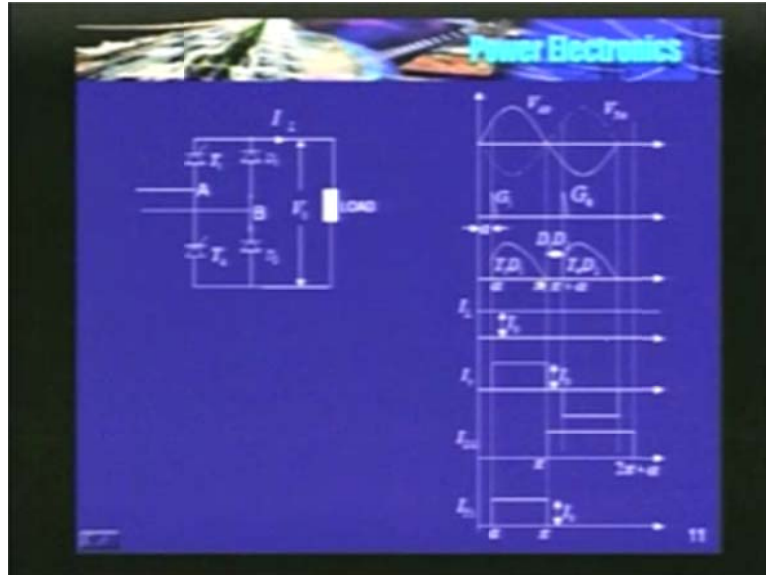
Only thing you need to know is type of load and the circuit equation, you can solve that. Half controlled bridge: just now we studied uncontrolled bridge, **now we are, let us deal**, let us discuss half controlled bridge wherein, there are 2 SCRs and 2 diodes. Configuration 1, what are the other assumptions? Other assumptions are load is highly conductive, so load current is assumed to be constant and ripple free, **the magnitude of I_0** , magnitude of I_L is I_0 , whatever the analysis we did for diode circuit, they are valid and source side inductance is 0.

We will see, why it is 0 or what happens if it is finite, sometime later. As of now, we will assume that source side inductance is 0. Another thing is SCR turns off immediately when a negative voltage is applied to it. In the sense, though all the devices are non ideal, they require a finite time to attain the forward blocking mode, the forward blocking capability.

In the analysis will assume that all the devices are ideal, turn off as well as turn on time is 0. In other words, the moment you turn on, the moment you apply a positive gate signal to a thyristor, it turns on and the moment you apply a negative voltage across it, it turns off. **At** in the positive half; of course, T_1 and D_3 , they form a common cathode configuration and T_4 and D_2 , they form a common anode configuration, the positive half potential of A is higher than potential of B. So, T_1 , if the gate signal is applied, T_1 can conduct.

Let us assume that in the positive half, somewhere at ωt is equal to α T_1 is triggered. In the lower half, since T_4 and D_2 form common anode configuration, device whose cathode potential is least will start conducting. So, D_2 starts conducting. So, this is the equivalent circuit; source T_1 , **load D_2 sorry** back to the source. Here are the wave forms; at ωt is equal to α , T_1 is triggered, at ωt is equal to $\pi + \alpha$, T_4 is triggered.

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So, when T_1 and D_1 are conducting, load voltage is same as the source voltage, it becomes 0 at ωt is equal to π . What happens from π to $\pi + \alpha$? T_4 is triggered only at $\pi + \alpha$. In the upper half, potential of B is less than higher than potential of A, in the negative half. At ωt is equal to $\pi + \alpha$, potential of B becomes higher than potential of A. Immediately, D_3 starts conducting. The moment D_3 starts conducting, a negative voltage appears across T_1 ; T_1 turns off. Nothing of that sort happens in the lower half, because T_4 , though T_4 is forward biased, we have not applied gate signal to T_4 . So, T_4 is still in forward blocking mode.

Load is highly inductive. So, current starts flowing through D_2 and D_3 . In other words, current free wheels through D_3 and D_2 , the equivalent circuit is D_3, D_2 . So, this is the condition; D_2 was conducting, potential of A, though it is higher than potential of B, we have an open circuit here, T_4 is not triggered.

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Lower Arm:

- ⇒ T_4 is F.B.
- ⇒ Gate signal is applied only at $\pi + \alpha$
- ⇒ From π to $\pi + \alpha$ T_4 is O.C.
- ⇒ D_2 continues to conduct
- ⇒ Load is free wheeling through $D_2 - D_3$
- $V_0 = 0$ Source $I = 0$
- ⇒ Continues till $\pi + \alpha$ while T_4 is triggered
- ⇒ It is F.B. & gate signal present
- T_4 starts conducting
- ⇒ Applied -ve V across $D_2 \Rightarrow D_2$ turns off

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So, D_2 continues to conduct, that is the load circuit. Voltage applied to the load is 0. Source current is 0, (not audible) α , current free wheels through D_3 to D_2 . What happens at ωt is equal to π ? T_4 was forward biased at ωt is equal to π . So at $\pi + \alpha$, it is triggered, it starts conducting. The moment it starts conducting, potential of A will become potential, the anode potential of D_2 . In the negative half, potential of B is higher than potential of A. A negative voltage appears across D_2 , D_2 turns off.

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- ⇒ From $\pi + \alpha$ to 2π
- ⇒ Operation is similar to that of α to π
- Only direction of I_L has reversed
- ⇒ From 2π to $2\pi + \alpha$
- ⇒ Operation is similar to that of π to $\pi + \alpha$
- ⇒ T_1 & D_3 form common anode config.
- ⇒ D_3 starts conducting
- ⇒ Applies -ve 'V' across T_1
- T_1 turns off
- ⇒ Upper half: T_1 is not triggered

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So, the equivalent circuit is now; source D_3 , load D_4 and back. So, in the first half or from α to π , current was flowing in this fashion or if I showed in the page, it is T_1 load T_2 . In the second half, source current has reversed, π plus α to 2π , it is enters ... back to 2 .

How do we turn off T_1 ? T_1 turns off the moment D_3 starts conducting. When the potential of B becomes higher than potential of E, potential of A, D_3 starts conducting. A negative line voltage appears across T_1 . Hence, this set of common turn off process is known as line commutation. Why it is line commutation? I am using the input line voltage itself to turn off the conducting thyristor. There are other processes that we will see sometime later, other processes of turning off the thyristor, we will see later. So, this is known as line commutation. The input voltage itself is used to turn off the thyristor, hence, the name line commutation.

The source current wave form; π to α to π , it is I_0 , π plus α to 2π , it is I_0 in the negative direction. What happens again at ωt is equal to 2π ? At ωt is equal to 2π plus, potential of B becomes less than potential of A, may be. But then, T_1 is not triggered. T_1 is triggered at only after α , 2π plus α . Till then, we have open circuit here. So, potential of A does not appear at the cathode of D_3 . So, D_3 starts continuous to conduct.

I repeat, D_3 continuous to conduct, whereas in the lower half we have an uncontrolled device D_2 , a common anode configuration. So, immediately D_2 starts conducting. The moment D_2 starts conducting, a negative line voltage appears across T_4 , T_4 turns off. So, current again starts flowing in D_3 and D_2 . So, from 2π to 2π plus α , D_3 and D_2 continuous to conduct. Voltage applied to the load is 0. T_4 is again commutated or turned off using the line voltage, hence, the name line commutation.

So, if I plot the duration of diode conduction with time, you will find that D_2 starts conducting. If I plot D , D_3 starts conducting at π , continuous to conduct till 2π plus α . Please, this should be I_{D3} , sorry about that, it should be I_{D3} . So, D_3 starts conducting at π plus, it continuous to conduct till 2π plus α . Please correct it, this is D_2 and this is D_3 , D_2 D_3 , sorry, 2π plus α , whereas, thyristor conducts from α to π itself.

So if I see, if you see, in 1 circuit some devices are conducting for a longer duration and some devices conduct for a very short duration. Magnitude of the current that is flowing through device is same. I have assumed load to be highly inductive. So, load current is constant and ripple free, magnitude is I_0 . So, average current rating of thyristor is less than the average current rating of the diodes, because they conduct for a shorter duration.

Somehow, that is not desirable. In 1 circuit, average current rating of some device is different from that of the others. There is a small mistake here, D_1 this should be D_1 , D_2 , D_3 . So, here D_3 and D_2 start conducting and here T_4 and D_3 . So, this is the current wave form of I_{D3} .

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$$V_o = \frac{V_m}{\pi}(1 + \cos\alpha)$$

$\Rightarrow V_o$ is always +ve
 \Rightarrow Load I is always unidirectional
 \Rightarrow Single Quadrant Converter $I = \frac{2V_o}{x}$

Displacement Factor = $\cos\left(\frac{\alpha}{2}\right)$

Lagging: RMS value of the fundamental component source I_s

$$I_s = \frac{2\sqrt{2}}{\pi} I_o \cos\left(\frac{\alpha}{2}\right) \quad PF = \frac{\sqrt{2}(1 - \cos\alpha)}{[\pi(x - \alpha)]^{1/2}}$$

So, what is the average output voltage? What is the average value of this wave form? 0 to alpha it is V_m , pi to pi plus alpha it is 0. So, if I take the average, it is given by V_m by pi into 1 plus cos alpha. Alpha is varying from 0 to pi, so average value is always positive. So, if I plot alpha versus V_o , this is the variation, **whereas**, where this is 1 per unit. 1 per unit is $2 V_m$ by pi, $2 V_m$ by pi. When alpha is equal to pi by 2, this becomes 0.

So, average value of output voltage is 0.5, per unit value is 0.5. Load current is always unidirectional. Current is always flowing from positive DC bus to the negative DC bus. I mean, current is always flowing from positive DC bus to negative DC bus, unidirectional. Average value of the output voltage is also always positive. So, power input to this bridge is always positive. In another words, source is always supplying power to this bridge.

So, if I plot VI characteristics of this, V_o is positive, I_o is also positive. **It is** operation is in the first quadrant. What is the displacement angel? **What is the**, what is the angel between the input sinusoid and the fundamental component of the source current? Again, it is odd function, odd harmonics are present. The angel between the fundamental component of the input voltage and fundamental component of the source current is found to be half of alpha. In another words, it is alpha by 2. So, displacement factor is cos of this angel. Minus sign indicates that power factor is lagging.

It is even the sorry, even the displacement factor is lagging. Because, if you see here, **sinusoid** input sinusoid fundamental components cuts the 0 axis at somewhere in here. So if you see here, fundamental component lags the fundamental component of the voltage. Hence, **the power** displacement angel is lagging.

What are the RMS value of the fundamental component of source, i ? Procedure is the same. It is found to be this value. You need to find the RMS value of the source current, this is the value and the power factor is given by this equation. The procedure you use is same as that we used in the full bridge uncontrolled rectifier.

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Observation:

- \Rightarrow If $\alpha \neq 0$, γ for T \neq γ for D
- \Rightarrow Av. Current rating of T < Av. Current rating of D

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So, what is our observation? If alpha is equal to 0, if alpha is not equal to 0, the duration for which the thyristor conducts is not the same as that of diode. Gamma for thyristors is not equal to gamma for the diodes. So therefore, average current rating of thyristors is less than average current of the diode.

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Case II: Operation α to x is same

$V_1 = V_m$

From x to $x + \alpha$

Lower arm common Anode config.

D_4 starts conducting

In upper half T_3 F.B.

\Rightarrow No triggering pulse (Gets only at $x + \alpha$) till then it can not conduct

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Let see, we will take a second configuration. In the previous configuration, we connected T_3 and T_1 in 1 leg. Now, we are connecting T_3 and T_1 in 2 different legs. We have T_1 and T_3 making a common cathode configuration and D_4 and D_2 making a common anode configuration. At omega

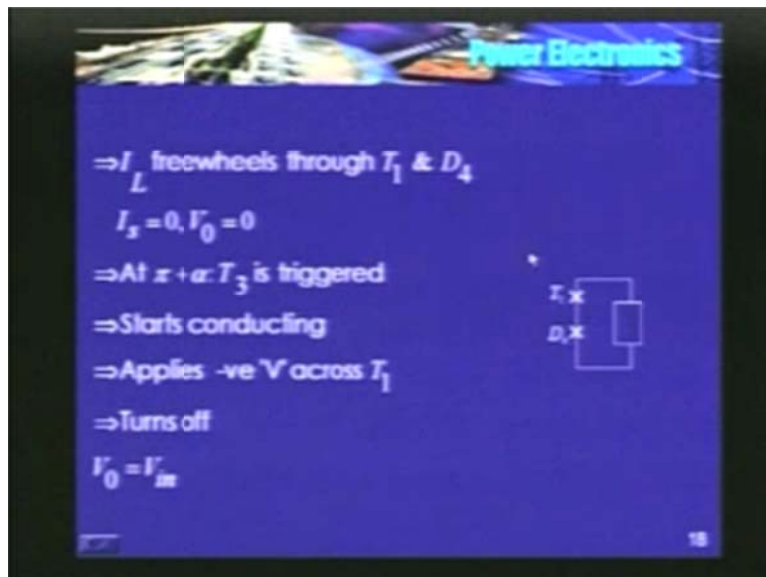
t is equal to α , T_1 is triggered. The operation of the circuit is same as that of the previous one, source, T_1 , load, D_2 .

What happens at ωt is equal to π ? In the lower arm, D_4 and D_2 form a common anode configuration. Potential of B is higher than potential of A from ωt is equal to π plus. So immediately, D_4 starts conducting. In the upper half, T_3 is forward biased but then we have not applied a gate signal to T_3 . So therefore, T_3 has not started conducting as yet. Since the load is inductive, current starts flowing between T_1 , load and D_4 . So, current starts flowing through T_1 , load and D_4 .

In the previous case, current started flowing from D_2 , D_3 so on. So, current free wheels through T_1 and D_4 . Voltage applied to the load is 0, source current is also 0. At ωt is equal to π plus, T_3 is triggered. The moment T_3 is triggered, cathode potential is same as the potential of B which is higher than potential of A, then negative voltages appears across T_1 , T_1 turns off. So, again line commutation, the process is known as line commutation. I am using the input voltage to turn off T_1 .

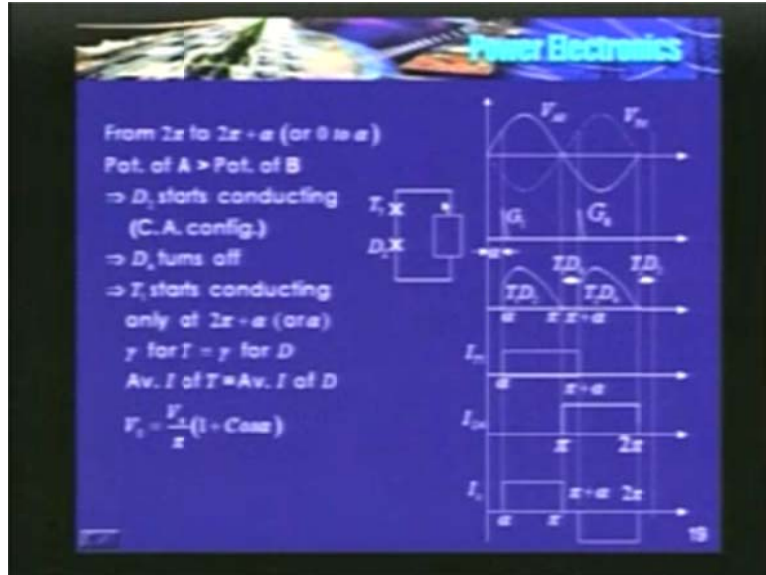
So, from ωt is equal to π plus α , T_3 starts conducting. T_3 , D_4 started conducting at ωt is equal to π plus. So, this is an equivalent circuit.

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This is the equivalent circuit at ωt is equal to π to π plus α and this is the equivalent circuit at from 2π to 2π plus α .

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So, here are the various wave forms. **Take** given gate signal to T_1 , gate signal to T_4 , $T_1 D_2$, they will conduct from α to π and from π to $\pi + \alpha$, $T_1 D_4$, same leg, 1 thyristor and 1 diode not conducting, from $\pi + \alpha$ to 2π , $T_2 D_4$ starts conducting and from 2π to $2\pi + \alpha$ $T_3 D_2$ starts conducting.

So, **will** if I plot the current flowing through thyristor T_1 with α , we will find that T_1 is conducting from α to $\pi + \alpha$ and D_4 if I plot, any diode for that matter, π to 2π . So, you will find that γ for T_1 is π radians and γ for diodes is again π radians. So, average current rating of thyristor is same as that of the diodes. The source current wave form is as same as the previous one; α to π , it is positive I_0 , $\pi + \alpha$ to π , it is minus I_0 . Average value of the output voltage is again V_m by π into $1 + \cos \alpha$. Wave form is the same, only the devices they there are conducting are different. Please, this should be T_3 .