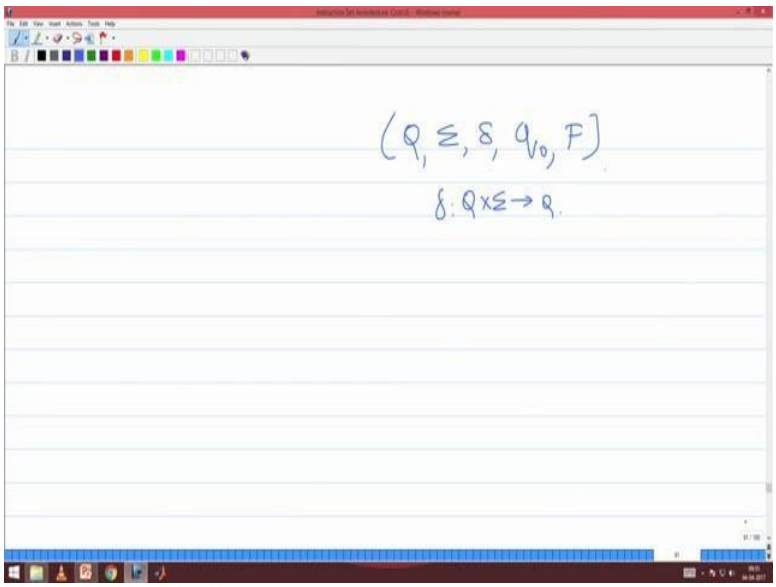
Computer Organization and Architecture
Prof. V. Kamakoti
Department of Computer Science and Engineering
Indian Institute of Technology, Madras

Lecture – 37
Part - 02
Shared Memory Architecture

Right, so now we will go and look at the first state machine; so to start with so how do we educate a state machine let me try and do that. So, to start with there is a start state.

(Refer Slide Time: 00:34)



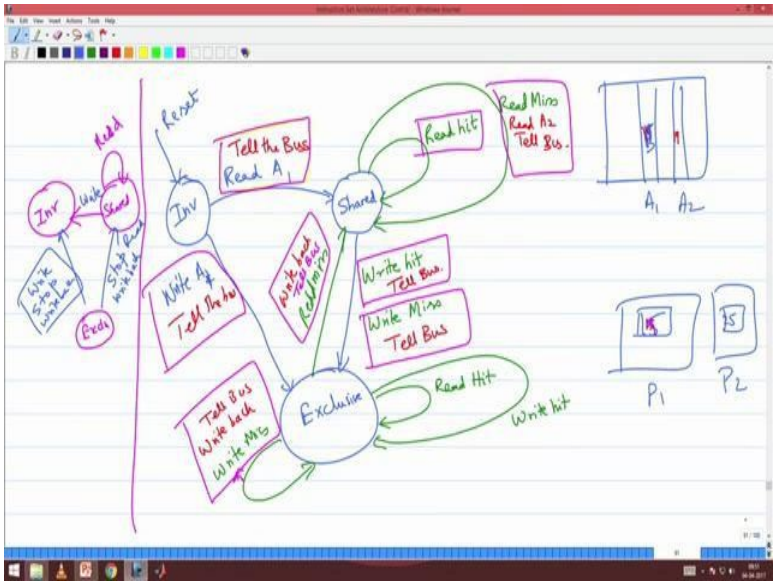
So, what is a DFA incidentally; how do you define a DFA it is a 5 tuple Q, sigma, delta Q naught F, where Q is the set of states, sigma is a set of alphabets, delta is a transition function from what

Student: (Refer Time: 00:50).

Q cross sigma to Q; Q naught is the initial state and F is a set of final states; this

is what I want you to answer. So, it is 5 tuple Q, sigma, delta, Q naught, F; Q is set of 5 initial states, sigma is say state; sigma is alphabets delta is Q cross sigma to Q; so, very few English words.

(Refer Slide Time: 01:23)



So, this is a precise mathematical definition of a deterministic finite automation come on [FL]. Now we start, so every fellow everything starts with invalid state; so, this is a start state. So, this is the state Q naught of your thing, so when I reset every cache line will be invalid.

Now, I read an address A; when I read an address A then I go into shared state because I am reading at A. So, let me say A 1, so in the main memory let this be the pros at P 1, this is the cache, this is A 1; that means, say that there is another A 2. Now let me say that this some 15 stored here and 19 stored here. Now when I read this thing A 1; I have 15, the value that is also 15; somebody else all can also read there also be. So, I am in a shared state, but now I go and tell the bus. So, whatever I am writing in red is; I say I go and whenever I read A 1; I tell the bus that I am reading A.

You are getting this? Now in this part after this, so again I am reading A 1 or whatever I call it as read hit when will I get a read hit I read the same address read A 1. I may also get what read miss, when will I get read miss? When I read A 2; I tell the bus right when I read A 2 and I get a read miss; you are getting this yes or no; you are able to follow.

And when I read A 2, since this is shared when I read A 2; I will just go and overwrite it

because whatever is there in the memory is I have 15 here, I also have 15 here, but when I when I read A 2; then I need not go and write this 15 back because its already its only in

a shared state. So, I need not go and write hit back into the cache you are getting, but when I get a read miss, I have to tell the bus that I am reading A 2.

Now, let us take the next thing when I get the; write miss when I do a write; write hit when I get a write hit; I go into an exclusive state. But I will tell bus about this write which address I am writing I will tell the bus. So, let me take some colour, colour what colour do you choose. Now, if I get a write miss; I have to just replace, so I need not what I will also tell bus. When will I get a write miss? I am already; I read A 1; now I am writing into A 2; that means, I will get a write miss here. So, I have to fetch 19 or I have to write something in the 19 write fetch also I will tell this thing; for the same cache line, this state machine is for a single cache line.

Now, what is the next thing I will get; in this state; if I get read hit; if I get a write hit; no problem, if I get a read hit there is no problem; if I get write hit there is no problem. If I get a read read miss, if I get a read miss what will I do if I get a read hit or write hit there is no issue because I am in exclusive state. If I get a read miss, I have to go to shared state, but while going to shared state; what I should do? I need to do a write back and have to tell bus also what I am reading. Now, if I get a write miss; now I am writing it to what I should do? Again I do a write back of A 1 and I tell bus. Are you able to follow this? Any doubts? Tell the bus I am writing into A 2.

Student: (Refer Time: 08:11); however, bus (Refer Time: 08:13).

It is the I am the only fellow know that.

Student: Ok.

I am the bus fellow, I have the bus I can only read or write into the bus. So, I will tell the bus say I am writing into A 2. So, when I when I read A 1; when I am storing A 1in exclusive state and I want to read A 2; that means, now the line after reading A 2; I go to the shared state, but then I had the latest value of A 1; so, I will write it back there and then bring A 2, but now I will become shared because the value of A 2; I am storing say probably 19 here, it is just the same as what is stored in the memory.

But if I am writing into A 2; what is a write miss because currently I am storing A 1; I am writing into A 2 that becomes a write miss. So, what I do; I will write back the latest

value of A 1 back and then I will start into writing into A 2 and I will tell the bus say I am writing into A 2. Now I am in invalid state and I write into A 2; I write into A 1 or A 2 whatever write. Now, I go to an exclusive state and I have to tell the bus here well this is another you all follow. So, this is for this and this is what we call as the processors initiator state machine; the shift of the I am associated with P 1.

So, P 1 does some transaction because of that how my status can change. On the other hand let us take the bus initiator thing, so bus initiator again if I am in a invalid state, I do not really bother what is happening in the bus. But, if I am in an exclusive state or shared state; I should see something. When will I be interested at all? I will be interested, if something that is happening in the bus is based on the address that I am storing.

As a cache line, I am storing address A; if something happens to A; then I get a lot it. So, so I will be saying what is happening there; I am invalid no problem, I am shared, I am storing address A; somebody reads A; like you know when they read A; they tell the bus somebody reads A; nothing happens I will be in the shared state. So, when I see a read hit, I can say read hit means the location I am storing is what is being read, I do not do anything; I just keep peacefully. Then when somebody is going to write, so I need not say read hit here; read somebody is going to read the same location then I remain in the shared state.

Somebody is writing into that location then I go and make myself invalid. I am in shared state, whatever value I am storing is what is there in the memory. So, somebody is writing into A; so that is why you know, when I do a write I say tell bus write. So, somebody is writing into A; that means, he will now have the latest value. I will not have the value I need not go and update the memory any because I do not have the; so, whatever I am storing is what is there in the memory that is what we defined that the shared state. So, I need not go and update the memory there; so, I just go off to invalid.

So, whatever I have now he has taken control, so whatever I have is invalid; I am in an exclusive state and somebody reads then I will say stop write back and so I am having a latest value of A; I am having 15 what is there in the memory is 10; somebody is trying to read that address A; I say A stop, stop I have the latest value. I go and write 15 into the memory; that is what I mean by write back. I will stop him, I will write back and I will now go to shared because he is going to read it.

So, he will also have the value of 15; I will also have the value of 15. So, now, I go into a shared state, when I get this is read; so, in this state when I get a read, when I get a write; I am holding A 1, somebody again is trying to write into A 1. So, when I get a write; what I do; I will say stop write back. I am having the value of A 1; somebody is writing into A 1; I am having 15. So, what is there is I am having 15; what is there is 11; somebody other P 2 wants to write say 25; into A 1, he is trying to write 25; other point I have the value of 15. So, what I say wait I go and write the value of 15 back and then ask him to now you go start writing whatever you want, so I go into an invalid state.

Student: Sir what is the point of write back?

Write back; what will happen if that P 2 write has an issue some segmentation fault, when I do a core dump; I should know what is the latest value that is there in the memory. So, that is the reason why I go and write back and then ask P 2 to now go and do a write. So, it is a very interesting very important question; now I am having the latest value of P 1 of address A; somebody else wants to write into that A, so what I do? I will stop him; I go and write the value of a whatever latest value I become invalid because he is going to have the latest value; he is going to write something more there, something other than this value and then allow him to do that.

But why do I go and update it; I go and update it because if that fellows thing has a exception, it goes to a core dump for whatever reason maybe. When it goes to a core dump, then I need to when I core dump; I need the latest value of (Refer Time: 15:28).

What is the core dump? It gives you the complete state of the memory and also all the variables; I mean the latest value and that is the precisely the reason why I go and write and then when I get a write, I go and stop and then write back and then allow him to proceed; so, these two are the state machines.