Switching Circuits and Logic Design

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Lecture - 08
Logic Families to Implement Gates

If you recall in the last lecture, we had talked about the various logic gates. Now, in the present lecture we shall be talking about some Logic Families to Implement Gates. Now, what we mean by logic families, see over the years there have been many techniques, or many ways in which people have come up with for designing this basic gates, because the ultimate objective was to design circuits, digital circuits and this gates were the basic building block.

Now, we shall be looking at some of these techniques or logic families using which such gates can be constructed, which will help us in designing larger circuits. Now, we shall be looking at some of the conventional methods, which have been used and also some unconventional methods. So, this we shall be discussing in the next couple of lectures.

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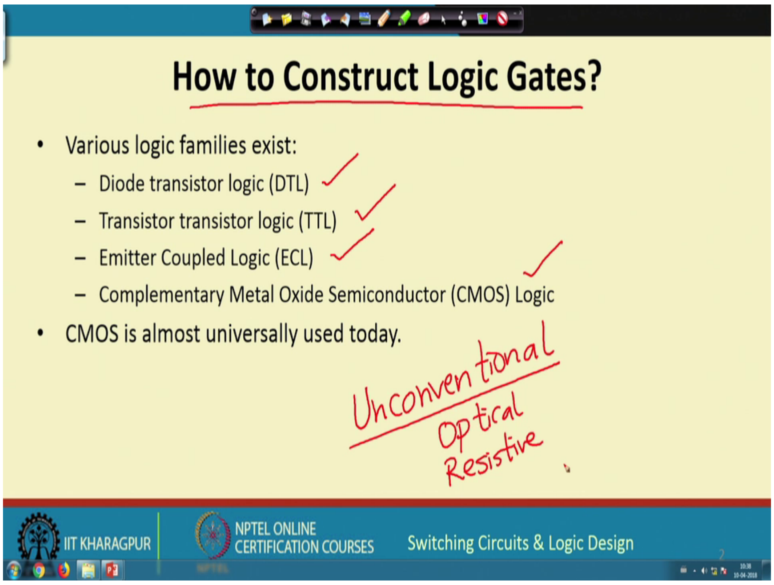

So, today in this lecture we shall be talking about the issue of logic families, which means how to construct logic gates so that they may be used in circuits.

Now, when you talk about logic families there are various logic families which have been used, like conventionally there are techniques like diode transistor logic, transistor transistor logic, emitter coupled logic, today the most widely used is something called CMOS, complementary metal oxide semiconductor, this is universal used today and there are some unconventional families also which we shall also be discussing in the next lectures. Just let me tell you unconventional it can mean, some kind of optical circuits, where instead of voltages and currents, we talk about lights presence and, absence of lights or there are something called resistive circuits, where the resistance value of some device is changed and that can represent the state 0 and 1 ok.

But in this lecture we shall be looking at some of the more conventional logic families and how they work very briefly.

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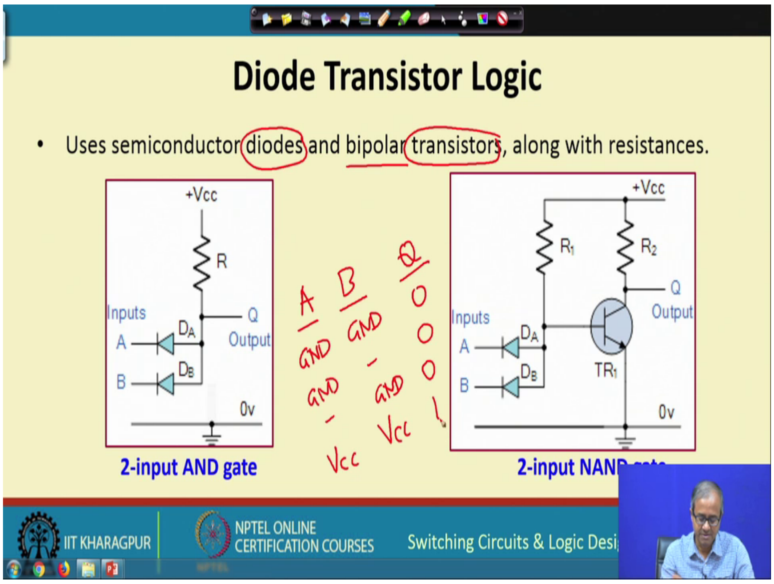

We start with diode transistor logic which was one of the first logic families that were proposed. So, as the name implies we use semiconductor diodes and transistors. So, so when these logic families proposed bipolar transistors were used for the implementation. So, I am showing you some simple examples. Let us consider this case where you want to build a 2 input AND gate. So, the way this circuit was designed was like this, they were 2 diodes connected like this and on the output site, there was a resistance connected to a positive supply voltage.

Now, let us see how this work this method used to work. So, the inputs are A and B. Suppose I have grounded both the inputs, ground means let us say logic 0 and, this positive supply voltage means logic on let us follow this convention. So, if the inputs are at ground, then you see from this power supply, there will be a current flowing path, current will be flowing towards A and B. And the voltage at the output node will be very low, it will be ground plus the drop across the diode maybe about 0.6, 0.7 volt like that.

So, the output will be at a very low voltage and, they are very low voltage let us say it is equivalent to logic 0. This will be true if at least one of the inputs are ground, if A is ground B can be high voltage also, or B is ground A can be high voltage also. Then also there will be a current flowing path and the same thing will happen output will be 0, but if both the inputs are at the high voltage plus voltage, then the diode should be reversed biased no current is flowing and the output will be equal to VCC so, the output will be 1. So, you see this is the truth table of an AND gate. So, you can realize a AND gate like this.

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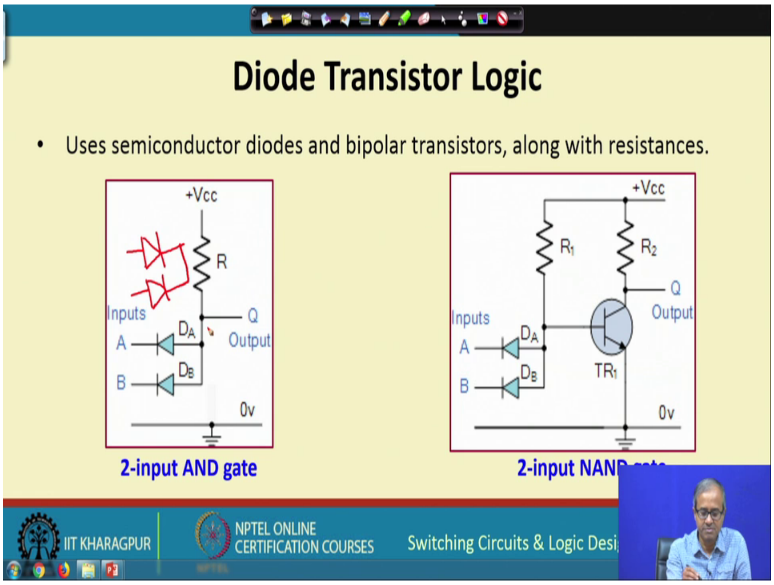

And just a thing if you just reverse the direction of these diodes, if you connect them like this, then it becomes an or gate, or gate says if at least 1 of the inputs are 1, then 1 of the diode will be forward biased, there will be high voltage here and the output will be high, but if both of them are 0 then this will be forward biased the voltage here is there. So, this you can design like this.

And to build a NAND gate for example, you have already seen how to build an AND gate this and followed by a transistor circuit like this, this realizes a naught, and AND followed by a naught is an NAND, you see this transistor how it works if this voltage is 0 low this transistor will be of no current will be flowing and the output will be almost equal to VCC high, but if this is 1 then the transistor will be conducting, there will be a current flowing and the output will be almost connected to ground it will be 0. So, this will be a naught operation if it is 1, it is 0, if it is 0, it is 1. So, this is NAND so, in diode transistor logic used to use diode and transistor like this to build circuits.

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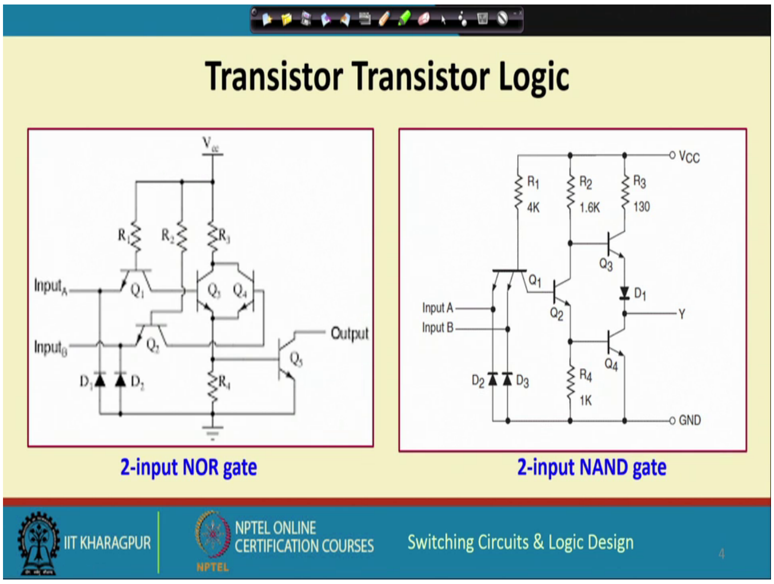

Then came transistor transistor logic where diodes were replaced by transistor, which made it switch faster see, I am not going into detail of the explanation this is these circuit diagram for 2 input NOR, this circuit diagram of a 2 input NAND let us say NAND gate. So, so whenever I mean at least 1 of the inputs are at 0. So, this emitter multi emitter transistor, this emitter would be conducting this would force this transistor to be off and then, it would force this transistor to be conducting and VCC will come to the output will become 1.

So, this is roughly how it used to work, I am not going into the detailed operation of this, but I am just showing that in TTL there are so, many resistances and transistors bipolar transistors that are used to realize the basic gates ok. These TTL's are used for SSI and

NSI level logic at 1 point in time, but today you do not see this kind of circuits anymore ok.

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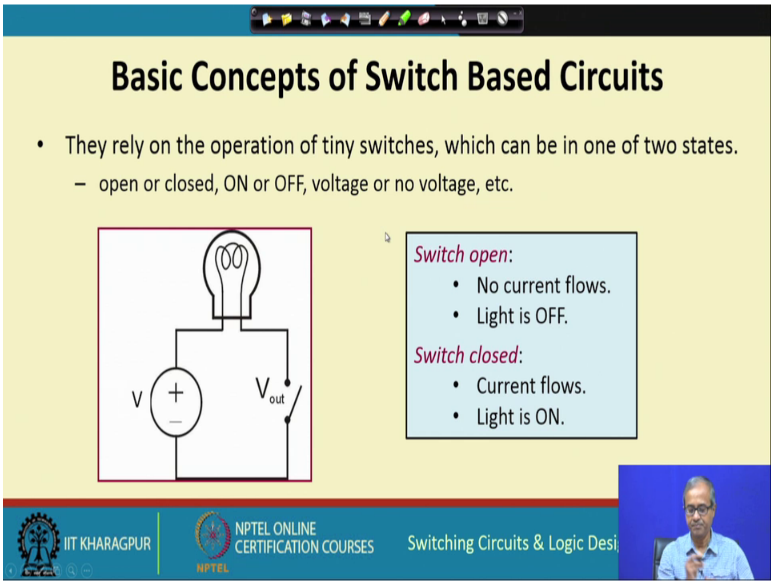

Today, as I said that most of the circuits we see is based on the CMOS technology and, CMOS technology is designed based on the premise of a switch electronic switch, a switch closing and a switch opening. Let us try to understand the concept, so called switch based circuits, they rely on the operation of miniature switches tiny switches, switches can be in 2 states, they are either open or closed.

So, you know how are switch is so, an equivalently I am showing a bulb connected in a circuit with a power supply and a switch. So, if this switch is this switch is open no current is flowing bulb is not glowing, but if the switch is closed current will flow and the bulb will glow. So, you see in this kind of switch based circuits, there can be distinctly two states switch open state and switch close state. So, in one state current is flowing and the light is current is not flowing and the light is not glowing off in the other state, current is flowing and the light is on right ok.

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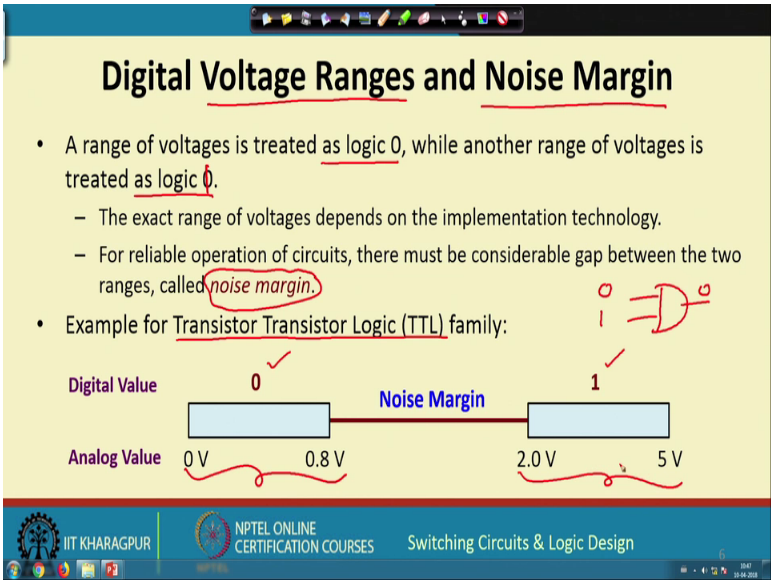

So, let us from here let us now look at some relevant issues, when we are trying to design gates. Let us consider suppose I am we are trying to design a (Refer Time: 10:08) let us an AND gate. So, are applying some input so, inputs are typically in the form of voltages, but in digital domain in binary we say it is 0 or 1. And the output will be something that will be 0 for an and gate.

Now, when I say 0 or a 1 what does that mean 0 can mean it is a low voltage, 1 can mean it is a high voltage, but well you may ask this low and high are very subjective terms how low or how high. So, so how low the voltage should be so, that the gate can treat the input as 0 and, how high the input should be the voltage. So, that the gate treats the input as 1.

These are some issues that need to be talked about. So, we are talking about something called voltage ranges and noise margins. So, I just now said with this example, a range of voltages is treated as logic 0 while some other range is treated as logic so, this should be 1 logic 1. Now, the exact range of voltages it of course, will depend on the logic family what kind of logic family you are using and, for reliable operation there should be sufficient margin between the 2 levels because, your electronic circuits are never perfect. There will be small variations in their operation and performance.

So, if your logic 0 and logic 1 are sufficiently spaced there is a lot of gap in between, then even in the presence of small variations in performance and the parameters the circuits will continue to work correctly ok. So, you see here I am showing an example, which is an example that pertain to the TTL family transistor transistor logic, here the digital value 0 and 1 are represented by the voltage range 0 to 0.8 volts and 2 volts and above.

These are the ranges of voltages to represent 0 and 1 and, whatever is there in between greater than 0.8 volt and less than 2.0 volt. This is considered as an invalid voltage range and this is the so called noise margin ok, because of some external noise a 0 should not become 1 or 1 should not become 0, there should be sufficient gap in between and this noise margin this ensures that.

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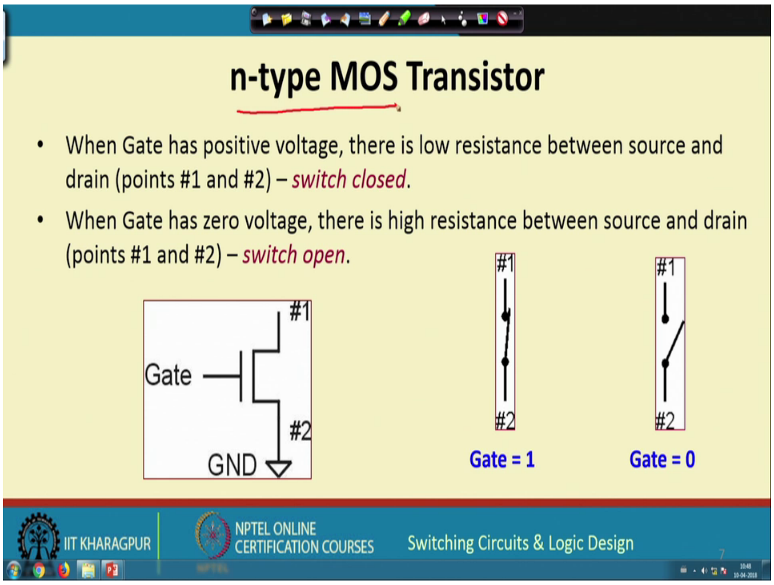

Let us now come to slowly towards CMOS complementary MOS. So, in CMOS we have 2 types of transistors n type and p type, without going into the detail just look at the functionality, we have n type and p type transistors. So, when you talk about n type metal oxide semiconductor or MOS transistor, the schematic diagram is like this is how the transistor looks like. There are three terminals gate and the other two terminals are called source and drain. So, when we apply a positive voltage on the gate, this switch is closed like is shown in this diagram. The switch is closed this is the equivalent circuit and between points 1 and 2 there can be a current flowing.

But if gate is 0 voltage the second scenario this transistor get non conducting and, there will be no current between 1 and 2. So, equivalently I can say that this switch has become open. So, for n type MOS transistor, when we apply gate 1, 1 means high voltage switch is closed if we apply 0 switch is open, but for p type transistor the situation is exactly reverse.

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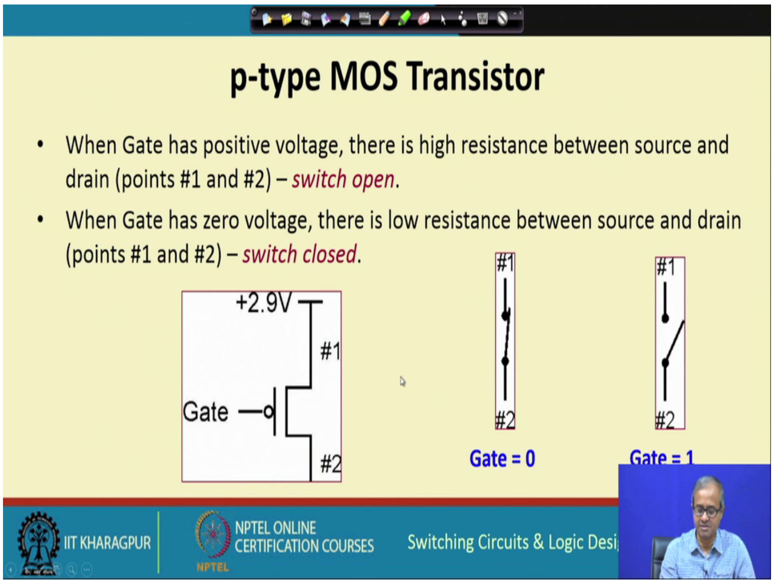

For a p type transistor which is represented like this, there is a small bubble here this indicates p type here, when the wherever here the positive voltage can many thing here I am showing as plus point 2.9 it can be higher also 5 volts also. So, here if the gate is low voltage 0 then it is conducting, but if the gate is high then it is non-conducting.

So, the behavior of the switch is just reverse, if the gate has positive voltage switch is open if the gate has 0 voltage the first 1 the switch is closed right. So, the behavior of the p type and n type transistors are reverse with respect to the switching behavior.

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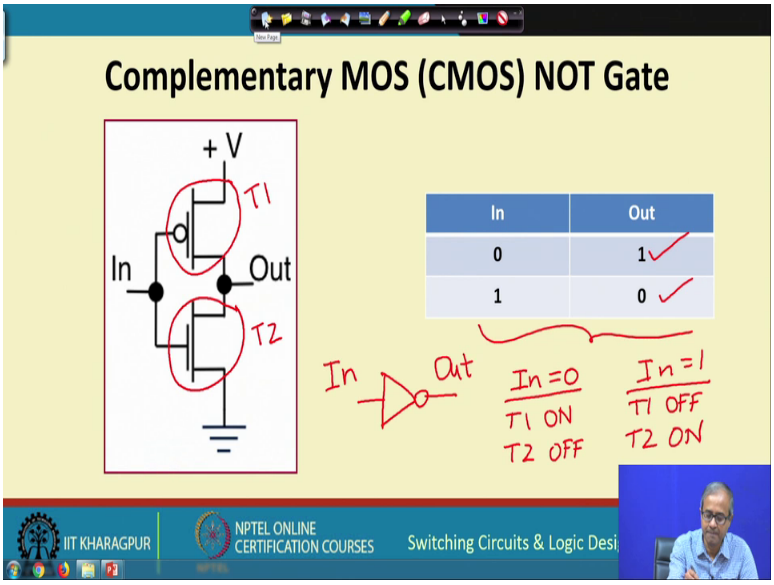

Now, let us come to CMOS circuits so, how was CMOS gate is built. So, let us come to the simplest circuit which show CMOS not gate. So, here the input is in the diagram the output is out. So, the truth table will be like this for a not gate 0 will become 1, 1 will become 0 let us see how this circuit works.

You see there are 2 transistors that are connected, 1 is n type transistor other is a p type transistor. Let us call them T 1 and T 2. Let us suppose my input voltage is 0; that means, low voltage. So, for input voltage 0 what we have seen the n type transistors would be off and a switch will be open and p type transistor it will be on. So, T 1 will be on and T 2 will be off. So, what does this mean T 2 is off means from out to ground there is no connection it is off, but this is on means plus V is connected to the output, which means output will be high voltage that is why output is one.

But if your in is 0 in is 1 now, the reverse will happen your T 1 will become off and T 2 will be come on because, T 2 is on now out will be connected to ground it will be low voltage so, it will be 0, it works as a not gate this is how a CMOS not gate works ok. So, other kind of gates are also fairly easy to build let us say a NAND gate.

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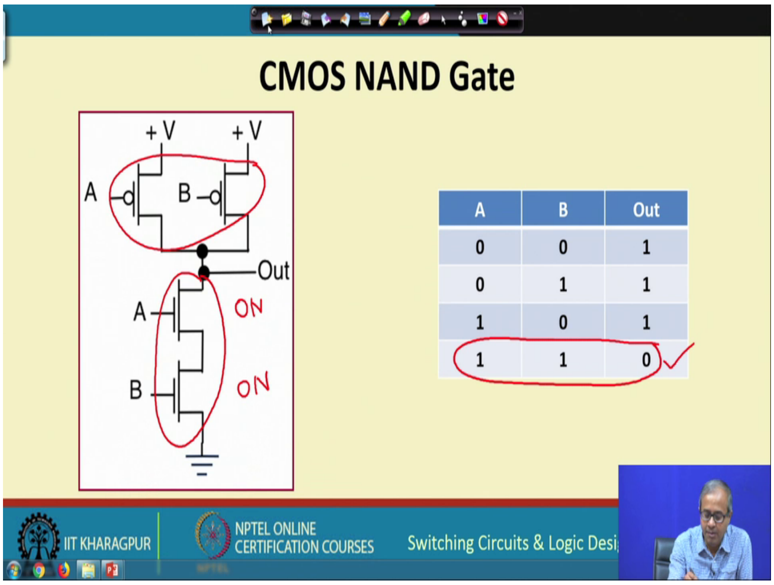

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate will require 4 transistors as we show in this diagram, 2 n type transistors here and 2 p type transistors here this is the truth table. So, when let us consider this last row first when both the inputs are 1 and 1 then what will happen.

This both this pull down transistors will be on and, this will be off because this are on from the output to ground there will be a path. So, output will become 0 output will become 0 right, but if you consider any of the other scenarios 0 0 0 1 or 1 0 here at least one of these 2 transistors will be off let say B.

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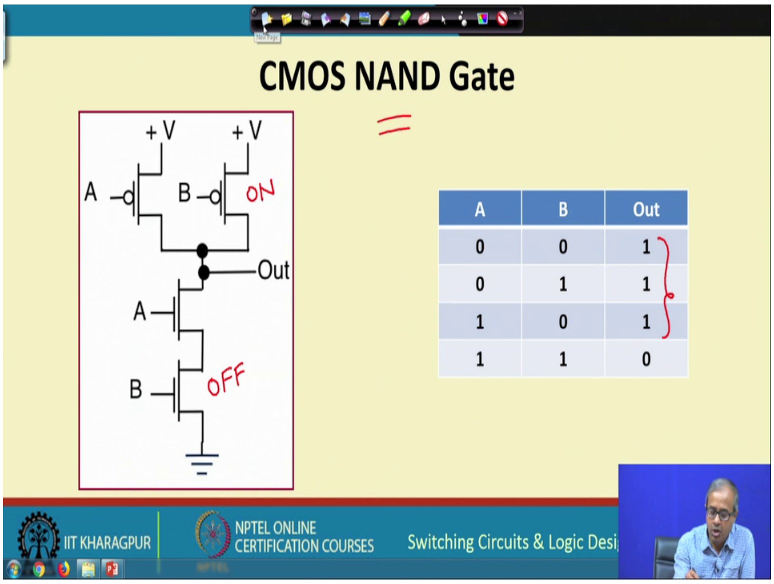

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

So, one of them will be off and at least one of these 2 transistors will be on. So, because 1 of A and B are off one of them is 0 at least. So, from output to ground there will be no path, but because one of at least one of these 2 transistors on from plus V to out there is a path. So, output will be high so, output will become 1.

This is your NAND function right. So, this is how this NAND gate works in CMOS, not gate operation is similar just the structure of the circuit will be little different it will look like this. So, these p type transistors are coming in series and n type transistor are coming in parallel.

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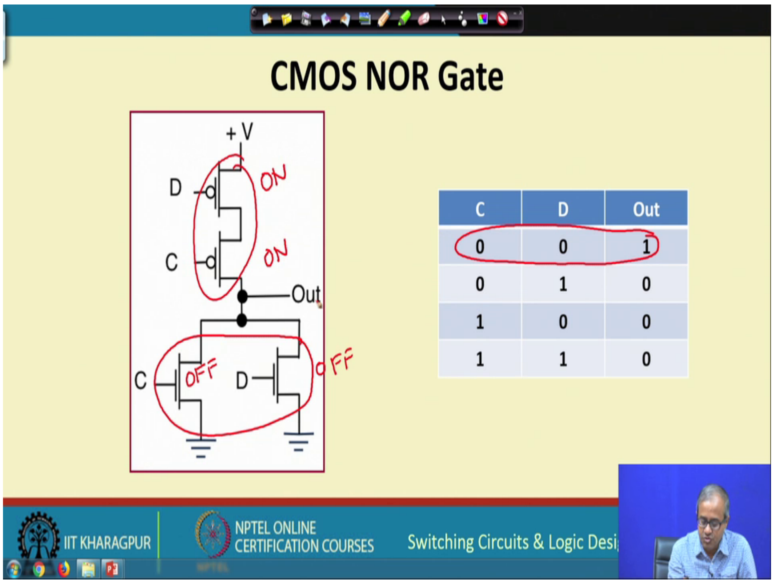

So, here again you see when both the inputs are 0, 0 means what this is off. This is off both these are on this is on this is on. So, from output to ground there is no path, but from plus V to output there is a path. So, output will be 1 output is 1.

But for any other condition you can check at least one of these to n type transistor should be on because one of them is 1. So, output to ground there will be a path output will be low and, both this transistors are not on so, plus V to out there is no path. So, this is not operation ok. So, it is easy to verify that it works. So, here I am assuming these transistors to be just switches, I am not looking into the other electronic characteristics of the most transistors, just functionally how it works as a gate ok.

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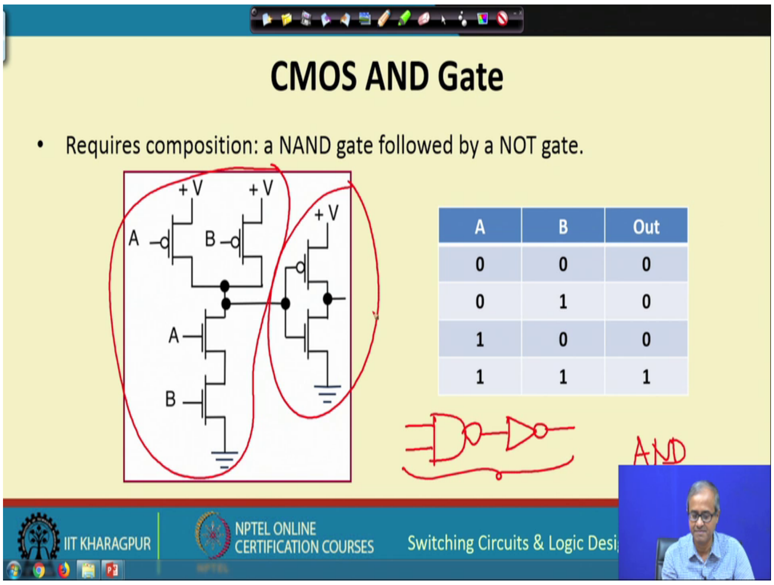

Now, when you want other type of gates for example, and well in CMOS you cannot directly implement an AND gate. So, what we have to do, you have to first implement a NAND gate followed by a NOT gate. So, in CMOS you remember in CMOS it is much easier to design a NAND gate more difficult to design a NOT gate more difficult design an AND gate.

You see this is an AND because what you have done a NAND followed by a NAND means what AND followed by NOT 2 NOT 1 after the other they cancel each other it becomes AND ok. So, CMOS and gate will be 1 NAND gate followed by a NOT gate.

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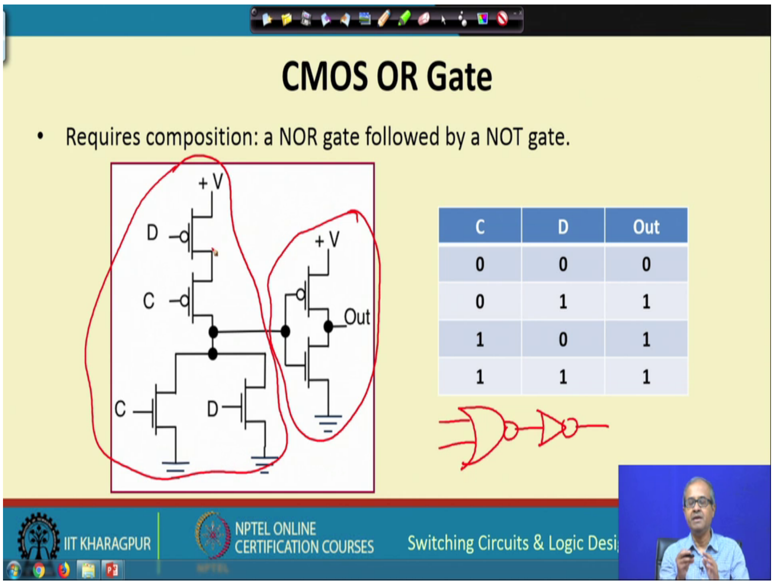

Similarly NOR gate so, OR gate will be NOR gate followed by a NOT gate. So, there will be a NOR gate followed by a NOT gate this is our. Now, this concept can be extended to any number of (Refer Time: 21:48) you can see instead of 2 transistor CD, you can connect many of them in parallel, instead of CD you can connect many of them in series. So, you can have a multi input NOR gate similarly NAND ok.

So, here I am not going to the detail of CMOS designs, but just giving you some idea that in CMOS how you can build gates and the advantage of CMOS is that in modern day technology, you can build these CMOS transistor or you can manufacture the CMOS transistor, in a very small dimension because of which in a chip you can pack. So, many gates today, you can pack close to a billion of transistors and NAND gates in a chip. So, CMOS gives you that big advantage. And in the CMOS design you do not need any resistances and any other components diodes these kind of things are not required because, resistances typically require much more area to fabricate in a chip here, you need only the transistors ok.

So, with this we come to the end of this lecture, where we had a look at some of the logic families. In the next lecture we shall be continuing a little bit more on CMOS and, then we shall be talking about a couple of unconventional technologies. These technologies are coming up they can also be used to design, digital circuits and gates and we shall be looking at those things.

Thank you.