

Switching Circuits and Logic Design
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Lecture – 51
Analog-to-Digital Converter (Part III)

So, we continue with our discussion on Analog to Digital Converter. If you recall what we discussed in the last lecture, we looked at some of the various techniques for AD Conversion. We started with the flash AD Converter, which was very simple in concept, very fast, but requires lot of hardware, lot of comparators, lot of resistances and also a priority encoder.

Then he looked at some of the counter based AD Converter: one was based on an up counter other was based on an up-down counter. Now in both of these methods, if the total number of bits is n , the number of steps can be 2 to the power n . So, in the worst case, the counter has to count from 0 up to 2 to the power n . So, the worst case conversion complexity was 2 to the power n clock cycles.

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(d) Successive Approximation Type ADC

- The principle of operation is analogous to *binary search*.
 - Suppose we are searching for a number (here V_{in}) in a sorted list.
 - We look into the middle of the list – effectively the size of the list reduces by half.
 - For 2^n steps, the number of steps required is only n .
- What modifications are required?
 - We use a *successive approximation register (SAR)* instead of a counter.
 - The SAR emulates binary search.
 - For example, in 4 bits it starts with 1000 (i.e. 8).
 - If the input is smaller, the next value is set as 0100 (i.e. 4).
 - If the input is larger, the next value is set at 1100 (i.e. 12).

The slide includes a diagram of a binary search tree. The root node is 1000 (representing the value 8). It branches into 0100 (representing the value 4) and 1100 (representing the value 12). A handwritten n is written below the tree. To the right, there are handwritten annotations: a bracket from 8 to 15, and a bracket from 4 to 12, with arrows pointing to the nodes.

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Now, today we shall be discussing in the third part of our lecture. We shall be discussing a new technique, another technique of counter-based AD Conversion. This is called Successive Approximation Type ADC. Let me first intuitively tell you that what we are trying to do in this kind of a converter. See here, we have 2 to the power n steps; the

basic idea is follows that we do not start with 0 and count up up up till you reach the level of the input voltage. Rather we start with the middle 0 to 2 to the power n . We start with 2 to the power n minus 1 , that is the middle, we start with a middle value and check whether that middle value is greater than or less than the input voltage. If it is less than we have to move further up, if it is greater than we have to move below.

So, in this one comparison, we have reduced the size of the total list to half. So, either we have to look at the upper half or the lower half. So, we repeat the same process. Suppose we see that we have to go to the upper half, we again look at the middle of the upper half. So, again with respect to the upper half, we have to look into the upper half of that or the lower half of that. So, the size of the list is becoming half at every step. So, the good thing here is that, instead of 2 to the power n comparisons or trials, we require only n trials this is a very big advance.

So, let us look into this in detail. This method is called Successive Approximation Type AD Converter. Now, for those of you who are familiar with this method of binary search in software, so this method does something similar to that, so if you have a sorted list of numbers. And if you want to search for a number you start with the middle, so you take a decision either to look into the left side or the right side, again look into the middle of that half and so on. So, for n numbers, the complexity of searching becomes $\log_2 n$ same thing happens here ok.

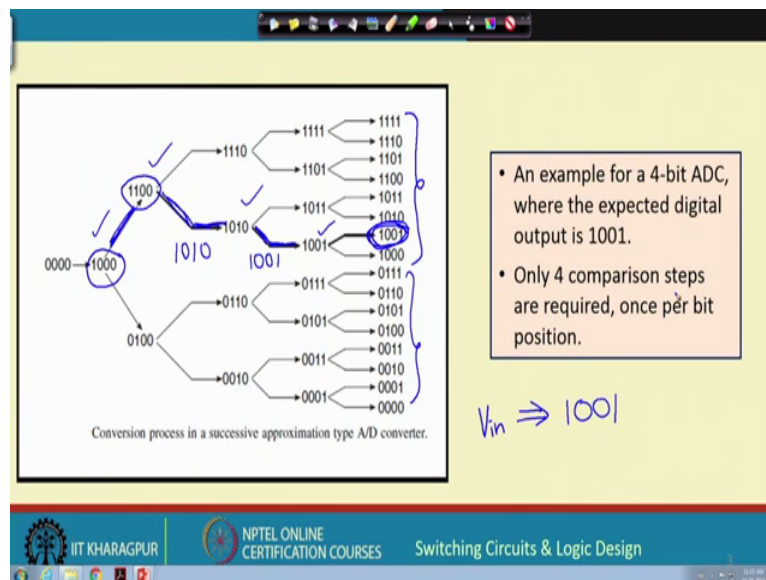
So, here as an analogy you can assume that the number we are searching here is the input voltage ok. So, we start with the middle of the list as I have said, and after comparing the middle of the list, we have to look at either the upper half or the lower half. And as I said, if there are 2 to the power n steps, the advantage again is that number of steps required is reduced to only n . So, what modifications are required to have this? See earlier, we used a counter either an up counter or an up-down counter. Here we use a modified version of a counter not exactly a counter. This is something called a successive approximation register, which simulates this binary search in hardware. Let's see how it works.

Let us take an example of a four-bit successive approximation register. We start by making the most significant bit one; that means, $1\ 0\ 0\ 0$. So, in decimal what does $1\ 0\ 0\ 0$ mean ? It is 8 . So, we have a range from 0 to 15 . So, 8 represents approximately the middle point, so we search the middle. Then we check the output of the comparator,

whether the input value which you want to convert is less than or greater than this value. If it is less than, if you have to go down what we do? We change this 1 to 0 and set the next bit to 1, but if we find that it is input value is less, input values greater, we have to move up. So, we leave this bit as one we set the next bit to 0.

So, we set the next bit to 0 always, but either the current bit we reset to 0 or leave it as it is. You say, 0 and 0 0 means 4, which is the middle point of this half and 1 1 0 0 is 12 which is the middle point of the upper half. This process we go on repeating ok. So, if there are n number of bits in this word, the number of steps we required this will be n only. So, instead of 2 to the power n, we have a technique here, where you require only n number of steps right.

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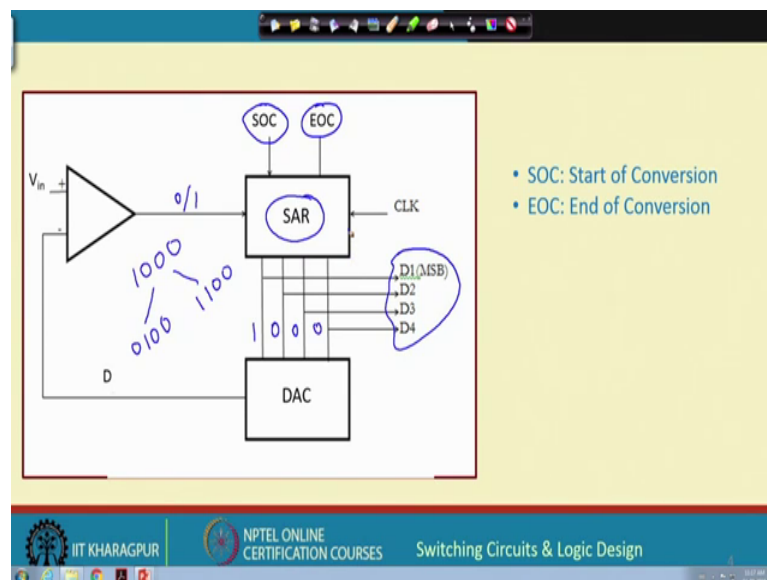


Let us pictorially show it in terms of a decision diagram like as shown in the left. So, as I said for a 4-bit converter, I am taking the example of a 4-bit converter. We start with 1 0 0 0.

Suppose the input voltage V in that we have applied that corresponds to the digital output; let us say 1 0 0 1. So, 1 0 0 1 is my expected output. The way the searching will proceed is as follows: you first make a comparison here, the output of the comparator there will be a comparator which will be comparing the current voltage from AD Converter with the input voltage. If we see that the V_{in} input is greater then, we have to move upwards, no you have to follow this link.

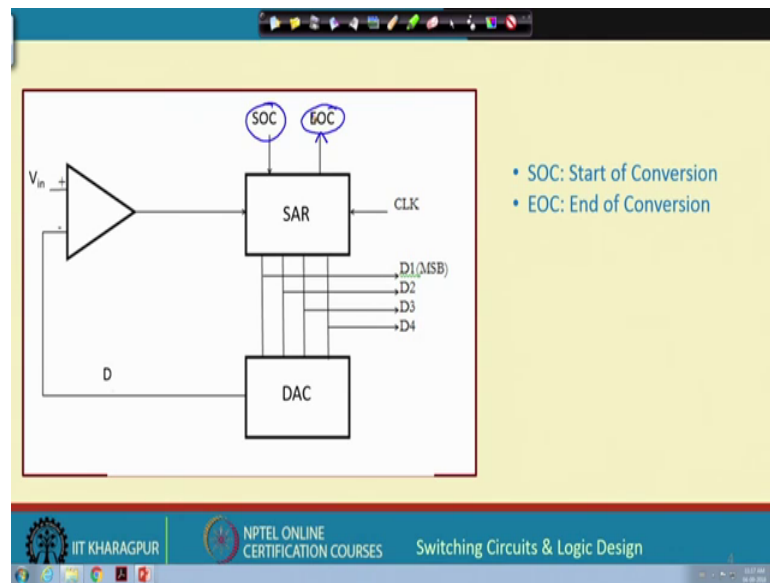
And the next data you have to compare is 1 1 0 0, which is 12. This will be half of the upper half right. This is the lower half, this is the upper half. Here we check and find out that the input voltage is less because it is lower. So, you will be following this path, what you do? See since you are moving up in the first case. This one remained as one, the second bit was made 1, 1 1 0 0. But at the next step if you see that it is less, what to do? You leave the first 1 as it is. The current one you reset it to 0, next bit you set to one, so it becomes 1 0 1 0. Then again there is a comparison you find that input is less, you follow this path. So, again the previous bits remain, the current bit which are set to 1 is reset to 0, the next bit is set to 1. 1 0 0 1. And here you finally, see it is greater and you arrive at the final value.

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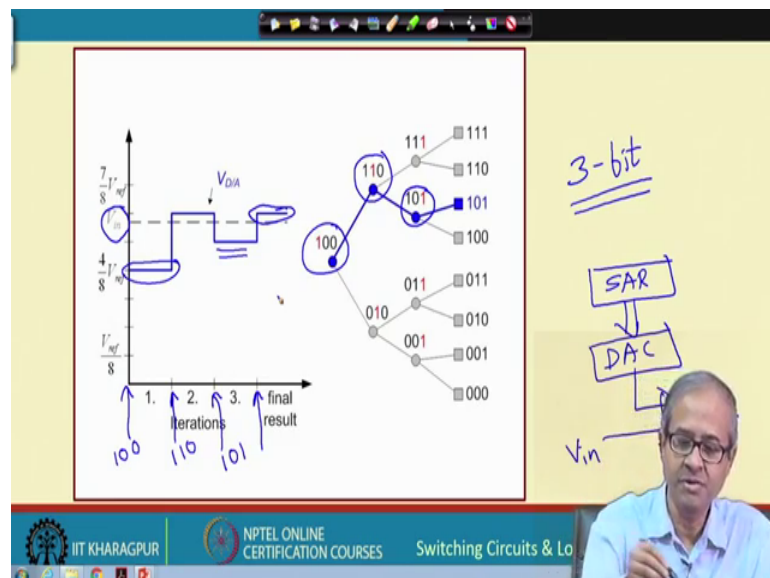
So, you see you require 1 2 3 and 4; four comparison steps only right. So, only four comparison steps are required to find the final digital value. Let us see the overall schematic now. The schematic looks very much similar to a counter type AD Converter the only difference is that here, instead of a counter we use a successive approximation register. Well, you just ignore this convention so which is msb lsb these are the 4-bits. So, 4-bits as I said we start with 1 0 0 0, the corresponding output of the AD Converter is compared by a comparator, with the input voltage depending on whether the output voltage of the comparator is 0 or 1 the successive approximation register takes the decision, because you start with 1 0 0 0. So, if the output is 0 means V_{in} is smaller you reset this to 0 to make the next bit 1.

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If it is 1 means V_{in} is greater, then you keep it 1 make the next bit 0 and you continue this. There are two additional signals as you can see Start of Conversion and End of Conversion. So, at the beginning when you want to start a conversion you set this Start Of Conversion signal to 1. So, this Successive Approximation Register will be initialized to 1 0 0 0 and the process will start and after the conversion is over the end of conversion which is an output signal this will be activated.

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So, you know that the conversion is over right. So, conceptually this is very simple. So, let us take a very small example of a 3-bit converter and see that how the signal changes with time, while the conversion is going on.

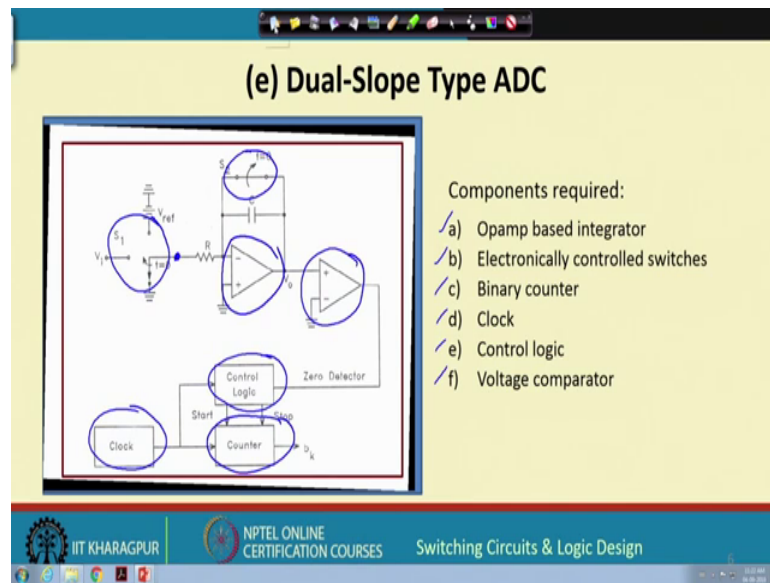
Suppose, I am showing the input-output curve; so along the x-axis, I am showing number of iterations and along the y-axis is the output voltage of the AD converter. Because we have the AD converter, successive approximation register is feeding the data to the AD converter. And this AD Converter output is compared with V_{in} . So, this output of the AD converter, we are plotting along the y-axis. And suppose this is my input voltage V_{in} .

So, the first iteration we shall be starting with 1 1 0, this corresponds to 1 0 0, the first iteration here. So, you see this is the level of the voltage it is half of the full scale 4 by 8 V_{ref} , this corresponds to 1 0 0. Then you compare with V_{in} and find that well V_{in} is greater, so you have to move up. So, the next value will be 1 1 0. So, in the second iteration here you put 1 1 0.

So, 1 1 0 will be equivalent to a level like this 6 by 8 V_{ref} . So, here you see V_{in} smaller V_{in} is lower than this. So, you in the 3rd iteration you reset this 1 to 0, make the next bit 1; 1 0 1 is 5, it is the lower one this one you find V_{in} is greater. So, in the last step, means you will be moving up and the final result will be 1 0 1; this 1 0 1 is the final result.

So, you see during conversion the output of the AD Converter will fluctuate widely, ok. Unlike a simple counter type, where the voltage rises steadily from 0 up to the input voltage level, but here since you are doing something like a binary search the voltage level will fluctuate like this and then it will stabilize ok. This is how this successive approximation AD converter works, ok.

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Fine, now the last kind of converter that you want to talk about here is something called Dual- Slope Type AD Converter. Now dual slope type AD Converter is accurate is quite accurate. But the problem is that because you have some op-amp based circuits you are using here speed of operation is a little slower, ok. Let us try to understand how it works.

These are the components required as you can see, there are 6 things required, which you can identify in this diagram. Op-amp based in the integrator: I shall talk about this this is your operational amplifier. Then you have a binary counter, this is your binary counter, you have a clock, you are applying a clock, you have some control logic. Of course, some control logic you have a voltage comparator, this is your comparator. And you have some electronically controlled switches; there are 2 switches 1 is this S 1, other is this S 2, the switch S 1 works as follows: This input of this op-amp, this point is either connected to an input voltage from here or is connected to a reference voltage out here.

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(e) Dual-Slope Type ADC

Components required:

- Opamp based integrator
- Electronically controlled switches
- Binary counter
- Clock
- Control logic
- Voltage comparator

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So, it switches like that and the second switch S 2, this is just an on-off switch, either it is connected or not connected, ok. Let us very briefly talk about how an op-amp based integrator works without going into the mathematical details.

Well, you have already seen how an op-amp can be used as an amplifier, non inverting and inverting. Now in an integrator, in this feedback instead of a resistance, he use a capacitance. So, this looks very much similar to a inverting amplifier, i f this is V in this is V out it like this. So, here what happens, well again without going into the derivation, if we look at the output voltage suppose initially the capacitor is discharged there is no charge because this point is at 0 Volts, this because, other point is grounded. So, V o will also be 0. So, if you just plot V 0, I am just plotting V 0.

This is the 0 level. So, it starts with 0. Now with time with a time constant of R C, this this capacitor will go on charging and because it is inverting it will go in the negative direction, ok. This is how this integrator works, right. And just one point to note is that this slope of this curve or this that means that within a particular time T, how much this voltage drops down to; this will be proportional to the input voltage. This is something you should keep in. Whatever voltage you are connecting, the rate of change of the output voltage will be proportional to that. So, we are basically exploiting this principle, ok.

So, let us move on we will be explaining how it works.

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- Principle of operation:
 - Integrates an unknown input voltage (V_{IN}) for a fixed amount of time (T_{INT}), then de-integrates (T_{DE-INT}) using a known reference voltage (V_{REF}) for a variable amount of time.
 - Conversion result is insensitive to errors in component values. Errors introduced during the integration cycle gets cancelled out during the de-integration phase.

$\frac{V_{IN}}{T_{INT}} = \frac{V_{REF}}{T_{DE-INT}}$
 $T_{INT} = \text{fixed}$
 $T_{DE-INT} = \frac{V_{IN}}{V_{REF}} \propto V_{IN}$

So, just if you move back once, here we are applying a reference voltage or we were applying an input voltage, ok. Now the idea is as follows: So, we are showing the output voltage; well actually this is actually negative we were showing the positive direction is actually negative way into our plotting. So, this is the output of the integrator, this is V_{INT} . We are saying ok, this is the integrator, the output is V_{INT} . So, the operation process like this.

So, initially at time T equal to 0, we connect the input unknown voltage to be converted at the input. We connect V_{IN} in the input and we allow the integrator to operate for a fixed time duration T_{INT} ; T_{INT} is fixed, ok. So, the voltage will change and will reach a certain point here. So, after this T_{INT} , we connect the input now to the reference voltage; reference voltage is a fixed reference voltage which is given. And we measure after how much time now the voltage will go down, because reference voltage has a different polarity.

So, if one is positive other will be negative right, the polarities are different.

So, the output voltage of the capacitor will change in the reverse direction. So, we measure after how much time the capacitance value is reaching 0, right. Now the calculation is very simple first part of it the input voltage, whatever you are applying V_{IN} divide by this time, this is this level of voltage proportional to this. And in the second part the reference voltage divide by this time. So, if you just solve this time T_{DE-INT} will be proportional to V_{IN} by V_{REF} , now because V_{REF} is constant. This will be proportional

to V_{in} . So, if we can measure this time that will be our corresponding digital output. If we use a counter to count this time in some way that will be proportional to V_{in} , ok. This is how it works.

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- At $t < 0$, S_1 is set to GND, S_2 is closed, and counter is cleared to 0.
- At $t = 0$, conversion begins and S_2 is open, S_1 is set to V_{in} .
 - S_1 is held for a constant time interval T_{INT} .
 - Counter begins to count; resets to 0 after T_{INT} .
 - Output of integrator at T_{INT} is $V_{in} T_{INT} / RC$, i.e. proportional to V_{in} .
- At $t = T_{INT}$, S_1 is set to $-V_{ref}$.
 - The integrator voltage drops linearly with a slope of $-V_{ref} / RC$.
 - The comparator checks when the integrator output voltage crosses zero.
 - When it crosses zero, the counter value is the required D .

$$\frac{V_{in}}{T_{INT}} = \frac{V_{ref}}{T_{DE-INT}}$$

$$T_{DE-INT} = \text{fixed}$$

$$T_{DE-INT} = \frac{V_{in}}{V_{ref}} T_{INT}$$

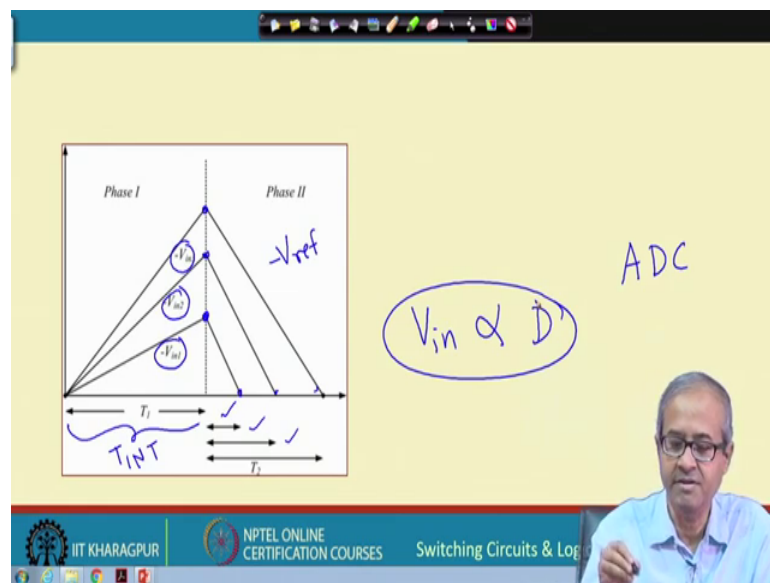
Let us see with respect to the diagram again, how the thing works, step by step we proceed starting from time T equal to 0, and we see how the electronic switches S_1 is 2 there are two electronic switches, how they are actually controlled, right.

So, initially, before the conversion starts we were saying T less than 0, so S_1 is set to ground. So, S_1 is set to ground S_2 is closed, which means the the capacitor is totally discharged and the output voltage V_0 out here V_0 is at 0 level here. At time T equal to 0, conversion starts, what we do, we open S_2 this is S_2 switch is open we disconnect it. So now, it works as an integrator, this is not there and S_1 is said to V_{in} we connect. This input to this input V_{in} out here and there is a control logic on a counter this counter will count up to a certain count value this will measure this T_{INT} .

So, we allow this to happen till T_{INT} time elapses, in T_{INT} the voltage will rise up to a level, which will be proportional to my input voltage V_{IN} right. So, the output of integrator will be actually V_{IN} , T_{INT} by $R C$, which is proportional to V_{in} because T_{INT} is constant $R C$ are also constant now. At this point, at time T_{INT} , we do two things: We said the switch to the reference voltage negative value; V_{ref} is a negative value we apply minus V_{ref} .

So, the output voltage of integrator will start increasing, will start reducing and this reduction will be carried out with a slope of minus V_{ref} by $R C$, this comparator out here it checks when the output crosses 0. And in the meantime, the counter is reset to 0 and the counter starts counting. So, as soon as the comparator output resets 0, the current value of the counter will be proportional to this T_{INT} . And this count value is the required digital output D that is how the dual slope AD Converter basically works, right.

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Now, just on last thing here; just here I am showing if the input voltages are changed. The first part we are using a constant time we call it as T_{INT} , right. The difference is that the slope of this curve will just be different; that means, the final value at the output of the integrator this will be different. But in the second part we are applying a constant reference voltage at the input so that the slope will be the same. So, the time it takes to cross 0 will be different either this or this or this. And if you use a counter to count and see after how long it crosses 0, that D will be proportional to my input applied voltage. So, I have a Analog to Digital converter starting with V_n . I have obtained a corresponding proportional digital output right. So, this is how this dual slope AD Converter works.

So, with this, we come to the end of this lecture. So, if you recall in this lecture, we looked at two different methods of AD Conversion: one was the successive approximation type, which is basically one classic example of implementing binary

search in hardware and the second method was a method called Dual Slope AD converter. Now let me tell you, I just mentioned dual slope is more accurate; now, the reason why it is more accurate is that well in an integrator in an op-amp circuit there can be errors in the values of the resistances and the capacitances, you cannot get a component with precisely a value which you want.

So, even if there are variations you are doing it in two phases, one is integration then D integration; the tolerance of the differences in the value they cancel out. So, the final result is independent of the variation in the component values that is why we say that the dual slope method is more accurate.

So, with this, we come to the end of this lecture.

Thank you.