

Switching Circuits and Logic Design
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Lecture - 50
Analog-to-Digital Converter (Part II)

So, we continue with our discussion on Analog to Digital Conversion in this present lecture. So, this is the part 2 of our lecture on AD converter let us look at some of the general characteristics first, there is something called “Resolution”; we want to talk about for a A D Converter first. Now just like for a D A converter, when we give a digital input and obtain the analog output we said that the step height was a measure of the resolution.

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Resolution

- The least significant bit of an analog-to-digital converter (ADC) gives the *resolution*.
- Related to full scale if the ADC is linear.
 - $LSB = \frac{A}{2^n}$ for an n -bit ADC.
 - For a linear 8-bit ADC with a 1V full scale input, Resolution = $1/2^8 = 3.9 \text{ mV}$ (0.39%)

$\frac{1}{2^8} V = 3.9 \text{ mV}$

$\frac{A}{2^n}$

The slide also features a graph showing a staircase-like output signal (D) versus an analog input signal (V_A). The graph illustrates how the output remains constant for a range of input values and then jumps to the next level, representing the discrete steps of a digital output.

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So, here also what is the minimum change in the input voltage that will result in one step jump in the output because here the output is digital. So, you see here our input is analog voltage V_A, but our output will be digital. Digital means there will be some voltage levels or digital levels. So, the output cannot be continuously changing they will be discrete.

So, as you change your inputs continuously your output will be changing in steps like; this. The resolution tells you that what this is your one step height. And what is the input voltage that corresponds to that change. So, you see if A is your full scale voltage of the

A D Converter. Then full scale voltage divide by the total number of steps A divide by 2 to the power n . This is defined as the Resolution. Let us take an example: suppose, I have an 8 bit A D Converter with a full scale voltage of 1 volt. Then full scale voltage 1 divided by 2 to the power 8. This many volts, this comes to 3.9 millivolts and so, this if you multiplied by 100, you get it as a percentage right. This is what your resolution talks about.

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Dynamic range

- Ratio between the minimum and the maximum amplitude to be measured.
- For a linear ADC the dynamic range is related to the number of bits (i.e. the resolution).
 - An 8-bit ADC has a dynamic range of 256.
- In case of large dynamic range some non-linearity has to be introduced.
- Commonly used terms:
 - n -bit resolution
 - n -bit dynamic range
 - *Example:* 8-bit resolution for a 12-bit dynamic range means that a signal in the range 1-4000 is measured with a resolution of 0.39%.

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Then comes the Dynamic range. So, what is the dynamic range of an A D Converter suppose, you see I have designed an A D Converter for some signal right. So, input there is an, there is an analog signal which is coming. So, I know that what is the minimum voltage level and the maximum voltage level in my analog signal. So, I am designing my A D Converter accordingly. So, the minimum and the maximum amplitude to be measured; that means, input the ratio between the 2 defines the dynamic range. Now there are a few things let me tell you.

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Dynamic range

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- For a linear ADC the dynamic range is related to the number of bits (i.e. the resolution).
 - An 8-bit ADC has a dynamic range of 256.
- In case of large dynamic range some non-linearity has to be introduced.
- Commonly used terms:
 - n -bit resolution
 - n -bit dynamic range
 - *Example*: 8-bit resolution for a 12-bit dynamic range means that a signal in the range 1-4000 is measured with a resolution of 0.39%.

Handwritten note: = 256

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So, for a linear A D Converter means the output and input are proportional. That is a linearity converter; the dynamic range can be calculated by the number of bits like for an 8 bit A D Converter will be having a dynamic range of 256. Because there are 256 so, when you divide the maximum voltage by the minimum voltage that will be equal to 256 right. This you can calculate for a linear converter if it is proportional, but for some application where the input is very large, then you need to just add some nonlinearity to the A D converter, but we are ignoring that for the time being; just mentioning that for large dynamic range some non linearity may be introduced.

Now, some terms that you resolution of 8 bits like, this I mentioned earlier. And dynamic range n bit dynamic range let us take an example: suppose we talk about 8 bit resolution and a 12 bit dynamic range, well 8 bit resolution means what, to just 8 bits of resolution we just now talked about earlier, 1 by 2 to the power 8 which comes to 0.39 percent. If you multiply it by 100 right, resolution of 0.39 percent and 12 bit dynamic range means, how many steps 2 to the power 12 means 4000 something 4096 and so, approximately 4000. So, range is 1 to 4000.

So, it means when you combine the resolution with dynamic range. It means that you specify a range, that I want to measure a range of 1 to 4096 with an accuracy or resolution of 0.39 percent both are important. One says that: what is the limit you are

measuring with and other one says what is the accuracy with which are measuring it ok. Dynamic range and Resolution both are important in that respect.

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The slide is titled "Conversion Time and Bandwidth". It contains the following text:

- How often can a conversion be done?
 - A few ns to a few ms depending on the technology.
- Input bandwidth
 - Maximum input signal bandwidth
 - Sample and hold input circuitry
 - Conversion frequency

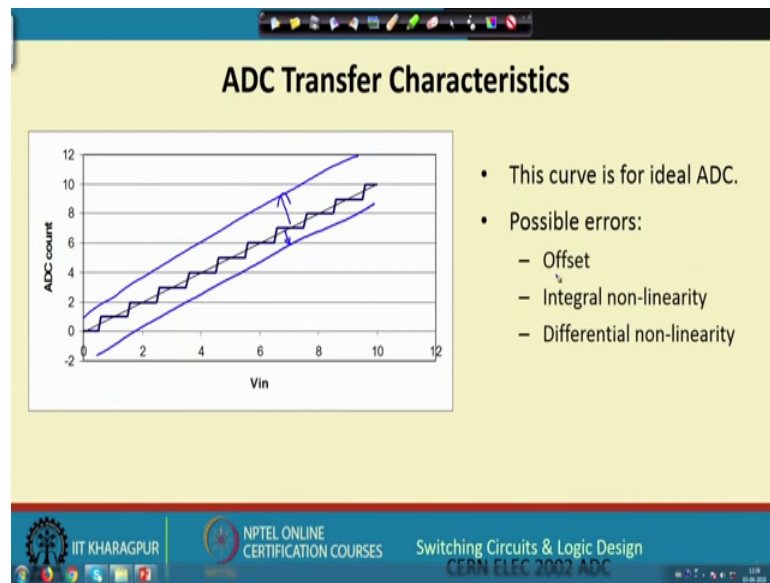
To the right of the text is a hand-drawn diagram of an ADC. It shows a rectangular box labeled "ADC". On the left side, there are three arrows pointing into the box, labeled V_A . On the right side, there are two arrows pointing out of the box, labeled D . Below the box, there is a small triangle representing a time interval Δ .

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Conversion time and Bandwidth Conversion time says that, suppose I have an A D Converter right. So, it depends on the design of the A D converter, how fast it can convert. So, suppose I am applying an Analog Voltage V_A in the output, I am getting a digital word D . So, how fast it can convert it can take a time Δ . Now depending on the technologies in which you are building this, the conversion time can be a few nanoseconds it can also be as low as a few milliseconds right.

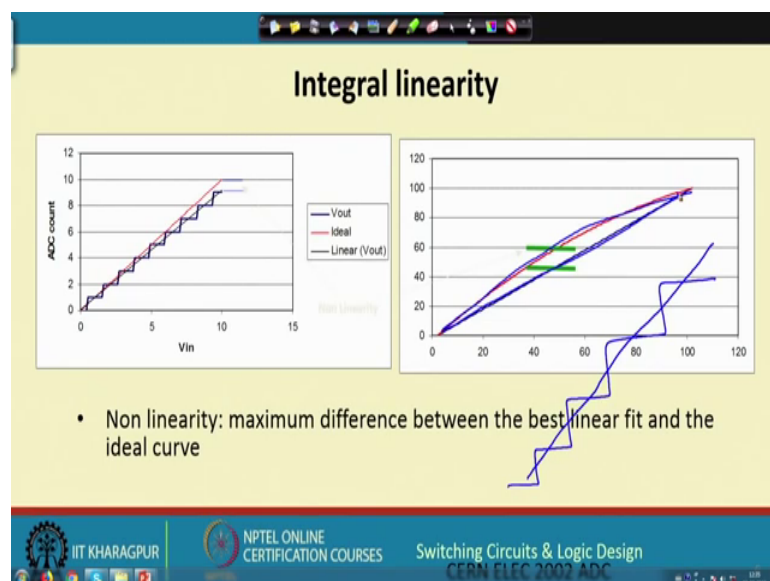
Secondly, you as I said earlier you will be using this sample. And hold circuit in the input that will determine the input bandwidth that, what is the maximum rate with which you can apply the inputs right the conversion frequency will depend on that. So, these are some of the parameters of an A D Converter. So, I am not going into the much detail of this.

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Fine let us, talk about ADC Transfer Characteristics for Analog to Digital Converter; I said that on the input side you have your input voltage and the output. You are getting a digital word. So, it will ideally it will be a step now there can be possible errors. Now, the first error is an offset error, offset error I already mentioned earlier with respect to D A converter is very similar that instead of this straight line. The curve is either getting shifted up or shifted down. There is a steady offset a positive offset or a negative offset, there can be an offset error now. Why this offset error, I mean occurs it depends on the actual technology with which you are building it.

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Fine, then comes the linearity or nonlinearity. Linearity means you see this step heights again quite similar to D A converter step height should be equal. But in this case, you may find that for some of the steps the heights may be may be unequal, which means you see the steps when you show like this, suppose I have the steps. So, if you join the middle point of these steps it will be like a straight line. So, the ideal case will be a straight line, as this blue line shows now. Because of this non-linear error, if you join the middle points it may show like a curve. As this red line shows, this shows the nonlinearity error right. So, this kind of nonlinearity error you can be there.

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Differential Non-linearity

$$1 \text{ LSB} = \frac{V_{\text{max}}}{2^n}$$

n - bit ADC

- Least Significant Bit (LSB) value should be constant but it is not.
- The difference with the ideal value should not exceed 0.5 LSB.
- How to check?
 - random input covering the full range.
 - frequency histogram should be flat.

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And there can be a differential nonlinearity, this is another kind of error. Differential Nonlinearity says that again the least significant value should be constant with respect to the output voltage. But it is not, but for a real A D converter for a for an acceptability converter. The difference from the idle value should not exceed half of the LSB value. Now typically how do we check, we apply a large number of random inputs covering the whole range now, the frequency histogram should be equal across all values.

But what will see, if there is a differential non-linearity that it will not be the same. Because ideal frequency should be flat like this black. One shows, but for differential nonlinearity you will see that it may vary ok. But these are some of the errors related to A D converter, you need not have to worry too much about these things now just remember that this kind of errors can take place.

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(a) Flash-type ADC

- This type of ADC provides the fastest conversion.
- Requires large amount of hardware.
 - For an n -bit converter, we require $2^n - 1$ comparators, 2^n resistors, and one 2^n -input priority encoder.
- We illustrate the design for a 3-bit ADC.

Comparator

V_1 — +
 V_2 — -

$V_1 > V_2, f = 1$
 $V_1 < V_2, f = 0$

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Now, let us come to the design of the different types of A D Converters. This is more interesting, the first kind of A D Converter design we talk about is something called a Flash Type any Converter. Now, let me tell you flash type A D Converter is the fastest type of A D Converter that is known, but the problem is that it requires too much hardware. Let us, see how flash type A D Converter as, I said it provides the fastest conversion. But it requires large amount of hardware in what way, suppose I have an n bit A D Converter I need $2^n - 1$ comparators; 2^n resistances and one priority encoder of length 2^n . Let us, talk a little bit about this well we talked about a comparator here right.

What is a comparator, this is not a digital comparator. Here what we are talking about is something of an analog comparator ok. Symbolically, it looks similar to an op amp, but this is not an op amp, this is a comparator. The way it works is that, the inputs at two voltages V_1 and V_2 . And the output is a digital output f the way, a comparator works is as follows. If V_1 is greater than V_2 ; that means, plus input is greater than, the minus input then the output will be one digital output. If V_1 less than V_2 output is 0 but remember that, when the inputs are equal then the output is not defined it may be zero or one doesn't matter. But it is defined when it is greater than or less than ok, this is how a comparator works. And priority encoder already you have seen earlier, what is a priority encoder. Let us see, how these things can fit in place to create an A D converter.

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The diagram shows a 3-bit ADC circuit. An analog input V_{in} is connected to a resistive ladder network. The ladder starts with a reference voltage V_{ref} at the top, followed by a series of resistors R . The nodes between the resistors are labeled A through G. Each node is connected to a comparator. The outputs of the comparators are connected to an 8-to-3-bit priority encoder. The encoder has three digital outputs: D_2 , D_1 , and D_0 . A handwritten note in blue ink says "3-bit ADC" and " $2^3 - 1 = 7$ ".

| A | B | C | D | E | F | G | D2 | D1 | D0 |
|---|---|---|---|---|---|---|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | X | X | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 |
| 0 | 0 | 1 | X | X | X | X | 1 | 0 | 1 |
| 0 | 1 | X | X | X | X | X | 1 | 1 | 0 |
| 1 | X | X | X | X | X | X | 1 | 1 | 1 |

Well on the left hand side. Let us, look at the design of a 3 bit. This is a 3 bit A D Converter. So, according to what we showed in the previous slide. We have 2 to the power 3 minus 1 7 minus then 8 minus 1 is 7 . There are seven comparators; there are n 2 to the power 3 , 8 resistances. And, we need a priority encoder with 8 input means actually 1 less 7 inputs. There will be output will be three now. Let us, see how this works, the first thing you see that I have a long resistive network starting a voltage.

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The diagram shows a 3-bit ADC circuit, identical to the one in the previous slide. It features a resistive ladder network with nodes A through G, each connected to a comparator. The comparators' outputs are connected to an 8-to-3-bit priority encoder, which produces three digital outputs: D_2 , D_1 , and D_0 .

| A | B | C | D | E | F | G | D2 | D1 | D0 |
|---|---|---|---|---|---|---|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | X | X | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 |
| 0 | 0 | 1 | X | X | X | X | 1 | 0 | 1 |
| 0 | 1 | X | X | X | X | X | 1 | 1 | 0 |
| 1 | X | X | X | X | X | X | 1 | 1 | 1 |

I have a resistive network like this. So, how does it work? So, how many resistance are there 1 2 3 4 5 6 7 8 talk about this point. What will be the voltage here ground here this is R. So, what is the resistance on top 1 2 3 4 5 6 7 7 R. So, if you look at this is V ref ok. V ref

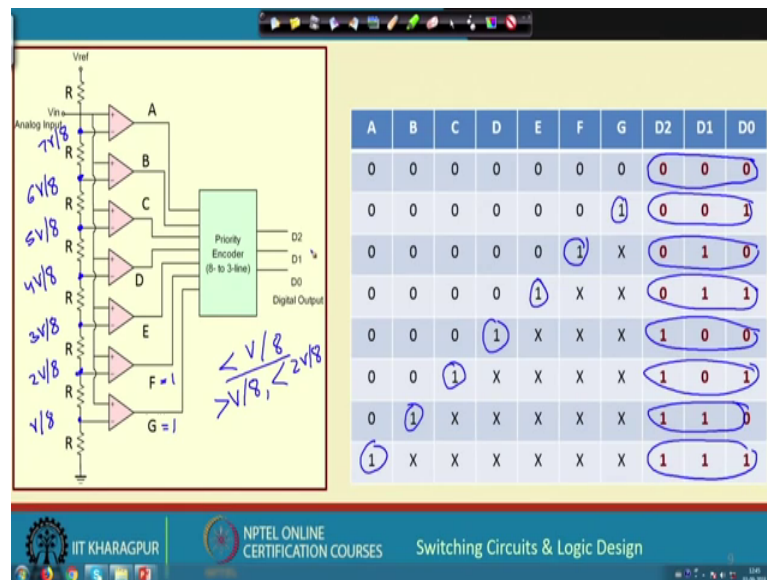
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The diagram shows a circuit with a resistive divider network connected to a priority encoder. The divider consists of a vertical chain of resistors labeled R, with an analog input V_{in} at the top and ground at the bottom. The nodes between resistors are labeled A through G. Each node is connected to the input of a corresponding priority encoder stage (A through G). The encoder has three digital outputs: D2, D1, and D0. Handwritten blue notes indicate that the voltage at node A is $V_{ref}/8$, at node B is $2R/8$, and at node C is $3R/8$.

| A | B | C | D | E | F | G | D2 | D1 | D0 |
|---|---|---|---|---|---|---|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | X | X | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 |
| 0 | 0 | 1 | X | X | X | X | 1 | 0 | 1 |
| 0 | 1 | X | X | X | X | X | 1 | 1 | 0 |
| 1 | X | X | X | X | X | X | 1 | 1 | 1 |

This is a resistance divider. So, the voltage here will be R divide by 8 R into V ref. So, the point here will be V ref I am just writing only V divide by 8. Voltage here it is 2 R and 6 R, on top this is 2 R and this is 6 R. So, now, the voltage will be 2 R divide by 8 right. So, it will be 2 V by 8 here this point. So, now, what I mean to say is that the voltage at this point would be V reference by 8 Voltage at this point.

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Will be 2 V by 8, here 3 V by 8, 4 V by 8, 5 V by 8 6 V by 8. And at this point 7 V by 8, this V is actually V ref right. Now, what are these comparators doing depending on the input voltage suppose input voltage is less than V reference by 8. So, what so in the plus inputs I am connecting the input voltage. V in analog input is connected to the plus inputs of the comparator and these voltages reference; voltages are connected to the minus inputs. So, if the plus input is less than all of them. So, the output A-B-C-D E-F-G will be all 0's. So, it will 0 0 0 0, in such cases the priority encoder is generating a digital output of 0 0 0. That is the lowest voltage level suppose now my voltage is greater than V by 8, but less than 2 V by 8. So, only the G comparator, G will be 1 all others will be 0 right. You see G is 1 all others are 0 and this is encoded as 001

Now, if is greater than 2 V by 8, but less than 3 V by 8, then G equal to 1, F will also be 1. But all others are 0 you see well if F is 1; obviously, G will be 1 that's, why I am showing it as do not care. Because it's a priority encoder if it is greater than 2 V by 8; obviously, it is greater than by 8 ok. So, in this case it is 0 1 0. Similarly if E is 1 is 1 means greater than 3 V by 8 then 0 1 1. If D is 1, D is 1 means greater than 4 V by 8 1 0 0 0. Then C means 5 V by 8 1 0 1.

Similarly, B is 6 V by 8 1 1 0 and if it is greater than 7 V by 8. A is 1, then 0 0 0. And this is priority encoder means, if a particular bit is 1 then the lower priority ones you need not see you can directly encode it. So, you see just using a resistive network, I have

generated all the reference voltages. And using so, many comparators I am comparing the input voltage parallelly with all these reference voltages. And whatever is the output coming using a priority encoder I am encoding it into a digital word.

So, see this conversion is fast, because it uses a single process delay of the comparators plus delay of the priority encoder that's it. There is no other delay in this conversion that. So, this is very fast, but the problem is that suppose, I want to design a 16-bit A D converter. So, you cannot afford to use 65000 comparators not possible ok. So, this can be used only for very small values of in right.

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(b) Counter-Type ADC

The diagram illustrates the Counter-Type ADC. On the left, a schematic shows the input voltage V_{in} connected to a comparator. The comparator's output is ANDed with a clock signal CLK to drive a counter. The counter's output Q/P is connected to a DAC, which outputs a voltage V_i . On the right, a graph shows V_{in} as a step function and V_i as a staircase function that increases until it reaches V_{in} . The x-axis is labeled 'counter stops' and 'no. of clock pulses'.

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Let us see more practical kind of converters which you can use for larger values of n . Let us look at something called a counter type A D converter. So, I am shown this schematic diagram on the left, here again we are using a comparator, but only one comparator. And we are using a binary counter there is a clock which is coming continuously. Let us see what happens this counter value is initialized to 0. Suppose it is a four bit counter we initialize to 0 0 0 0 and we are using a D A converter also. We already know how to design a D A converter. So, in this approach we are using a D A converter to design an A D converter ok.

The idea is very simple we initialize the counter with 0. We feed it to the input of the D A converter. D A converter generates D output, which is equivalent to 0, the lowest voltage you compare this lowest voltage with your input voltage that you want to convert. If you

see your input voltage is larger which means the output will be 1. So, when the clock comes this will be 1. So, the counter will count counter will become 1. So, D A converter will increase the output voltage by one step, again that voltage will be compared, if V_{in} is still larger the output of the comparator will be still 1; so, again counter will count by one more to.

So, in this way the counter will go on counting 0 1 2 3 4 and the output of the D A converter will also go step by step it will go on increasing. And continuously the comparator will be comparing that increasing voltage with your input voltage as soon as the D value or the output of the D A converter crosses the input analog voltage it will stop because the output will become 0 and the this and gate output will 0 and the counter will stop counting.

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(b) Counter-Type ADC

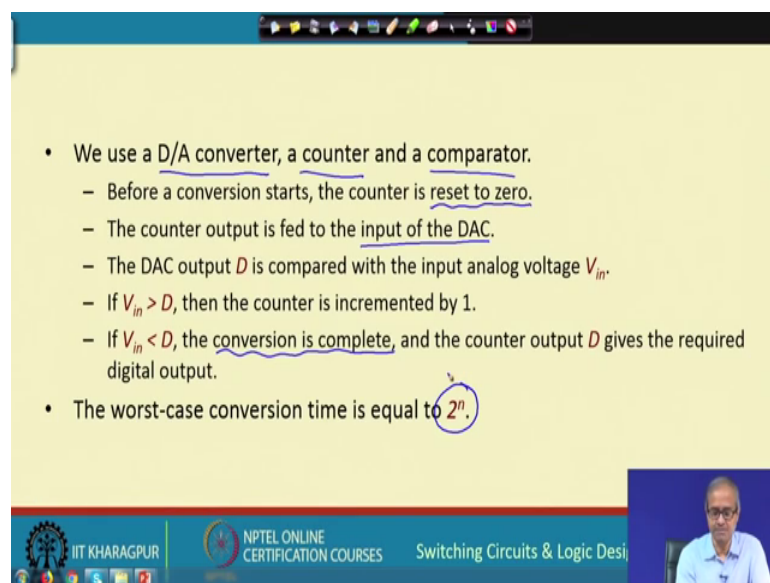
The slide illustrates the operation of a Counter-Type ADC. On the left, a schematic diagram shows an input voltage V_{in} connected to a comparator. The comparator's output is ANDed with a clock signal CLK to provide a clock signal to a Counter. The Counter's output D is connected to a DAC, which produces an analog output O/P. The DAC output is fed back to the comparator. On the right, a graph shows V_{in} on the y-axis and 'no. of clock pulses' on the x-axis. A horizontal dashed line represents the input voltage level V_i . The graph shows a staircase function where the output voltage increases step by step with each clock pulse. The counter stops at the 5th pulse, where the output voltage crosses the input voltage level V_i . Handwritten notes include $V_{in} \propto D$ and a circled $\frac{n}{2}$.

So, schematically you can show it like this the output of the D A converter. It will increase step by step as soon as it crosses this V_{in} . Let's say this is your input voltage level you have applied, whatever voltage you have applied as soon as it crosses the counter stops. And at this point whatever is the value in the counter that is the equivalent digital value in the for the D A Converter. This V_{in} well instead of calling it D; let us call this as D, this makes more sense V_{in} will be proportional to D. So, you are getting the value of D right 0 1 2 3 4, but the problem here is that in the worst case for an n bit

conversion the counter will have to count 2 to the power n times its an n bit counter. So, number of clock pulses required can be as large as 2 to the power n

So, you can see why I have said that flashed up converter was faster because everything was done in a single step, but here there is a clock you are applying clock maximum 2 to the power n times for a 16 bit converter. 2 to the power n can be about 65000. So, 65000 cycles may be required to complete the conversion right. So, whatever we have said this is actually mentioned here.

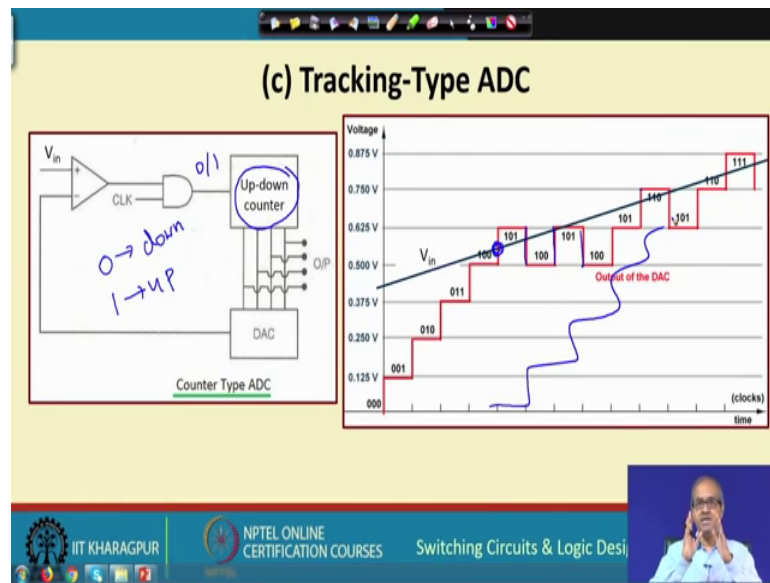
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- We use a D/A converter, a counter and a comparator.
 - Before a conversion starts, the counter is reset to zero.
 - The counter output is fed to the input of the DAC.
 - The DAC output D is compared with the input analog voltage V_{in} .
 - If $V_{in} > D$, then the counter is incremented by 1.
 - If $V_{in} < D$, the conversion is complete, and the counter output D gives the required digital output.
- The worst-case conversion time is equal to 2^n .

So, we use a D A converter, A counter and A comparator. Before the conversion starts, the counter is reset to 0, the counter output is fed to the input of the D A converter. And the D A converter output is compared to the input voltage that you are applying the input voltage is greater than the D A converter output. Then the counter increments by 1 if it is less than the counter does not increment anymore and conversion is complete. As I said the worst case conversion can be 2 to the power n time number of clock pulses.

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Now let us modify the design a little bit. When we move to a method, which is called Tracking Type A D converter. Let us see for a simple counting type A D converter. What we are doing we are having a counter starting from 0 we are counting up, up, up, up, up. And we are stopping as soon as we cross the level of the input voltage that count value will be my digital output.

Now, suppose what I do instead of a binary counter normal up counter we use a up down counter. Now, here we say that well we want to continuously track the input voltage we do not want to start counting from 0, every time one problem with the counting type converter was that you always start counting from 0 0 1 2 3 4. Suppose your input voltage is equivalent to a count of 1000. So, you will have to count 1000 times 1000 clock pulse next data you sample. Maybe it was 1005 again from 0 will have to count 1005 next sample value was let say 1001 again from 0 you have to count to 1001.

So, it was very time consuming. So, what I am saying is that suppose the input waveform is slowly changing. We know that from 1000, it can go up 2005 or say 995 not much change. So, why every time start from 0. If you remember the last count value, why do not you start from there either go up or go down. So, you use a up down counter instead of a normal up counter. So, your modified schematic will look like this you use an up down counter. And rest is very similar from the output of the D A converter. You use the comparator and the comparator output can be either 0 or 1 and similarly the output of

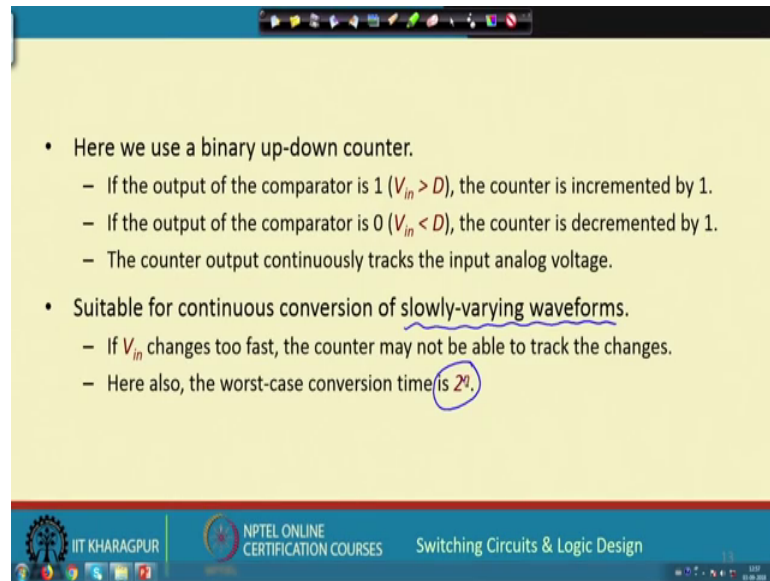
this clock will be 0 or 1. So, when it will be 0 it will be 0. If V_{in} is smaller ok, the D A converter output is larger. So, if D A converter output is larger I will have to reduce the value of the D A converter output. So, 0 means, I will be counting down, I will reduce the value of D A converter, but if it is 1, which means V_{in} is larger D A converter, output is smaller. I have to increase the D A converter value.

So, if it is 1, I have to count up. So, there is no concept of stopping the count. I am continuously doing it if it is 0, the count is counting down. If it is 1, it is counting up this is called Tracking Type. Because the D A converter output tries to track the variation of the input waveform continuously. So, as this example shows suppose this is my input voltage this straight line just an example: suppose the input voltage is changing linearly in a straight line. And well the first time you start with 0 0 1 2 3 4 5 here you cross. So, here you have 1 conversion after that if you go up you see that input voltage is less than that that is why you decrease here is a down count next step it is higher you increase. So, again its crossed next step you decrease next step your input voltages increase. So, it will be increasing here it crosses again it decreases again it increases two steps.

So, it is continuously trying to track. So, it is not coming to 0 and from 0 it is again trying to search right. So, this tracking type of A D converter works much faster as compared to a simple counter type counter type. For those of you who know programming, it is like a linear search you are searching for a certain value of V_n starting from 0 0 1 2 3 4 5 6. You are going up now in tracking type it says once you have found it for the next time you start from there either go up or go down. Tracking type works well for signals which are changing relatively slowly ok because, it changes very fast. So, it may not be able to track.

So, whatever we have said is here we use a binary up down counter if the comparator output is 1. We increment the counter if it is 0 we decrement the counter. As I have said is suitable for relatively slowly varying waveforms because the reason is that if V_{in} changes too fast the counter may not be able to track the changes because we are basically using a clock to either count up by 1 or count down by 1.

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- Here we use a binary up-down counter.
 - If the output of the comparator is 1 ($V_{in} > D$), the counter is incremented by 1.
 - If the output of the comparator is 0 ($V_{in} < D$), the counter is decremented by 1.
 - The counter output continuously tracks the input analog voltage.
- Suitable for continuous conversion of slowly-varying waveforms.
 - If V_{in} changes too fast, the counter may not be able to track the changes.
 - Here also, the worst-case conversion time is 2^n .

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If it changes in a jump by 100 steps again you will have to count up 100 steps slowly-slowly. It will not be so, efficient right, but in the worst case the conversion time is still 2^n to the power n right. So, we come to the end of this lecture. In the next lecture we shall be looking at well a similar kind of a technique, but a scheme which works much better in the worst case. Because here also we said in the worst case I may have to start from 0 and go up to maximum 2^n .

But in the next method that we shall be talking about in the next lecture, we will see that for an n bit conversion maximum n clock cycles will be required for 1 conversion. Suppose, I have a 16 bit converter I do not need 65000, 2^n to the power 16 cycles clock cycles. I need maximum only 16 clock cycles, it will be much faster and scalable for larger values of n you will be able to use it. This will be discussed in the next lecture.

Thank you.