Switching Circuits and Logic Design
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Lecture - 39
Synthesis of Synchronous Sequential Circuits (Part IV)

So, we continue with our discussion and you take another example of Synthesis of a Synchronous Sequential Circuit. In our, I mean if you recall in our last lecture, we talked about a serial adder and in this lecture we shall be talking about that sequence detector. Let us look into this lecture the part 4 of our discussion. So, sequence detector this is something which we have already seen earlier just to recall.

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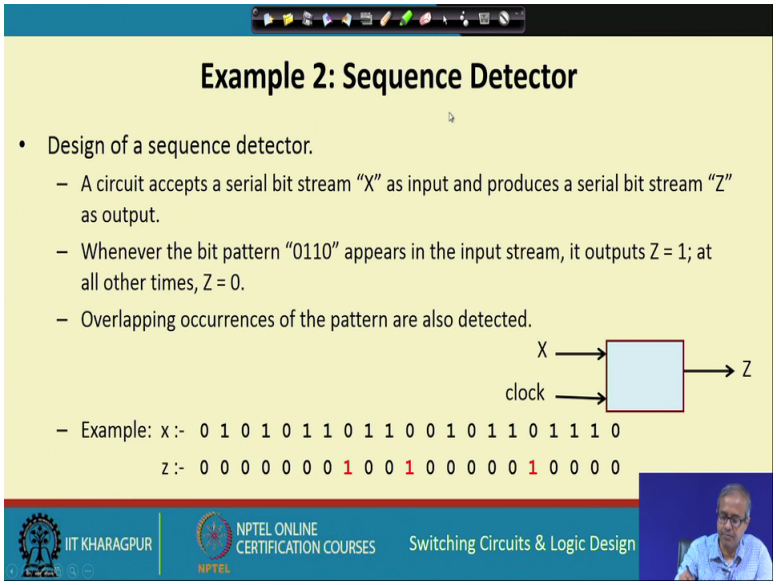

In this sequence detector we want to detect this bit pattern 0110; in this input stream X, X is a serial bit stream that is coming. And whenever this pattern appears the output Z also generates a serial output stream, the output bit will become 1 and at all other times output will be 0 and we will be allowing overlapping occurrences of 0110; as we have mentioned this were discussed earlier ok

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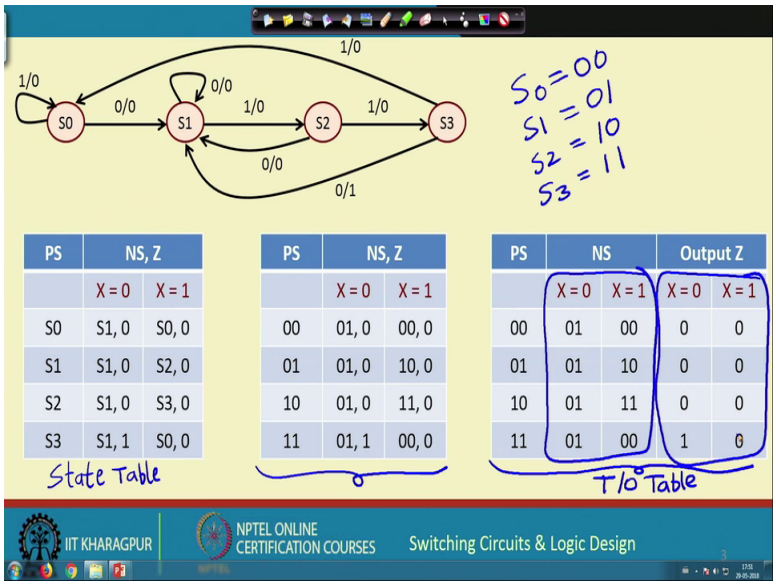

So, this was 1 example where this outputs once were generated ok. Now this was the state transition diagram that we have worked out earlier; now from that point let us try to proceed. Here we show the corresponding state table first step is to go into the state table. So, there are 4 states; so, I show the 4 states. So, 0 to S 4 because there is a single input, there be 2 input combinations 1 correspond to X equal to 0 X equal to 1.

So, whenever in state S 0 and input X is 0; so you go to S 1 with 0 if it is 1 you remain in S 0 with 0. Similarly for the other combinations you can check let say from S 3 if it is 0 you go back to S 1, S 1 with output 1; if it is 1 we go back to S 0 with output 0 well; so, this was the state table. Now let us do state assignment; this is the table which is after state assignment and the convention that you are followed is S 0 state is encoded as 0 0, S 1 as 0 1 S 2 as 1 0 and S 3 as 1 1.

So, you see this 2 tables are same, but wherever this S 0 is that is replaced by 0 0; wherever S 1 is that is replaced by 0 1 just that. And then we have constructed the transition and output table this is what we have mentioned; transition and output table where we had separated out this states and the outputs, instead of showing them in the same table separated by commas; we have put them into 2 separate tables one here and the other here. The first one is for the states second one is for the for the output.

The output you see it was 0 0 0 1 and all 0 0 0 0 1 and all 0. So, this is how we have proceeded up to the transition and output table it is fairly simple.

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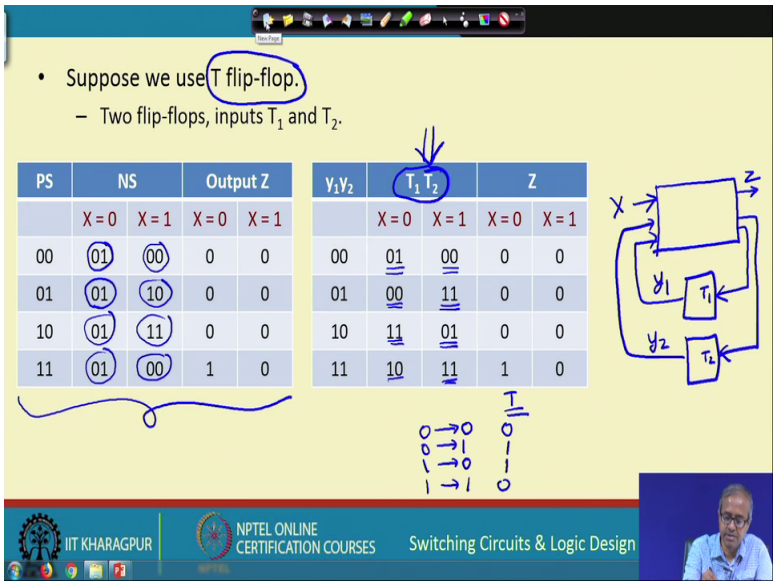

Now, from there this is the transition an output table I am showing again this is the transition and output table. Now suppose we are now selecting the memory element let us suppose we are using T flip flops right. Let us see what we are trying to do here; here we are saying is that because there are 4 states our sequential circuit module will look like this; there will be 2 memory elements right.

There will be X, there will be Z and these are y 1 and y small y 1 and small y 2. Now, what we are saying is that we shall be using T flip flops; so, this will be T 1 and T 2. So, instead of capital O and capital O; it will now, will be generating T 1 and T 2 directly from this circuit. So, how will be generating T 1 and T 2? Now again for a T flip flop let us think of the excitation requirement for a T flip flop whenever I want to go from 0 to 0. So, the T will be 0; 0 to 1, T will be 1 1 to 0 T will be 1; that means, whenever there is a change T will be 1 and 1 to 1 again T will be 0; this is how were T flip flop works.

Now, let us see here instead of the next state I am just listing T 1, T 2 values here. Let us see from 0 0; I want to go to 0 1; that means, first one is 0 to 0 first one is not changing second one is changing. So, T 1 T 2 is 0 1 second one is changing 0 0 to 0 0 no change. So, 0 0; no change 0 1 to 0 1 no change 0 0 no change 0 1 to 1 0 both are changing ok; both are changing. So, that is why T 1 T 2 both are 1 1 1 0 to 0 1 both are changing 1 1; 1 0 to 1 1 only the second one is changing. So, 0 1; 1 1 to 0 1 the first 1 is changing 1 0 1 1 to 0 0 both are changing 1 1.

So, this is how you are constructing the excitation table corresponding to T flip flop right this is what you have done here.

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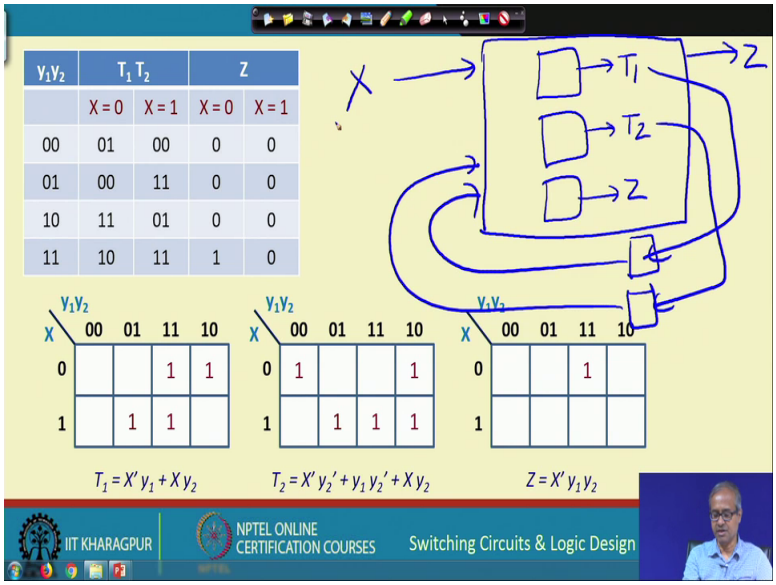

Now, once we have constructed this excitation table; I am showing it again here. From here you can directly generate the functions and construct the Karnaugh maps. Here I have one input X because this is one input I am showing it and this way and this y 1, y 2 I am showing on the in this direction. So, this T 1 T 2 first let us consider T 1; this is for T 1 for T 1 where there is 1? There is a 1 here, here and here. So, let us see this 1 is for X equal to 0; 1 0, X equal to 0; 1 0 this 1, X equal to 0 1 1 this 1 X equal to 1; 0 1 this 1 X equal to 1 1 1 this 1.

So, in this case there will be 2 cubes one will be like this, one will be like this. So, the expression for T 1 will look like this X 1 bar; y 1 and this one will be X S and y 2. Similarly for T 2 if you now go if you now look at T 2; so, you see where T 2 is changing; T 2 is 1 T 2 is 1 here, here, here, here, here; 5 places. So, X equal to 0 and 0 0; X equal to 0 and 0 0 here X equal to 0 and 1 0 here X equal to 1 and all these 3 X equal to 1 all these 3.

So, here the cubes will be one cube will be like this, one cube will be like this and the other cube can be either this or this. Let us see which one I have taken; this X 1 bar y 2 bar X 1 bar y 2 bar is this one; this cube y 1 y 2 bar y 1 y 2 bar I have taken this one y 1 y

2 bar and X y 2 bar is this; this is T 2 and finally, for Z there is a single 1 here it is a it is X 1 bar y 1 y 2.

So, once you have done this. So, now what will your circuit look like? Now if I look into the circuit as a big black box; inside your circuit all these functions will be there. There will be X bar, y 1 plus X y 2 this will be there will be one block that will generating this function T 1. Then this will be another functional block there be another block that will be generating T 2 and there will be another circuit that will be generating Z right.

So, your this circuit will be generating your output Z and there will be 2 flip flops; this T 1 will be connected to 1 of them and T 2 will be connecting to the other of them there will be fed back and X will be your input; this will how your circuit will look like. So, now you understand that how you can arrive at the final circuit; you have your state table, make a state assignment, select the flip flop type means after; you have the transition and output table you get the excitation table based on the flip flop type.

And from the excitation table you can directly construct the flip flops; you can you can directly construct the Karnaugh maps; if the number of variables is 3 or 4 of course, and you can state away minimize the functions. Once you minimize the functions you have got the circuit specification, you can directly arrive at the circuit right.

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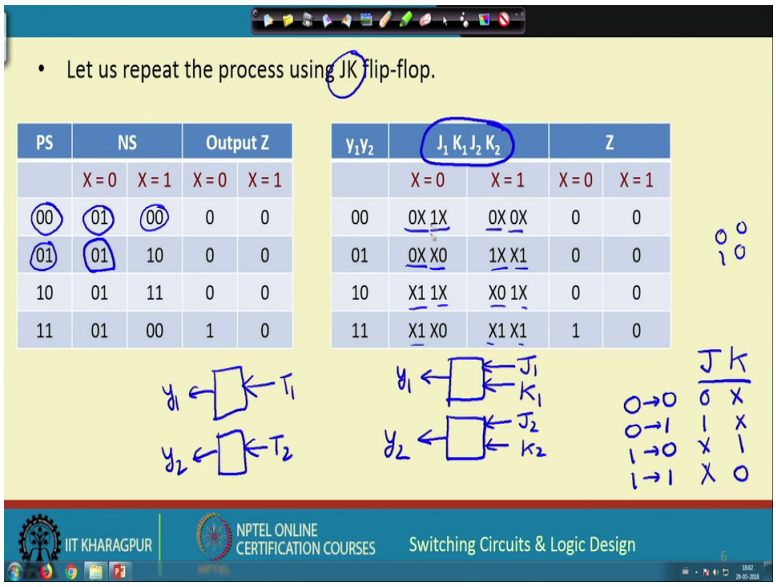

Now, here we have used a T flip flop right; now suppose now we are saying that well let us use J K flip flop not T. So, now how will it look like? Now see earlier in the previous case we had 2 flip flops ok; the inputs were T 1 and T 2 and the outputs were generated as small y 1 and small y 2. But now if you are using J K flip flop; now your requirement will be there will be 4 inputs that need to be generated J 1, K 1 and J 2, K 2. Because for every flip flop will be generating 2 inputs the first one will be generating small y 1 the second one will be generating small y 2.

Now, again for a J K flip flop you think of the excitation requirement J K flip flop how do you do? 0 to 0 0 to 1 1 to 0 and 1 to 1; from 0 to 0 you can apply either 0 0 or 0 1. So, 0 don't care; from 0 to 1 you can either apply 1 0 or 1 1; so 1 don't care. 1 to 0 you can apply either 0 1 or 1 1 which means don't care 1; 1 to 1 means either 1 0 or 1 1; that means, just a second 0 to 1 is 1 to no 1 to 1 is either 0 0 or either 0 0 or 1 0; that means, don't care 0 don't care 0 yeah fine.

So, now you see this J 1, K 1, J 2, K 2 that we will have to generate; this was our transition and transition and output table. Now let us see one by one present state was 0 0 you are going to 0 1. First one is 0 to 0; 0 to 0 means 0 don't care you see 0 don't care, then 0 1 0 1 is 1 don't care 1 don't care. Then 0 0 to 0 0 both are 0 to 0 0 don't care 0 don't care, 0 don't care. Then from 0 1 you are going to 0 1 0 to 0 1 to 1 0 to 0 is 0 don't care 1 to 1 is don't care 0 0 don't care like this you can have all right like this you can get all of them. Now, the point to note is that once we have obtained this table; now you can get the Karnaugh map for this all this 4 functions, you will now require 4 Karnaugh maps.

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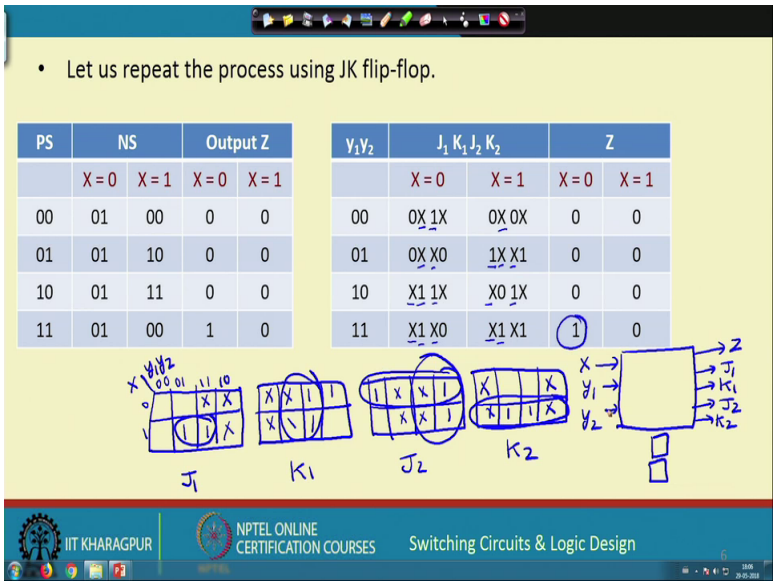

4 for J K J 1 K 2 and 1 for Z 5 in total; So, let say X in this direction and y 1 y 2 here; let say this is for J 1; J 1 let say there is don't care here; don't care means 0 1 0 0 0 0 1 1 1 1 0 0 1 0; this is don't care 0 1 1; 0 1 1 is also don't care and J 1 this is also J 1 this is 1. So, X 1 1 and 0 1 1 and 0 1; this is 1 and these are don't cares 1 1 0 1 1 0 is don't care and 1 1 1 is don't care.

So, here you can have best you can have a cube like this and minimize it right for J 1. Similarly for K 1 what will happen? K 1 let say K 1 will be the second one don't care don't care 1 1; X equal to 0. So, it will be don't care don't care 1 1 and don't care, don't care; first one don't care, this is 1; 1 1 1 is 1 1 1 is 1. So, here you can have a bigger cube like this; this is K 1. Similarly you can have J 2; J 2 will be the middle one; 1 don't care 1 don't care. So, 1 is for 0 0 0 and 0 1 0 0 0 0 and 0 1 0 other are don't cares and J 2 0 don't care 1 1 is here 1 0, these 2 are don't cares.

So, here you will have one cube like this and one cube like this; this J 2 and then you go for K 2. So, when your K 2 will last 1 don't care 0 0 0 and 1 0 0 0 0 and 1 these 2 don't care and here you have 1 in 0 1 and 1 1 0 1 and 1 1 others are don't care. So, you have a cube like this; first for Z there is no need of construction it is a single 1 no minimization.

So, you see you can directly get the functions from here; now what you do? You have your combinational circuit; you can design according to these functions. You will be having the input X, you will be having this inputs y 1 y 2 coming from the flip flops and

it will be generating Z; it will be generating J 1, K 1; J 2, K 2 and you will be having 2 flip flops here.

One getting J 1 K 1 generating y 1; other getting J 2 K 2 and generating y 2 ok; so, you see the examples that have worked out the show that; however, complex your circuit can be. While of course, in d and T the number of variables are inputs to the flip flops you need to controller less for J K and SR it becomes bigger, but still it is manageable you can work out you can minimize.

And there are functions which can be minimized better using J K or T flip flop there are other functions, which can be minimized better using D flip flop. So, there is no hard and first rule that which flip flop is better which will give you smaller circuit this all comes from experience right.

So, here we have worked out a number of examples; we shall look at some more examples later. So, let us come to the, this already we have done let us come to the end of this lecture. So, what will see later is that we shall work out a couple of counter design examples because counter designs are interesting. So, in our next lecture we shall be looking at some designs of counters, we shall we going through the entire process of counter design. And after that we shall be looking into the design of resistors and counters from slightly different perspective. So, those discussions we shall be going through in our later lectures.

Thank you.