Switching Circuits and Logic Design
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Lecture - 35
Clocking and Timing (Part II)

So, we continue with our discussion on Clocking and Timing issues in flip flops and synchronous sequential circuits. So, the title of this talk is: Clocking and Timing the second part. Now in this part, we shall be talking about several other features of timing that are important. For example, we shall be talking about the maximum clock frequency that we can use in a circuit such that correct operation can be guaranteed then you shall be looking at something call hazards and clock skew already you have mentioned and finally, we shall be looking at an example synchronous sequential circuit and see how it works ok.

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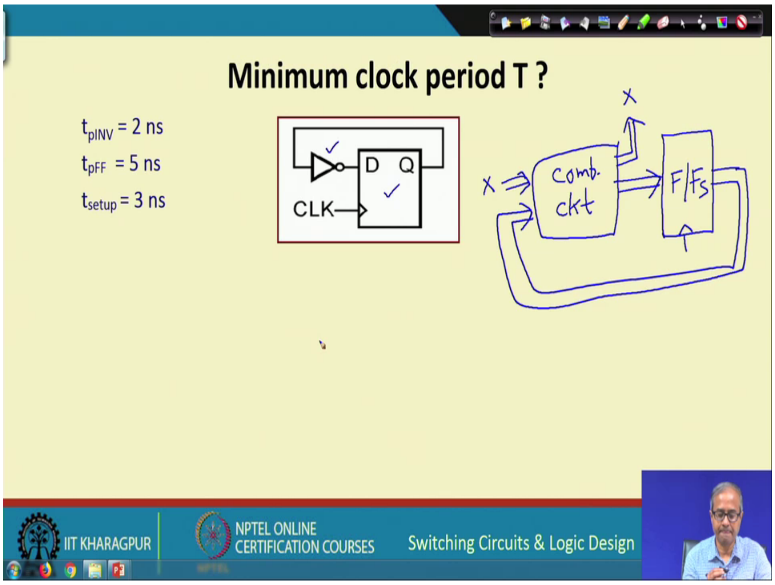

Minimum clock period T ?

$t_{pINV} = 2$ ns

$t_{pFF} = 5$ ns

$t_{setup} = 3$ ns

D
Q
CLK
X
X
Comb. ckt
F/Fs
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So, we consider this example means a very simple example you see means any synchronous sequential circuit generally if you look into the block diagram level, it will consist of 2 blocks; one is a block which contain one or more flip flops and there will be another block, which will be a combinational circuit just gates combinational circuit. So, the output of the combinational circuit will be feeding the flip flops, and the flip flop outputs can come to the input of the combinational circuit. Now, in addition you can have some more inputs coming here and some outputs can be generated from here. Now, in the example any of course, clock will be there clock will be applied to flip flops, now in this example we do not have these inputs coming to the combination circuit and this outputs generated from the combination circuit.

So, for flip flops we have a single d flip flop here, and for the combinational circuit we have a single inverter or NOT gate here ok. So, let us look into this example and try to do an analysis. Now the assumptions regarding the delays that you make are as follows, we will assume that the delay of an inverter this NOT gate tp inverter inv is 2 nanoseconds.

The delay of this flip flop so, once the clock comes after how much time the output will come it is 5 nanoseconds tpFF, and setup time of this flip flop is 3 nano seconds. Now, as I said earlier if you recall in our last lecture, the hold time and the propagation delay overlaps actually hold time need not be considered when you are talking about the maximum clock frequency minimum clock frequency minimum time period yeah fine.

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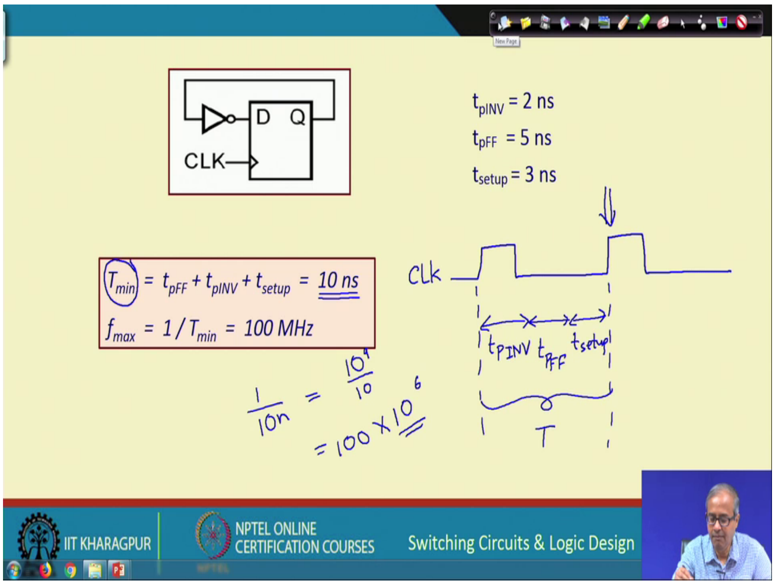
D
Q
CLK
Clk
t_{PINV}
t_{PFF}
t_{setup}
T
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$t_{pINV} = 2$ ns

$t_{pFF} = 5$ ns

$t_{setup} = 3$ ns

$$T_{min} = t_{pFF} + t_{pINV} + t_{setup} = 10 \text{ ns}$$

$$f_{max} = 1/T_{min} = 100 \text{ MHz}$$

$$\frac{1}{10n} = \frac{10^9}{10} = 100 \times 10^6$$

So, let us see for this example as I said, now we are trying to determine the minimum clock frequency for which the circuit will work correctly let us look into the clock; the clock signals is coming I am just showing 2 pulses positive edge triggered so, this is the active edge. So, if you look at the second edge let us concentrate here.

So, with respect to the first edge; so, when the first edge comes so, after how much time this d will be generated? There will be a delay out here which will be equal to the delay of the inverter, the inverter delay D will be generated. And after this delay is generated you will have to hold this before the clock pulse also before this clock pulse you must have a mandatory setup time, this delay you have to give and also you should not forget the delay of the flip flop. So, after tp inverter your generating this, after this delay this will get into this.

So, there will also be a propagation delay of the flip flop. So, these 3 delays are getting the getting added up here and there must be greater than the clock time period let us take 2 cases. So, min what I am saying is that T min in this example will be some of these 3 times, which is coming to 10 nanoseconds 2 plus 5 plus 3. Now, because frequency is the reciprocal of the time period, the maximum frequency will be 1 by minimum time period. So, 1 by 10 nanoseconds 1 by 10 nanosecond means 10 is 10 to the power minus 9. So, it is 10 to the power 9 by 10 this is 100 mega 10 to the power 6 mega hertz right.

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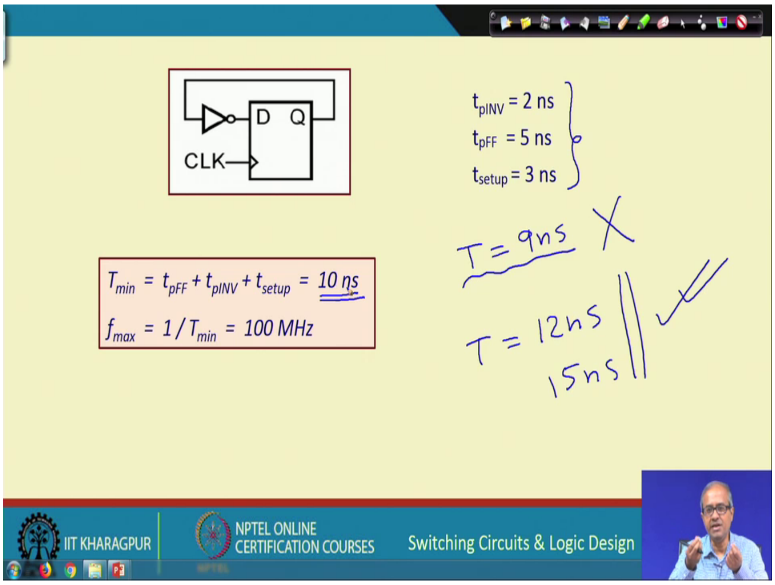

$t_{pINV} = 2$ ns
$t_{pFF} = 5$ ns
$t_{setup} = 3$ ns

$T_{min} = t_{pFF} + t_{pINV} + t_{setup} = \underline{10\ ns}$

$f_{max} = 1/T_{min} = 100$ MHz

$T = 9ns$ ✗

$T = 12ns$
$15ns$ ✓

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Now, let us say suppose we choose a clock with time period 9 nanoseconds. So, what we have to do when you are designing a circuit we will have to make this calculation, and see that whether 9 nanosecond is enough or not. In this case because we see that we need minimum of 10 nanosecond so, this will lead to a timing violation we cannot have a clock with time period 9 nanosecond. But let us say we are using a clock with 12 nanoseconds or 15 nanoseconds this is certainly greater than this minimum of 10 so, this is perfectly permissible. So, what we do whatever minimum we calculate, in addition we also put some more you can say a buffer.

So, I mean if it is coming to 9 we say that well let us keep it minimum 10 and that way we can choose the clock frequency maximum clock frequency with which we can operate our circuit right.

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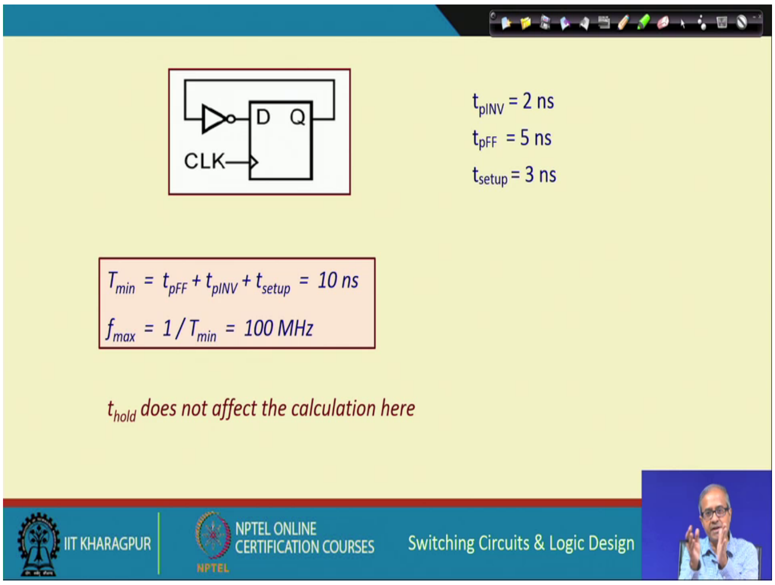

$t_{pINV} = 2$ ns

$t_{pFF} = 5$ ns

$t_{setup} = 3$ ns

$T_{min} = t_{pFF} + t_{pINV} + t_{setup} = 10\ ns$

$f_{max} = 1 / T_{min} = 100\ MHz$

t_{hold} *does not affect the calculation here*

D
Q
CLK
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And one thing to notice that as we have said that for a hold time delay, does not affect the calculation here because when the clock edge comes hold time means after that minimum how much I have to hold the inputs, but already that propagation delay is calculated from the clock edge. So, propagation delay time includes the hold time. So, we need not have to add the whole time again ok. So, this does not affect the calculation.

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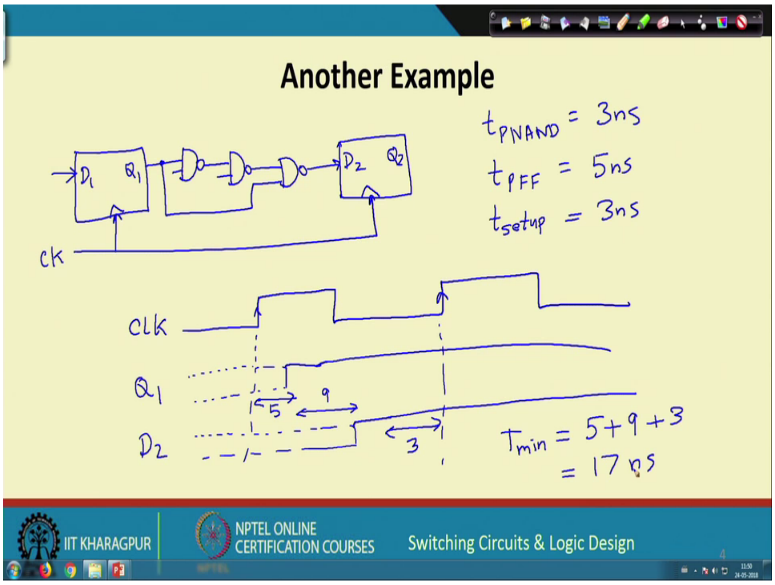

Another Example

$t_{pNAND} = 3ns$

$t_{pFF} = 5ns$

$t_{setup} = 3ns$

$T_{min} = 5+9+3$

$= 17\ ns$

D_1
Q_1
D_2
Q_2
ck
clk
Q_1
D_2
5
9
3
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Well let us take another example, which let us ha draw like this suppose we have a d flip flop let us call it D 1 and Q 1 this input is coming here, and let us say in Q 1 this has been fed to a let us say a chain of gates. So, here I am showing here 3 gates let us say. So, some external inputs are coming here, some external inputs are coming let say this Q 1 itself can come here again and this is being fed to another D flip flop let us call it D 2 and Q 2 and there is a clock signal, which is being fed to both these flip flops.

Consider a scenario like this and assume that the propagation delay of a NAND gate tp NAND is 3 nanoseconds, propagation delay of a flip flop is 5 nanoseconds and setup time is also 3 nanoseconds. So, for this circuit if you just look into the timing once more so, I am showing 2 clocks let us say like this these are the active edges.

So, if I look at Q 1 Q 1 when the clock edge comes the propagation delay is 5 nanosecond. So, Q 1 whatever it was earlier I do not know whatever it was earlier, after a delay here of 5 nanoseconds, I will get the value of Q 1 here after this clock edge comes t PFF right and this value will remain after that, it’s a does not change after let us say. Now, let us talk about D 2 what will happen with D 2? D 2 will also face the delay of these 3 NAND gates which will be equal 3 into 3 9.

So, there will be another delay of 9 nanosecond after this. So, D 2 whatever the value it was I do not know after that whatever is new value of D 2, new value of D 2 will be generated here and in addition before the next clock edge comes. So, you must have the set up time of 3 nanosecond maintained here; so, 5 9 and 3 at the minimum time that you must have between 2 successive clock edges. So, in this case your minimum time period will be 5 plus 9 plus 3, which is 17 nanoseconds.

So, in this way given any circuit so, if you have an estimate of the delays of the different components the gates flip flops, then you can have a calculation which can tell you what is the maximum frequency with which your circuit should work. So, you should not blindly select clock frequency and see whether the circuit is working or not, because every circuit component will have some delay and the clock must be slow enough so, that all gates are getting sufficient time for evaluation ok. So, these 2 examples actually try to show this.

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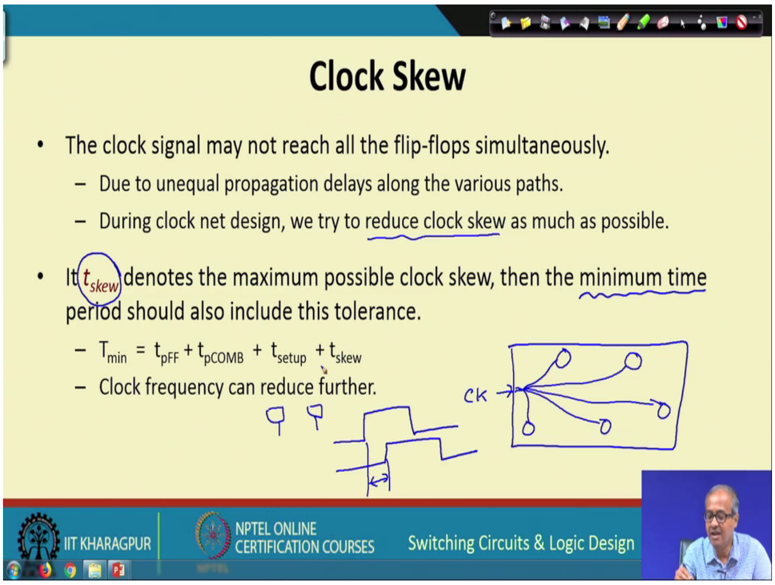

Clock Skew

- The clock signal may not reach all the flip-flops simultaneously.
  - Due to unequal propagation delays along the various paths.
  - During clock net design, we try to reduce clock skew as much as possible.
- If t_{skew} denotes the maximum possible clock skew, then the minimum time period should also include this tolerance.
  - $T_{min} = t_{pFF} + t_{pCOMB} + t_{setup} + t_{skew}$
  - Clock frequency can reduce further.

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Now, talking about clock skew already I just mentioned this earlier in the last lecture, the main concern is that the clock signal let say suppose we have a chip here I said, the clock signal may be fed to the input of the chip and there can be several flip flops spread all around the chip. So, this clock signal has to be connected here, has to be connected here has to be connected here and so on.

So, the length of the wires will be unequal and because of resistive and capacitive effects of these wires, there will be a delays rc time constant delays and the delays will be unequal in general and this due to un equal propagation delays along the various paths, there will be clock skew which means clock signal may not reach all the flip flops simultaneously.

While of course, when we are designing this clock network we try to reduce clocks skew as much as possible ideally 0 but, but in practice we cannot exactly make it 0 we will try to reduce it as much as possible. There are methods of doing that, but that is slightly beyond this scope of this course we shall not be discussing how to reduce skew here just what is skew that is enough. Now, the point to notice that, let us assume t skew is the maximum possible clock skew meaning for 2 flip flops, if let us say the clocks are coming the first clock is coming like this, the second clock is delayed like this. So, what is the maximum difference that is defined as t skew ok.

So, if you consider also clock skew then the minimum time period for the clock, the calculation would be a little different. Like as we have seen earlier for the for the T min calculation we have to calculate the delay of the flip flop, we calculated the delay of the combinational part; that means, the 3 NAND gates were there in the previous example and of course, this setup time. Now, in this case in addition we also have to add clock skew.

Because you do not know how much clock skew is, but we know what the maximum clock skew can be; which means for the 7 flip flop the clock edge might get delayed or might get advanced by that amount. So, that also you must make provision when you are estimating the minimum time period of the clock right. Because of this the clock frequency can reduce with respect to the case where you are ignoring clock skew right this is the idea.

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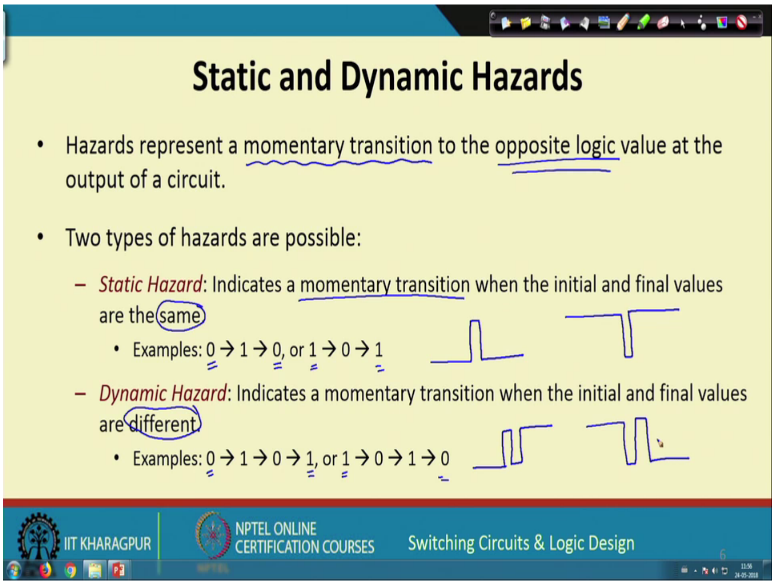

Static and Dynamic Hazards

- Hazards represent a momentary transition to the opposite logic value at the output of a circuit.
- Two types of hazards are possible:
  - *Static Hazard*: Indicates a momentary transition when the initial and final values are the same
    - Examples: 0 → 1 → 0, or 1 → 0 → 1
  - *Dynamic Hazard*: Indicates a momentary transition when the initial and final values are different
    - Examples: 0 → 1 → 0 → 1, or 1 → 0 → 1 → 0

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Now, now we considered I means, another property of circuits, related to delays these are called hazards. The idea is given a circuit I am applying some input, I am expecting some outputs. Let us say the output was 0 now the output is supposed to be 1. It may so happened that instead of the output going from 0 to 1 in a clean transition, we may say that it may vary several times before settling to 1; that means, there can be unnecessary transitions for very short durations these are called glitches, and this glitches actually are called hazards in circuit design.

So, definition of hazard very loosely can be mentioned is that, they represent momentary transition in the value of a signal line to the opposite logic value. Like I am showing some examples, 2 types of hazards are possible static and dynamic. Static hazard is one it says there is a momentary transition, when the initial and final values are the same; like the initial value was 0 final value is 0, but what I see in the output that it makes a momentary transition to 1 before settling to 0; that means, 0 1 and back to 0. Or the other way round suppose the output value supposed to be 1, it makes a very temporary transition to 0 before settling to 1. Dynamic hazard is similar, but here the initial and final values are different.

So, let us say initial value is 0 final value is 1. So, it may so happen that instead of a clean transition it makes a transitions like this and then settles down; that means, 0 to 1 back to 0 again 1 or the reverse from 1 to 0 back to 1 like this. 1 to 0, 0 to 1 1 to 0. Now if this circuit outputs are directly connected to some other circuit and this glitches may affect the operation of those circuits, then there can be a problem. So, you should be aware of such glitches or hazards and design circuits in such a way that it should only be activated in the edges of the clock and these hazards should be stabilized before the clock edge comes ok. So, the idea is like this.

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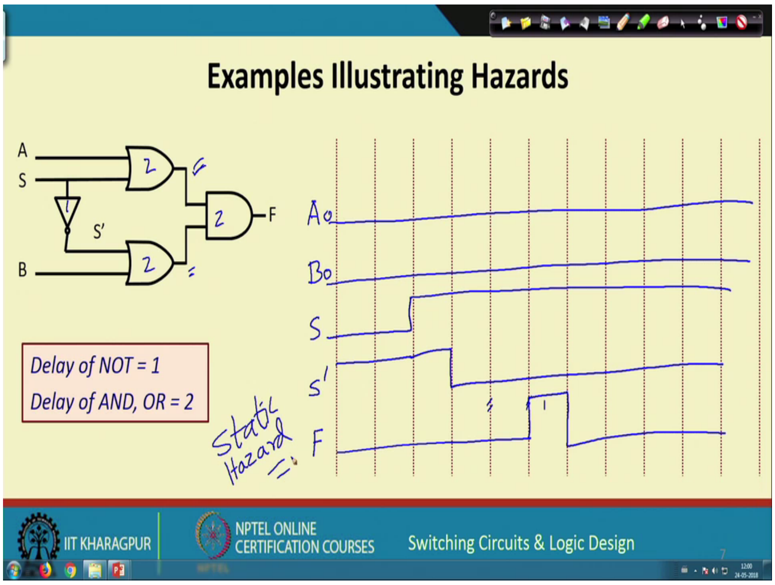

Examples Illustrating Hazards

Delay of NOT = 1
Delay of AND, OR = 2

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So, let us take some examples to illustrate the occurrence of such hazards. So, here we consider one example like this, this is a circuit comprising of four gates let us assume delay of the NOT gate is 1 and delay of the other gates is 2 2 and 2 let us show a typical scenario. Suppose this input signal A is applied constant 0. So, I have applied a constant 0 here, B is also constant 0 B is also constant 0 0. Now S what we do? S let us say it was 0 here we make it 1 and then we leave it as 1. So, what will happen to S prime? S prime is the not of S and the delay of this NOT gate is 1.

So, it will be not, but it will not become 0 immediately after a delay of 1 so, this grids I have shown these are one unit. So, after one unit S bar will become 0, and then it will remain 0. So, now, if you calculate F what will be the value of F? So, in one case you are taking or of A and S or of A and S the delay is 2. So, here one 2 delay 2 means here this point will become one at this point. And if you look at this gate or of S bar and B; S bar and B you see S bar is 1 here right or B so, it will get again delayed here.

So, if you just plot this will become like this, this I suggest you also show the waveforms of these 2 lines and then do an, and it will be clear to you. So, here what you are saying that the F was 0, and it is supposed to be 0 again in the stable state, but because of the delays of the gates it is temporarily moving to 1 and remaining one for one time unit before coming back to 0, this is an example of static hazard right let us take another example.

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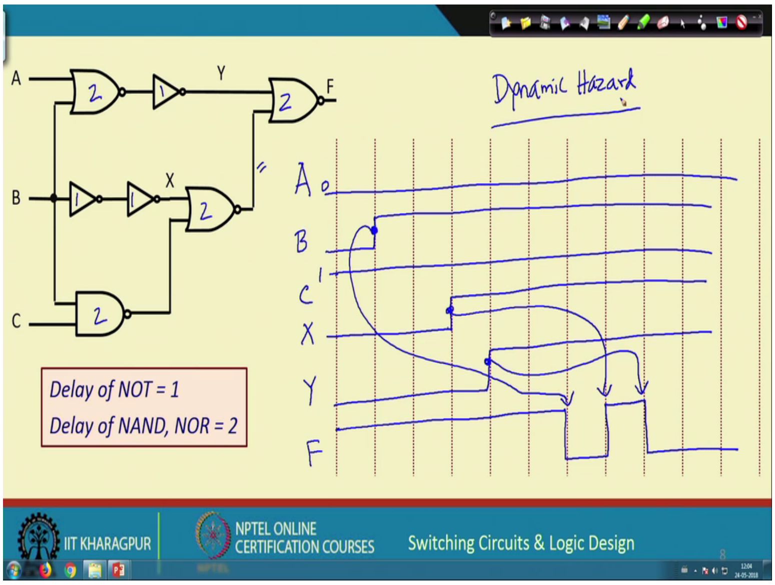

Delay of NOT = 1
Delay of NAND, NOR = 2

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This is the slightly more complex circuit, here we assume the delay of the NOT gate there are 3 NOT gate this is 1. So, this is 1, this is also 1 this is also 1 and NAND and nor gate there are four of them it is 2 this is 2 2 2 and 2. So, here again let us take a scenario, where the input A is permanently at 0, I am applying 0 at A. B input let say it was 0 we make it 1 here and leave at 1.

C input let us say it is one continuously it is 1 these are the 3 inputs ABC we are applying. Now let us see what will be the value of X. You see the value of B is getting inverted twice 2 NOT gates. So, the same values should come at x, but after a delay of 2 units one plus 1. So, whatever B is there, there will be a delay of 2 so, X will be like this right B after delay of 2 and what will be Y on the other side? See here this A is 1 A is 0 B is also becoming 1. So, this 1 this is 0. So, output of this y would be one. So, initially y was 0 because A 0 B 0 both were 0 it was 1 0.

So, it was 0 Y is supposed to become 1, but the delay will be from the inputs 2 plus 1 3. So, when B is changing after that 1 2 3. So, Y will also change, but it will change here after a delay of 3. Now if you just look at F I am again jumping some steps, you can also plot the value here it will it may be easier, but what will see that in F in this part of the circuit after this X as come, there is delay of 2 before this is changing and again a delay of 2 before this is changing so, 1 2 3 4.

So, you will get A value like this, B is changing yeah like this. So, the first edge will be because of this transition in B, you show it like this in an arrow, the second edge will be due to transition of X here this edge, and the third edge will be due to the in a transition at Y here is this. So, you see all this edges are because of the delays in these gates and some signal value changing somewhere, this is an example of dynamic hazard which you have demonstrated. So, you are not going into the theory behind static and dynamic hazard, just I have shown you one example and with the help of the example we have seen how this hazard shows up ok.

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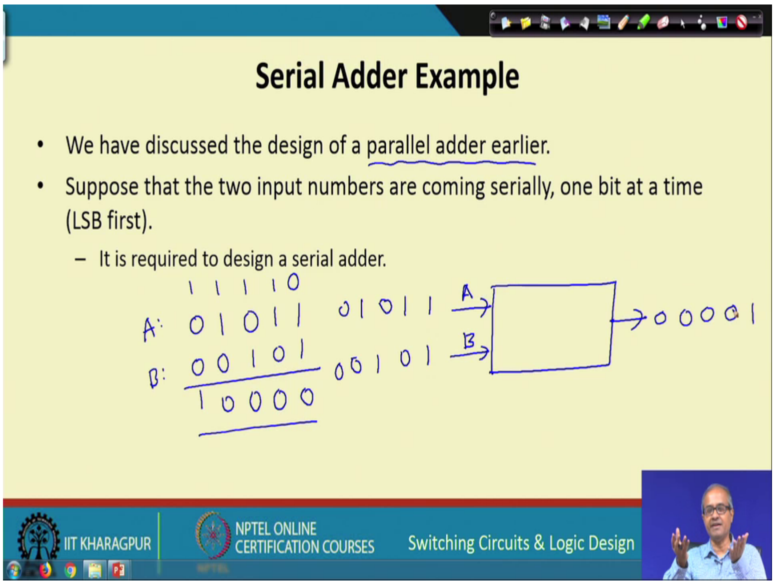

Serial Adder Example

- We have discussed the design of a parallel adder earlier.
- Suppose that the two input numbers are coming serially, one bit at a time (LSB first).
  - It is required to design a serial adder.

Lastly we shall be showing you one example of synchronous sequential circuit; this is an example of a serial adder. Now, before going into a serial adder well earlier you have already seen how a parallel adder works like let us say whenever you add 2 binary numbers let us take another number 0 0 1 0 1, you add this bits accumulate the carry add this carry carry carry, 1. This will be the sum and initially for the first stage you typically assume that the carry is 0.

So, in the parallel adder design we had a full adder in all the stages. Now what is saying is that, we are saying we have a serial adder; that means, I want to design a circuit like this where these 2 numbers let us call it A and B, they are fed serially. Serially means least significant bit first, first I feed 1 and 1 then I feed 1 and 0 then I feed 0 and 1, then I feed 1 and 0, then I feed 0 and 0 and in the output here I am expected to generate these bits in that same order, first I will get 0 then I will get 0 then 0 then 0 and finally, 1.

So, there is a single input A single input B where I am sending 1 bit at a time, and in the output I am generating 1 bit at a time. So, if you think that how this circuit should works, suppose you are a serial adder you imagine yourself to be a serial adder where the bits are coming one by one. So, if I tell that well the next pair of bits are 1 and 0 what should be the output? Well your question will be well I cannot say what will be the output unless I know: what is my carry, because I also up to add the carry right to ab to get the next sum. So, you will have to memorize the carry, there has to be a flip flop inside your circuit which will be memorizing the last carry right.

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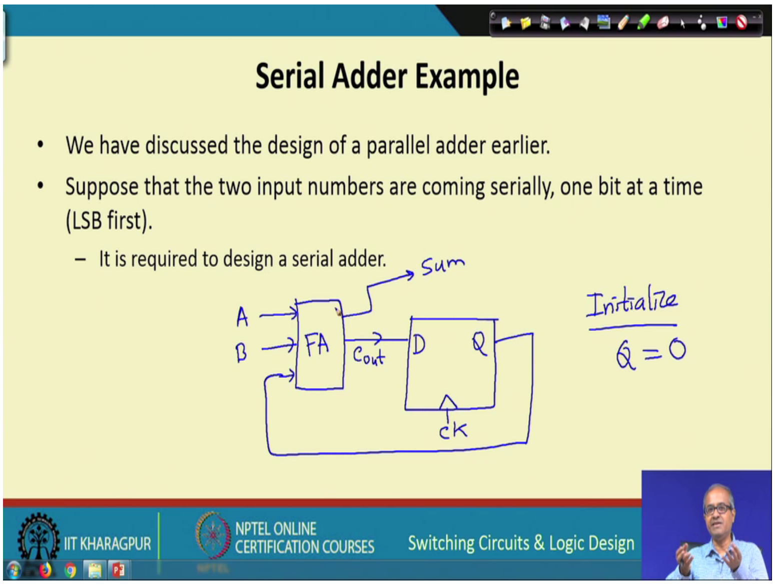

Serial Adder Example

- We have discussed the design of a parallel adder earlier.
- Suppose that the two input numbers are coming serially, one bit at a time (LSB first).
  - It is required to design a serial adder.

Sum
A
B
FA
Cout
D
Q
ck
Initialize
Q = 0
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So, to implement this circuit well we shall be going into the formal we have designing's are circuits later but what we are saying is that we shall having a D flip flop, and what will you do? We will be having a full adder, where the 2 serial bits A and B will be fed here, and the carry input will be the output of this memorized carry will come here and the output of the full adder the carry out will be stored in the flip flop and the sum will be generated as the serial output and this will be working in synchronism with a clock. And the only point to notice that this flip flop must be having an asynchronous clear input, because we have to initialize Q to 0 before you start the addition. So, every time you add 2 bits the previous carry will be coming, those 3 bits are added you generate sum you generate a carry the new carry gets stored and the process continuous.

So, you see the advantage of a serial adder is that you need so, little hardware, you need only one full adder and one flip flop, but the drawback is that if you are adding to 16 bit numbers, you will be requiring 16 clock pulses. So, it is very slow serial. So, we have just shown one example, later on we shall be looking into more formal ways of designing or synthesizing a circuit given a specification, this we shall be starting from our next lecture onwards. So, with this we come to the end of these lecture so, over the last 5 lectures, we discussed various latches and flip flop types and clocking and timing issues.

Thank you.