VLSI Physical Design
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Lecture - 64
Summarization of the Course

So, we have at last come to the end of this 12th week long course on VLSI physical design. So, over the last 12 weeks we have seen lot of issues, lot of aspects on VLSI physical design and some of the challenges that are faced there in.

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So, here in this last lecture I will try to summarize whatever we have seen over the last 12th weeks. So, we summarize the total coverage of the course that you have seen so far.

So, if you recall during the first week we have looked at some of the basic concepts of design automation, and how we can represent a design, then we looked at the various design styles like standard cell, semicustom, full custom and so on because we repeatedly mentioned there are many steps in VLSI physical design, which are highly dependent on the design style that is actually been used. So, if you use standard cell design style for example, which is most predominant, some of the tasks become much simpler because your topology or the configuration or the structure of your circuits become much regular and we also looked at the various steps that are required to be followed in physical automation.

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Now, during this second week we looked at some of the means initial steps that are required for the VLSI physical design, like circuit partitioning was the first step we talked about. So, when a large design is divided into smaller pieces, then creating tentative floorplans for this partitions or blocks, then how to place this blocks; that means, after the exact shapes and sizes and also the location of pin (Refer Time: 02:39). So, how to place them? So, we looked at various algorithms in this regards, and we also considered this specific design style related radiations that can affect our decision as to which algorithm should be used.

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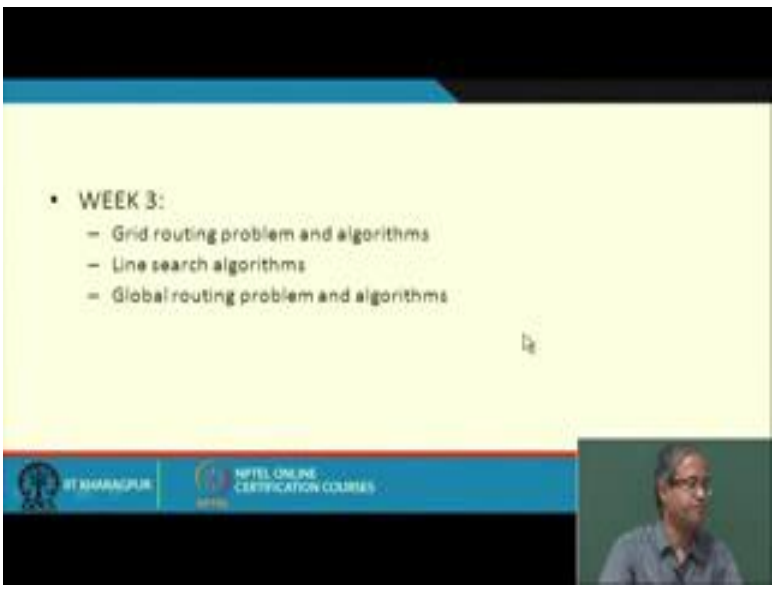

So, during third week we talked about the routing algorithms, specifically we talked about the grid routing problems. So, we talked about the algorithms like lease algorithms, headlocks algorithms, the various line search algorithms, and also talked about the global routing problem, so how we can represent it the different kind of data structures, and also some of the algorithms that are used.

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During the fourth week we looked at the detailed routing problem and the various solutions in particular the channel routing algorithms we have discussed and then we started our discussion on the very important issue of clock design, and the various timing issues that come there in.

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So, we continued our discussion in week 5, where we talked about how to design the clock networks, various clock routing architectures like H tree X tree method of means and medians etcetera and we looked at the various methods of clock tree design and the kind of hybrid approaches that are followed to minimize the clocks skew, because we said this is very important when you design a clock network, the main objective is to minimize the clocks skew as much as possible up to the terminal points. And of course, you also looked at how to route the power supply connections power and ground.

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Then we moved on to the timing related issues; in week 6 we started with some introduction to the timing closure problem, then we looked at the very important issue of timing analysis related problems of slack analysis, and how to identify the critical paths. We recall the paths which have negative slacks they are considered as critical paths in a design, false paths to remove unnecessary computations were possible and lastly we looked at timing driven placement techniques, which are some refinement of placement techniques we talked about earlier, where timing issues are also incorporated within the algorithms.

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Then we talked about the timing driven routing techniques, and this was followed by various physical synthesis techniques, where we can make some modifications to our netlists so as to meet some of the timing requirements or timing corrections that are required. So, we talked about gate sizing, introducing buffers, restructuring netlists and finally we looked at so called performance driven design flow. So, how this performance related issues are timing related issues can be incorporated during the various stages of the design, and then we looked at various approaches to timing optimizations.

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So, in week 8 we looked at means interconnect and layout related issues like how do we model interconnects, so, how do we estimate the delays of this interconnection lines, so (Refer Time: 06:46), delay model, lumped RC models various models we discussed there. So, we also talked about the design rule check and some design rules lambda based design rules, advance this rules are framed. So, how (Refer Time: 07:03) a tool can automatically check whether this design rules are followed or they are violated.

We talked about layout compaction techniques, which are again based on this design rules typically. So, these are some finer adjustments we do after the layout is completed before we do the so called tapeout we try to compact the layout, we try to do some visual inspection try to see whether the design rules are satisfied, if there are some design rule violations we try to correct them these are the kind of methods or tools that we use to make one final look and the at the design and adjust the design if required wherever some violations are detected.

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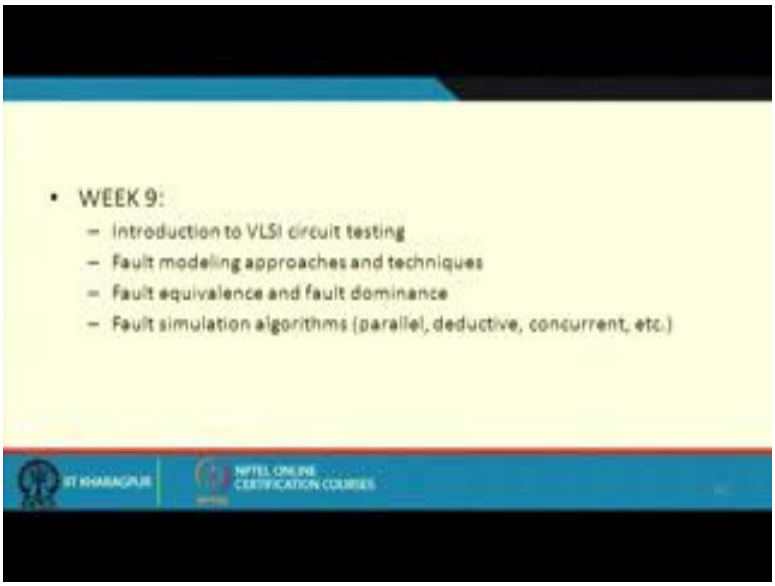

Now, during the next weeks we looked at another very important aspect of VLSI design, not only physical design; this is the aspect of testing. So, during week 9, we introduced the VLSI testing problem particularly the digital circuit design and testing; testing of digital circuits, we look we mentioned that how fault modeling is very important in this process. We mentioned how to reduce the number of faults using concepts like equivalence and dominance, then we looked at some of the faults simulation algorithms, which are a very useful tool for the test engineers we looked at some algorithms like parallel deductive and concurrent.

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During week 10, we continued to with our discussion on testing and looked at some basic concepts of test pattern generation then we looked at design for testability techniques specifically the scan path method. We looked at one of the standards the boundary scan standards and finally, built in self test technique, where we can design a circuit such that it can test itself.

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So, during week 11, we looked at some of the aspects of low power VLSI design which is also very important in present day VLSI design. So, we looked at the basic concepts various sources of power, dynamic power, static power, leakage power we looked at some general techniques for power reduction, we looked at some gate level techniques also at the level of gates how can we can make some changes so that power reduction is possible.

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And in this last week we looked at some architecture level techniques and also some algorithmic level techniques; where even at the higher level you have seen if we can follow some techniques, it is possible to provide some significant saving in power dissipation when we finally, synthesis our design into the layout level up to the layout level alright.

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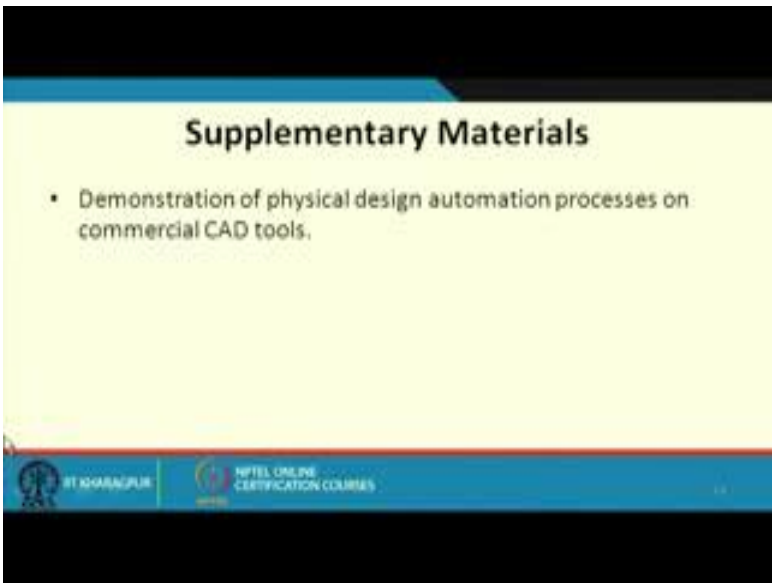

Now in addition there will be some supplementary materials that has been provided; this supplementary materials actually provide some demonstration of the physical design

automation process on some commercial CAD tools. So, here we have specifically looked at some of the commercial CAD tools like Cadians, we looked at some design flow in specific emphasis on physical design process the backend design, and also special emphasis on static timing analysis and related issues.

So, this exposure of the commercial CAD tools was not exactly meant to teach you how to use this CAD tools, but rather to give you an idea or a flavor of how this tools look like, but of course, if you want to learned or master this tools, you can use this introductive demonstration lectures to get started on it, you can go to a place where this kind of tools are available and have access to it and see how the designs and these tools are actually been used. So, once we use these tools hands on only then you can have a real feel of the capability of the tool because most of these tools are pretty compliance even huge, it is not possible to cover all aspects of this.

So, these were the supplementary materials and here I mentioned some main references refer VLSI design automation, we used references 1 and 2 and also the reference 4, and for testing mainly we use reference 3.

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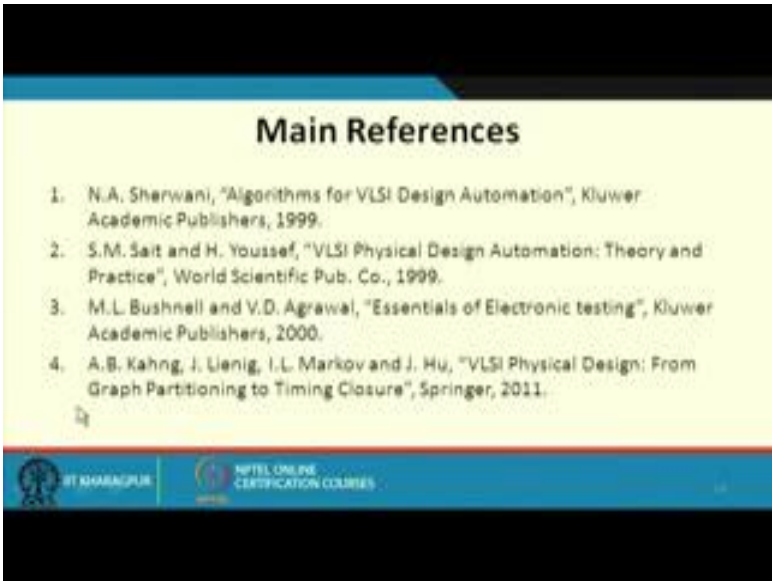

But of course, you can understand nowadays there are so many other references available on the internet, you can have a look at the internet, you can see lot more materials available there. So, I would; I should not or I would not want to limit you by specifying only a limited set of reference and saying that you do not look beyond this, I said that

these are only for reference, there is much more comprehensive and up to date materials and they are available on the internet on the web. Please visit the web, search through the topics you want to understand and learn, and you will get much more deep insight into the topics wants to go through them.

The objective of this course was not to make you experts in this topics, just to make you aware of some of the challenges that exists; this is just the tip of the iceberg, if you are really interested you need to study lot more go into the deep of this topics, possibly learn to use the CAD tools because it is there where you are actually using these design automation in practice and I believe in this way you can be a good engineer or an expert so as to say in these areas.

So, with this we come to the end of this course, and I thank all of you for enrolling in this course, for attending this course, and I sincerely hope that this course has been of some help to you either academically or professionally or otherwise. And we really appreciate if you can provide some of your feedback regarding this course on the discussion forum that is available, that will be helpful for us really so that we can possibly enhance on update some sections of this course on or make some enhancements in future versions if you decide to run this course again in the future.

Thank you very much once again.