VLSI Physical Design
Prof. Indranil Sengupta
Department of Computer Science and Engineering
Indian Institute of Technology, Kharagpur

Lecture – 55
Boundary Scan Standard

So, in the last lecture, we talked about the design for distribute technique. So, one method we looked at namely this scan path. Now in the correct lecture we shall be looking at some of this standardization effort in this regard. See scan path is a concept, but various manufactures can implement can path in different ways. Now imagine a scenario, that I am system integrator or an assembler. I have manufactured mother board; on which I have put let say 10 different ICs which may be manufactured by different companies. Now once I put the chips in the ICs, normal trouble starts, how do I test my board? This each of this chips are a VLSI chip those are complex containing millions and billions of transistors.

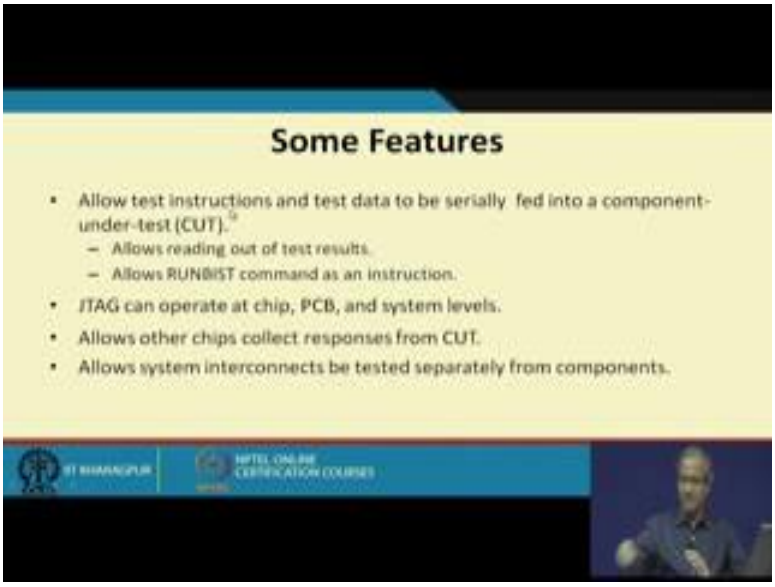
So, how do I test the chip once they are soldered on the printer circuit board? There has to be solution there. And again unless the companies agree among themselves on some standards, it is very difficult to almost impossible to come up with a feasible way to go this. Now fortunately such a standard exists called the boundary scan standard which we shall be looking at briefly in this lecture.

(Refer Slide Time: 01:46)

So, this is actually one of the standards like I was talking about. So, you know how manufacture chip can be tested. We looked at several methods test generation dft and so on. As I said different manufactures may use different methods for testing. So, there is no standardization or there was no standardization. So, when several chips are assembled on a board. So, how do I test the individual chips, why they are designing on the board.

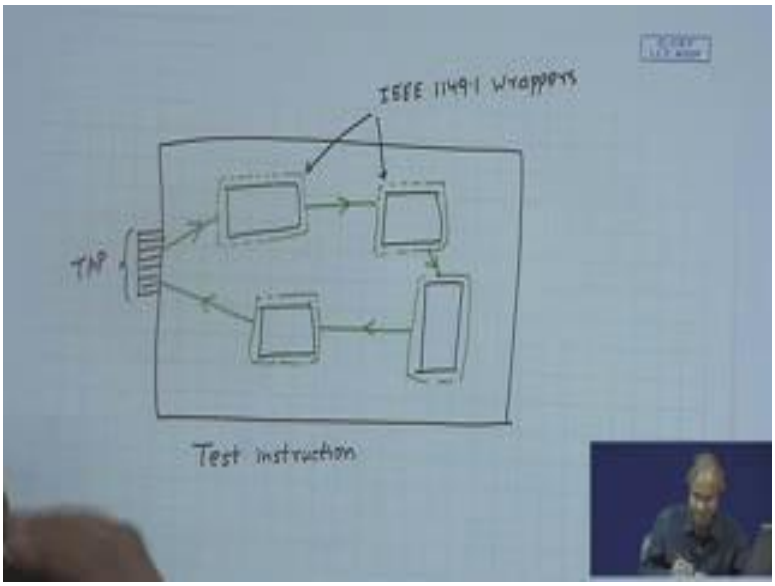
So, what was done is that, there was a there is an action group called joint test action group JTAG. This is the short form of it was formed which was comprised of several of the leading semi conduct a manufactures and academicians and finally, standard called i triple e 1149.1 which is sometimes also called boundary scan standard which emerged now it became. So, popular that now a day most of the people called them as the JTAG standard, JTAG port, JTAG standard. That is known which is be used by many designers and the users today it has become so popular.

(Refer Slide Time: 03:13)



So, some of the features of this boundary scan technique is as follows. Here we apply tests as some kind of instructions, like let me show you the overall prospective. Like I have a printed circuit board I have board. So, there are several chips which are residing on the board.

(Refer Slide Time: 03:28)



Let us say there are several chips, and on the edge of the board I have some kind of a connector through which I can feed some signals.

Now, my question is how do I test the individual chips, but the idea is something like this. So, so we tell the manufactures, that when you manufacture the chip you also manufacture something else. This is called something call a rapper, I just talk about it shortly. So, I manufacture something else means around each of this circuitry of the chip. So, once I do it my advantages, that I can connect this chips together for testing. Let us say this is the direction let us say. There can be other signals also I am showing just one signal. Now I am how do I do test? First I must tell from outside that what kind of test I want to do, that is done using something called a test instruction. This is like I am having a very simple processor in this rapper, where I am serially feeding in an instruction, this rapper is decoding what kind of instruction it is and it is taking appropriate actions.

Now, these boxes that I have showed dotted boxes, these are i triple e 1149.1 rappers. Now this rapper allows inter-operability in terms of test communication. They can test instruction I am feeding to the first chip; we have this chip fines that well this instruction is not form it is for the next one. So, it will simply by pass or forward it to the next chip. This will again chip if it is not for this it will BYPASS of forward to the next chip, like that it goes on fine. So, this standard allows test instruction and data to be serially fed into particular chip on the board it also allows the reading out the outputs or the test

results. Some of the chips may be having a best or a built in self-test mechanism that we will talk about later inside. This means the chip can test itself that can also be means included as an instruction. And this standard is hierarchical. So, you can work it at the chip level, PCB level, and also the system level where there is there are multiple such boards connected.

So, the serial output for one board can go into the serial output of the next board, like that you can change this is a hierarchical kind of a standard, not only meant for chips on a board, on a single chip you can do it, multiple chips on a board you can do it, multiple boards also you can do it. So, here you test not only the chips the circuitry inside, but also means you can test the interconnections. Because when we have several chips on a board, not only the correctness of the chips, but also whether the interconnections are correct, there is a break or short circuit, this kind of things also have to be tested right. So, JTAG allows all this thing to be done.

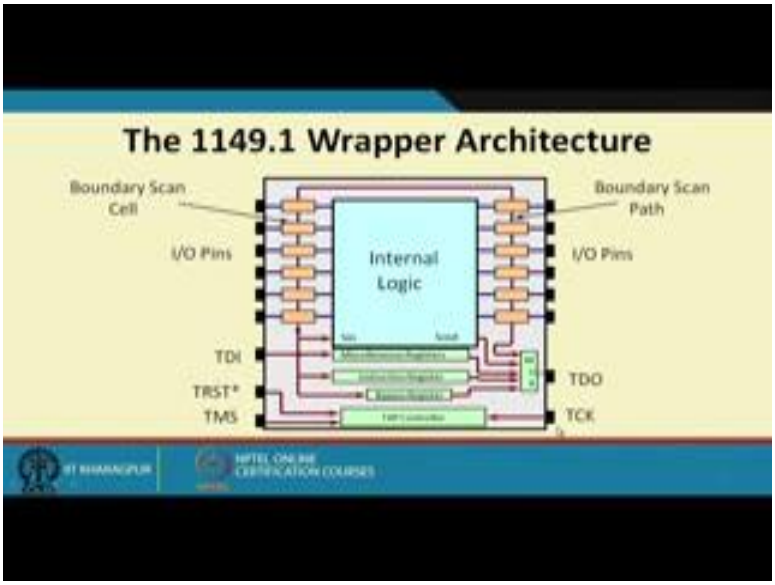
(Refer Slide Time: 07:31)

So, I said the basic idea is to have test rapper, for every chip or component that is manufactured now. In fact, the EDA tools using which you design the chips, they have a instructions a single instruction and instruction to create the rapper.

Once you are complete with the design, you can create the rapper with it using a single command. So, the rapper will be automatically generated and the corresponding net list is done. So, this as we show how it is done. So, that in the test rapper corresponding to

every input or output pin, you have something called a boundary scan cell. Now in addition you can have some registers. And some extra pins for testing for interfacing with the rapper some serial input serial output something like test control and so on. And there are some test instructions as I said which are also fed serially there is a particular format in which you can feed the instructions.

(Refer Slide Time: 08:43)

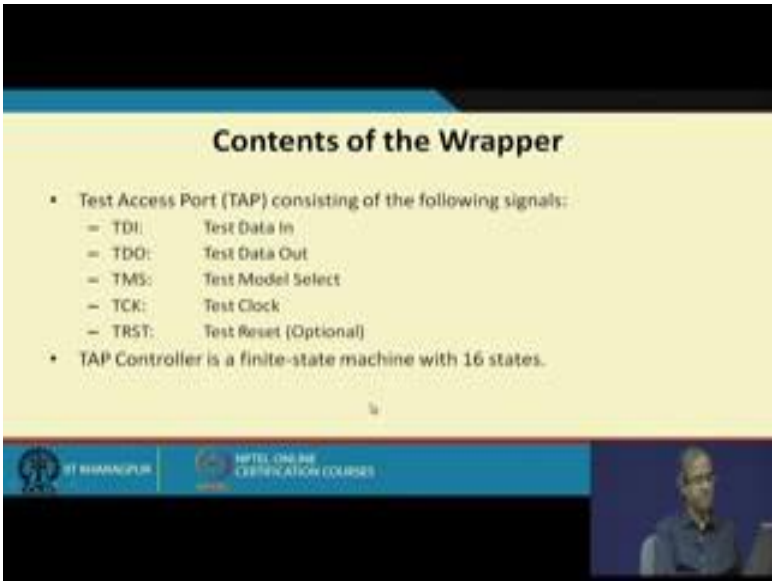


Now, this diagram shows how the test rapper will look like. You see this blue rectangle in the middle this is my actual circuit which you are supposed to be there in the chip. So, without all this thing this would be my whole chip, but now I have put so many other things also.

So, what I have done? This small rectangle boxes here these are the so called boundary scan cells. So, I have put one such scale, cell one such cell I means alongside every input or output pin. Now each of the boundary scan cell as you can see there of 4 connections. One from bottom top left and right, so they are connected on certain way. Like from the external pins of the chip when a single comes, the signal can be sent to this internal logic from left to right connection, but sometimes when you want to test something, you can configure them as the shift register mode. From here you can shift the data serially, along this path again you can serially, you can send the data out from this test data out or DTO. DTI stands for test data in, test data out. Now in addition there are some at some registers like an instruction register which can whole the test instruction that is being loaded.

There is a BYPASS register which can help you to skip this chip and go to the next chip if required. And there can be other miscellaneous registers multiplexors and connections. And these special signals 5 of them are shown. The one marks star means this is optional, but other 4 mandatory signals. They are controlled by something called tap controller. Tap stands for test access port. These signals constitute the test access port. Like here if you come back to this diagram once more I have shown. So, here I said that at the edge of the PCB I am sending some signals. So, actually these will be the test access port signals. So, I need 4 or 5 of the signals from here all right. So, this is how the rapper works. So, so once you design chip this circuit for a chip, you give a command the rest remaining part can be automatically included with it and your whole integrated chip which is now said to be 1149.1 complaint can become ready.

(Refer Slide Time: 11:42)



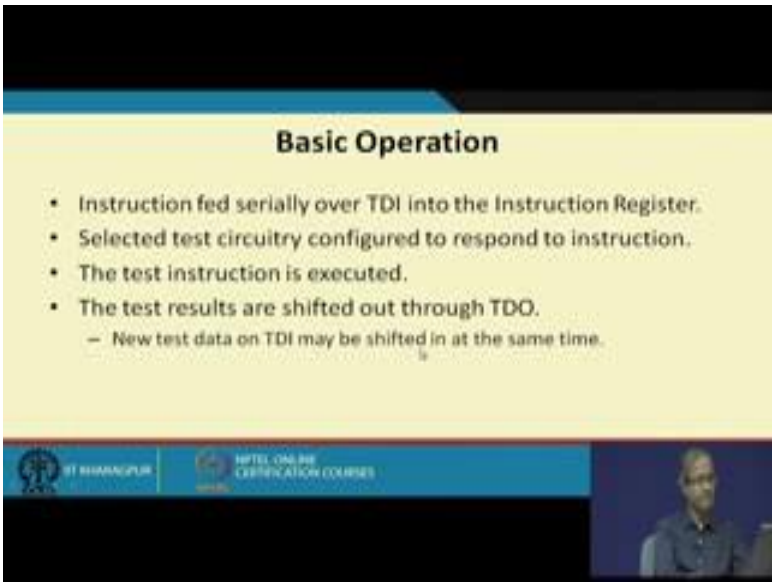
Now, the content of the rapper as I said there is called a test access port. 5 control signals are there one of them is optional. Test data in this is somewhat very similar to this scan in one of the scan chain method. Test data out is similar to scan out. Test mode select a similar to test control and test block. So, you see that the concepts which are used here are very similar to this scan path concept that we had seen just earlier. And this tap controller is again sequential circuit of final state machine, and there are 16 states actually I am not going to detail. So, such is not a very complex controller quite simply one.

(Refer Slide Time: 12:29)

Now, among the special registers, these 3 registers are mandatory. You must have the boundary scan registers alongside the input and output pins. You need to have a BYPASS register in case you want to skip a chip; you need to have a instruction register to store the test instruction.

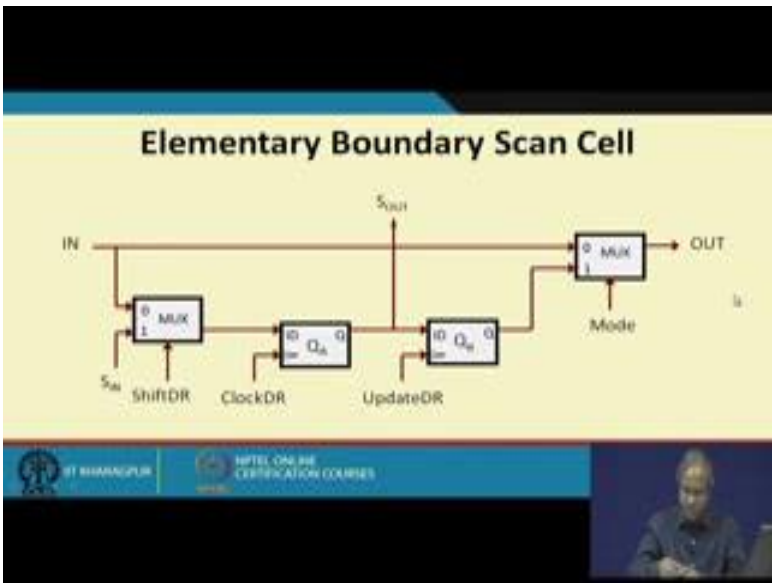
Now, in addition you can have some other registers which I have very special to design. Like you can use a register very stored the idea of a device. So, that from outside you can read out the idea and check the identity of the device which device it is. Similarly, there is some registers which are very specific to designs, design specific. Just let me tell you in this context, that for those of you who are familiar with FPGA boards and FPGA kits. So, so you may have seen that the way you do programming on the FPGA kit typically from a desktop or a laptop you connect a port that is called a JTAG port. Now that JTAG and this JTAG is same, that JTAG port was used primarily for testing, but now a day that same port is used for downloading the configuration data for FPGAs. The serial input through the TDI, TDI input because of getting shifted inside the chip.

(Refer Slide Time: 13:59)



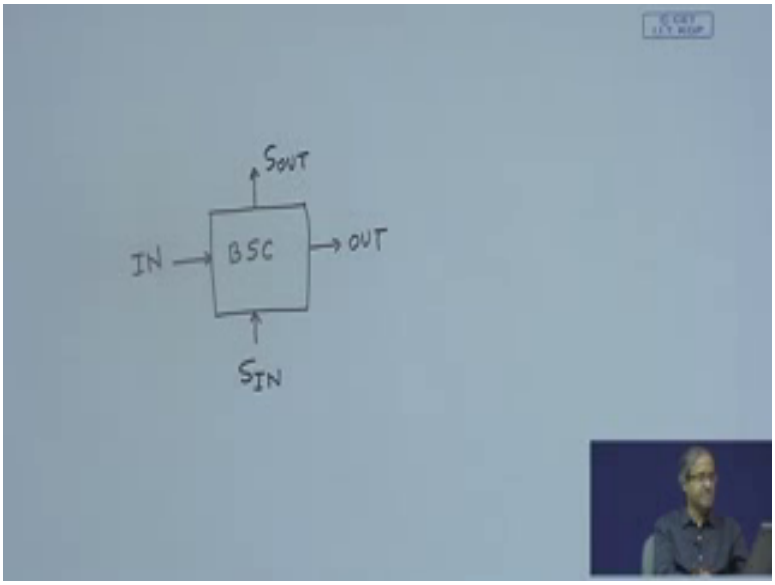
So, the same put is used for so other purposes also. So, the basic operation is that we feed the instruction serially into the instruction register. The selected test circuitry will get configured accordingly depending on the instruction which has been fed in. So, the multiplexes controls will be selected and so on. So, whatever is the intended will get executed. And after completion the test results will be shifted out through the DTO pin. And while this is being done new test data can be shifted on TDI just like scan out and scan in was over lapped in this scan path method equal to the same thing here also.

(Refer Slide Time: 14:41)



Fine now the boundary scan, boundary scan cell it looks like this. So, again in a schematic sense if you look at the boundary scan cell as a blog box boundary scan cell.

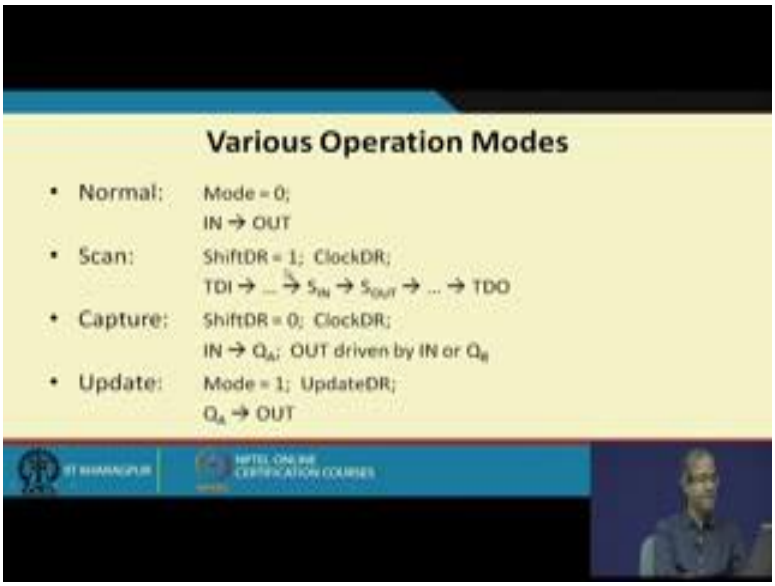
(Refer Slide Time: 14:52)



So, from the left side you have a signal let us call it in, and the right side there is a signal called out. So, on from bottom there can be a signal S in and from top 3 can be a signal S out.

This is the schematic. So, we can move a data from left to right or from bottom to top. Now let us see what is there inside. There are 2 flip flops, there are 2 multiplexors. So, when the input data is fed to a chip I want to send it directly to the circuitry inside. So, the remaining part is by passed in will go straight to out. So, this mode control if it is 0 then this 0 will be selected. So, it will go out. So, for going from S into S out the path followed will be this. From S in you select the lower input of the multiplexor, it will the stored in the first flip flop, and the output of this flip flop will go out here. There is also mode in which from S in you can move it to out. So, from bottom to right there also is a path, but there are 2 flip flops as you can see. One flip flop is used for shifting other flip flop is used for actually capture. Because see while this shifting is going on you should ensure sometimes that data here is not changing.

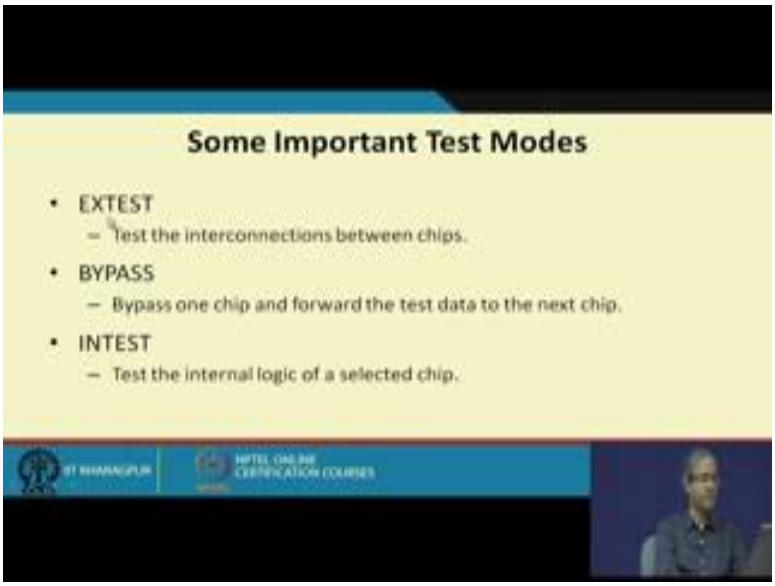
(Refer Slide Time: 16:55)



So, you can copy the data here retain this and during that time you can shift something here, some changes are going on in this flip flop, by the second flip flop and here this out will not change. So, roughly this is how the boundary scan cell looks like. Now basically there are 4 modes of operation. Normal mode I said mode equal to 0. So, n goes to out. Just I have said mode is 0 in goes to out. Second one I say this has a scan mode, here ShiftDR is said to 1 and ClockDR is activated. So, let see ShiftDR is said to 1 means S in is selected and ClockDR is activated which means S in gets stored here. So, I am creating chain of flip flops there are several such boundary scan cells connected one after the other one after they are connected. So, this this S in will go to S out, that will go to the S in of the next one S out. So, they chained as a shift register just like in this scan path design same way.

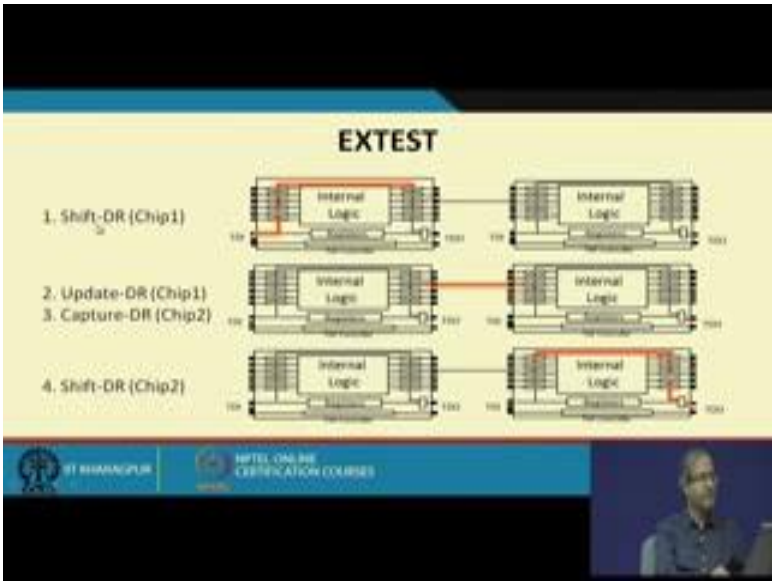
So, this is called scan mode. And in the capture mode shift divide equal to 0 and ClockDR. Shift divide equal to 0 means n is selected and (Refer Time: 18:06) input I am storing here. So, here I am not storing the value of S in, but whatever is coming from the input of the pin I am capturing it and storing it here this is so called capture mode. So, in goes to Q A and out can be driven by either in or Q B output. Depending on the mode it can be either from here or from here, but the important thing is that in is getting captured here. There is another mode called update where Q A to out the value of Q A can go to out. This is also there fine.

(Refer Slide Time: 18:46)



Now, here we shall be show you 3 of the important test modes of the boundary scan, there are other modes also. EXTEST BYPASS and INTEST, now the EXTEST mode is used to test the interconnections between the chips - BYPASS mode is used to skip one chip and go to the next one. And INTEST is used to test particular chip; that means, the internal logic. Let us look at the basic concepts one by one.

(Refer Slide Time: 19:23)



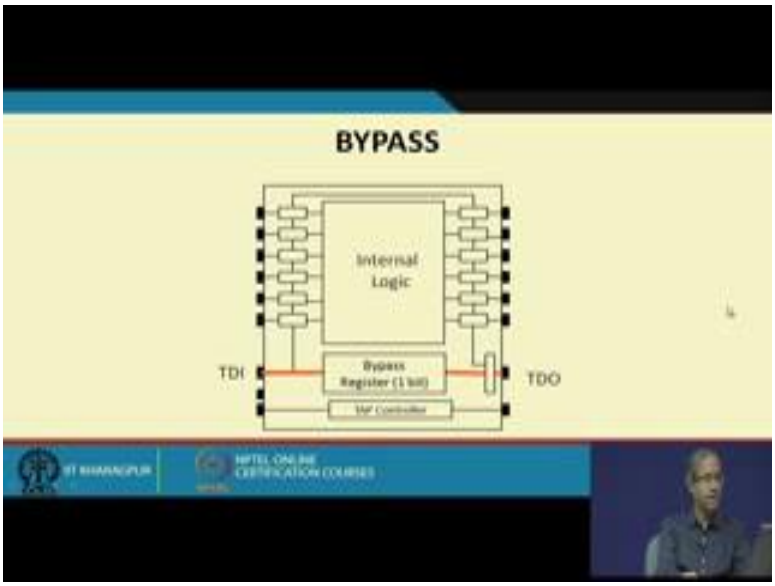
Well EXTEST diagrammatically it looks like this or the diagram may be too small for you to read, but I will just explain this steps. Suppose there are 2 chips on the board one

is this and the other chip is this. So, TDI TDO, what I do? I activate ShiftDR. So, what will happen if ShiftDR is activated let us look at this diagram once more, if ShiftDR is activated then S in gets inside here right. So, that same thing happens. So, it is actually this scan mode shift divide equal to 1, means I am looking at the scan mode. So, in the first chip we are in this scan mode, all the boundary scan flip flops they are in this scam mode. So, what I do now. So, after setting it in the ShiftDR mode we serially apply bits to TDI. So, this bit so will be serially shifted through this shift register, and there will be reach these scan cells. Suppose I want to test one of the interconnections here.

So, I wait till this beats reach this flip flop this boundary scan. So, I apply so many clocks. So, after it is done I do an update on DR, update means the data was they are here on this flip flop it will get shifted to the next flip flop and made available on out. Which means so whatever I shifting now the data will be available on the output pin, and capture DR means whatever is coming on this line this where chip 2. Chip 2 will be capturing it in the first flip flop. So, now, you see what are doing. What where saying is that whatever bit to us shifted here, I am moving that bit to the second chip I am capturing it here. Then after capturing I am configuring the chip 2 in the shift mode again scan mode, and again an applying clock so that this bit which has captured will get serially shifted out through the DTO pin. So, if this interconnection was faulty, then what bit pattern I am in shifting in and the bit pattern that is coming out will be different.

So, by checking this by checking the validity of this bit patterns, I can verify whether this interconnection is working correctly or not. The same thing can be done for multiple interconnections together. So, I can just capture multiple such patterns together and shift in together. This is EXTEST mode.

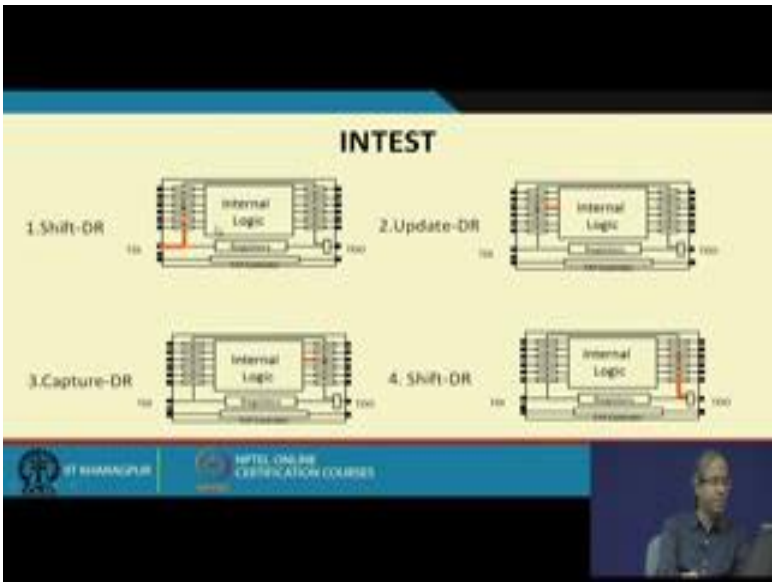
(Refer Slide Time: 22:15)



Then comes the BYPASS mode. BYPASS mode is fairly simple. There is a BYPASS register I mentioned, now BYPASS register is just single flip flop, it is a 1-bit register. In the BYPASS mode whatever I am feeding in TDI it doesn't go to the boundary scan cells. It directly comes to this 1-bit flip flop and after a 1-bit delay when a clock comes it comes to TDO. So, what I mean, whatever bits your shifting here, this particular chip will be bypassing that and it will be straight away sending them to TDO. So, it can go to the next chip.

BYPASS is used to skip a particular chip. And lastly let us look at test mode using which we can test the internal logic.

(Refer Slide Time: 23:04)

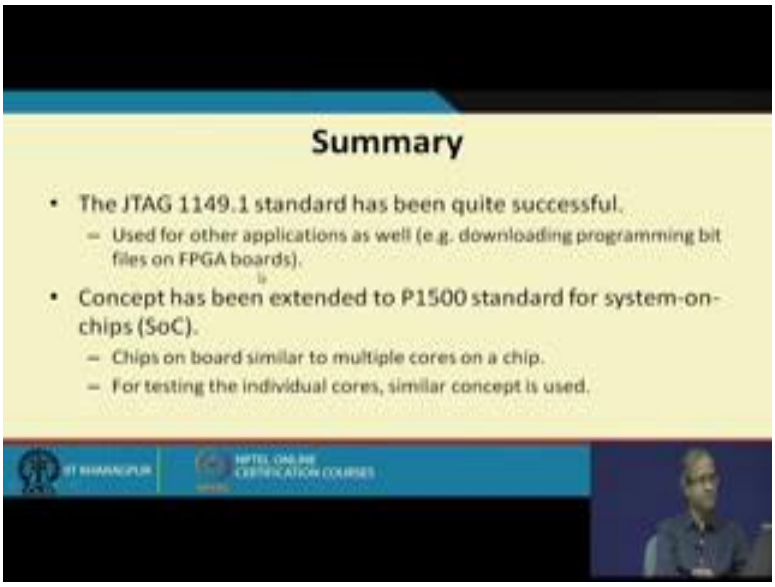


So, here the concept is quite similar as compared to EXTEST because in the first step we configure the chip in the ShiftDR mode. So, that whatever we feed through TDI will get shifted, but you see we shift it here I am showing up to here, but it will get shifted up to a point so that all the inputs to the internal logic and applied. So, once these are applied you go to the update DR one means, whatever there in the first flip flop will get saved in the second flip flop and now there will be available as input to the internal logic. So, now, the internal logic will do some computation based on the applied input, and after the computation is done you activate the capture DR signal. So, the output will get captured on the first flip flop of the boundary cells. Then again you configure in the ShiftDR mode and shift them out serially.

So, this is exactly similar to this scan path approach for sequential circuit testing, to scan in our test data like this. We scan out like this. Now here again, it is not necessary that will be scanning in all of them, may be a part of them we are scanning in, and let me also look at one thing, let me go back to that rapper diagram. Here you saw you see here that in addition to the boundary scan cells, there can be also a scan in and scan out pin for this internal logic. So, there is also facility whatever data your feeding that can go directly into your scan in of this internal logic. And scan out whatever is coming out that can also go out and the available over TDO. So, this mode is also there. So, it is not that you saying that internally you cannot use any scan path that also you can use.

So, it is like a combination. So, let us go head. So, you see that here, using all these test modes your able to get some kind of a board level in first structure, where you can test the individual chips on the board, you can even test the interconnections between the boards.

(Refer Slide Time: 25:46)



So, to summarize the JTAG 1149.1 standard has been quite successful in this sense that most of the chips that we you see today, that have been used, they have this standard built him. And just as I said that use for other applications as well which has nothing to do with testing, like I said the downloading of the programming bit files on the FPGA boards. Now this JTAG 1149.1 standard this has been extended also in a number of different ways, like there has been and analog boundary scan version a test standard which, which allows also analog signals to be fed to a circuit. This can be used to test the mix signal kind of chips, where there are both digital and analog components involved.

And other thing you know that today, we are moving almost we have already moved you can say so that is not today toward something called system on chip designs. It earlier we have talking about chips on the boards. Now the VLSI chips are become much denser. Now all those chips on the boards can be squeezed in to a single chip today. So, whatever was the separate chip earlier, will be something called a core inside my chip now my chip will be consisting of multiple cores.

So, whatever requirement we had for a board level testing, we have now the same kind of requirement for a core relative testing, but inside a chip. Multiple course some of the course might have been taken from some other designers, it may not be might design at all, I want to test the integration of the course. So, this is standard called P1500, this is meant for system on chip. This also quite popular for the present day system on chip designs, this is also an i triple e standard. So, which are also been used.

So, here as I said that chips on boards have been moved to multiple course on a chip. And we use very similar concepts. So, I think with this we come to the end of this lecture. So, in this next couple of lectures we shall be looking at something called built in self-test. Like a technique way a chip can test itself. That is the best thing which you can think of right, but there are constrains that we will see, but for today I think that is all.

Thank you.