VLSI Physical Design
Prof. Indranil Sengupta
Department of Computer Science and Engineering
Indian Institute of Technology, Kharagpur

Lecture- 05
VLSI Physical Design Automation (Part 1)

Hello welcome back. So, in this lecture we shall be looking at some of the steps in VLSI physical design automation that we shall be discussing in more detail in the modules to follow. So, the lecture title VLSI physical design automation part one.

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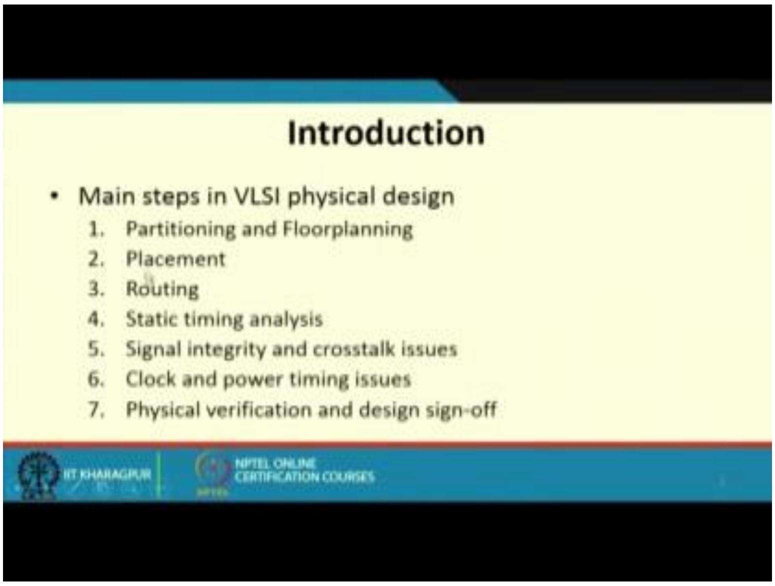

Introduction

- Main steps in VLSI physical design
  1. Partitioning and Floorplanning
  2. Placement
  3. Routing
  4. Static timing analysis
  5. Signal integrity and crosstalk issues
  6. Clock and power timing issues
  7. Physical verification and design sign-off

So, here if you look at the main steps in the VLSI physical design cycle, so here I have listed some. In fact, these are specifically the steps which I shall be discussing in this course in significant detail. So, again I repeat whenever I talk about VLSI physical design, I assume that I already have a circuit netlist available with me. Typically it is the transits level netlist it can also be a get level netlist, which can be technology mapped to standard cell libraries. So, I assume that that kind of netlist is already available to me then I go through some sequence of physical design automations steps in order to create the final layout.

So, the main steps are partitioning and floor planning followed by placement, then the very important steps of routing, then static timing analysis signal integrity crosstalk issues, clock and power timing design and finally, physical verification and design sign off when we are ready to send our final design to the fabrication facility for the ultimate manufacturing of the device for the chip.

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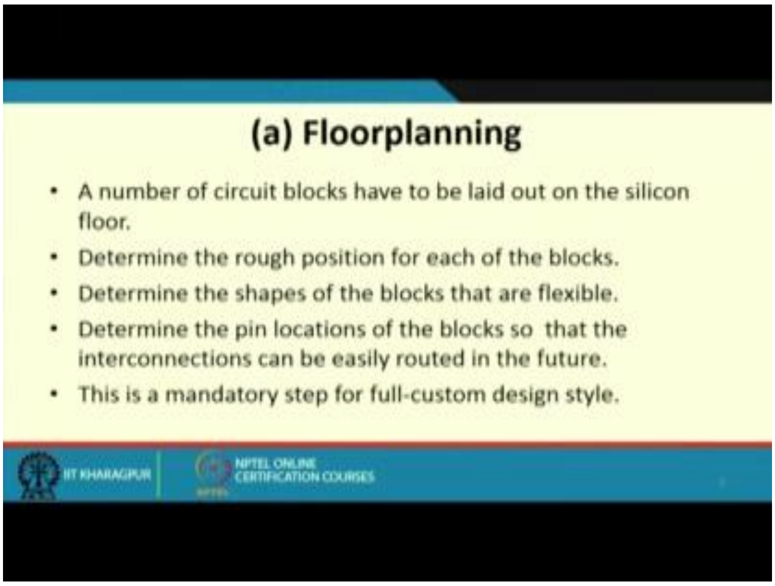

(a) Floorplanning

- A number of circuit blocks have to be laid out on the silicon floor.
- Determine the rough position for each of the blocks.
- Determine the shapes of the blocks that are flexible.
- Determine the pin locations of the blocks so that the interconnections can be easily routed in the future.
- This is a mandatory step for full-custom design style.

So, let us start with the first steps Floorplanning. Floorplanning what does it mean? A number of circuit block have to be laid out on the silicon floor, determine the rough position of each of the blocks, determine the shapes, determine the pin locations. You see I have mentioned the lot of things, let us talk about a analogy you will be able to appreciate better. Suppose you are building a house from scratch, it is not that flat your buying which someone else as constructed. So, you have a floor area, you want to create your floorplan and you want to create your own design with respects to the rooms, spacing and so on.

If you see what are the different steps, let me just carry an analogy. So, in floorplanning you have a number of circuit blocks that have to be placed, but here let say you are going for say a 2 bhk house a floor, here your blocks will be 2 bedrooms let us say 2 toilets, 1 drawing come dining room, 1 kitchen and 1 balcony these will be your blocks you want to place that say right.

Now, you have one idea regarding the approximate size of these blocks, because you know how big your 2 bedrooms should be, how big the drawing room should be, but the exact shape and configuration is not yet decided, that you can plan along with the other blocks when your placing them like for example, the drawing room should it be a square like, should it be a little rectangular shape, should it be l shape it and so on. So, the exact shapes of these blocks will have to be decided during this phase; not only that in VLSI floorplanning I mentioned about the pin locations, here in this analogy the pin location would correspond to the exact location of the doors and windows; so where you want to put the doors, windows and the corridors if required for connecting the different blocks.

So, there is a very similarity between these 2 problems. So, in VLSI we look at a similar kind of a thing, I have different blocks I have a fixed area of silicon where have to place everything, I have to tentatively find out or fix where to place this and if the blocks are flexible I can adjust the sizes like for example, if I have a block let us say whose area I know is 10 units by 10 units, but its layout is not fixed. So, I can laid them out in so many different was I know that the total area is 100 square units.

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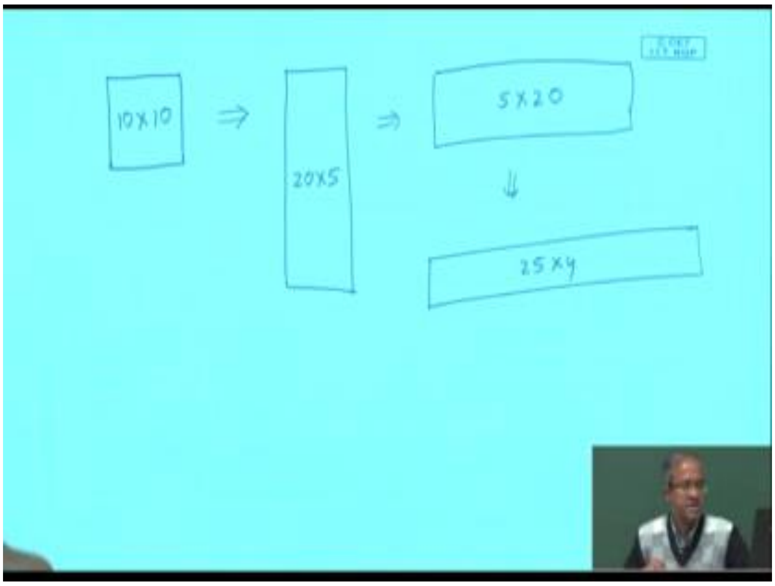

So, I can lay it out like this, I can lay it out 20 by 5, I can lay it out 5 by 20, I can lay it out 25 by 4. So, there so many options available to me right. So, during floorplanning you will have to exercise these options and find out which of this will give you the best kind of solutions. Now this is of course, a mandatory step for full custom design, now again here we are coming to the design style related issues, you think of the semi customers standard cell base designs where all the cells are placed in rows. So, now, my placement problem is not unrestricted, it is not that I can place anything anywhere up block or a cell I have to place only in one of the rows. So, the floorplanning problem part say does not exist in standard cell designs, for FPGA greater a does not exist; for FPGA floorplanning does not exist, you have to place a circuit module into one of the CLB’s only placement is there.

But floorplanning you need not have to do there, but of course, sometimes you can use some bit of floorplanning there, because you may want some circuit portion to be allocated to one part of the FPGA, in order that delay is interconnection delay is are less. There are ways to inter connect with FPGA software to force that certain blocks must be mapped to the CLB’s, which are located in a close neighbourhood within a rectangular region those you can specify fine.

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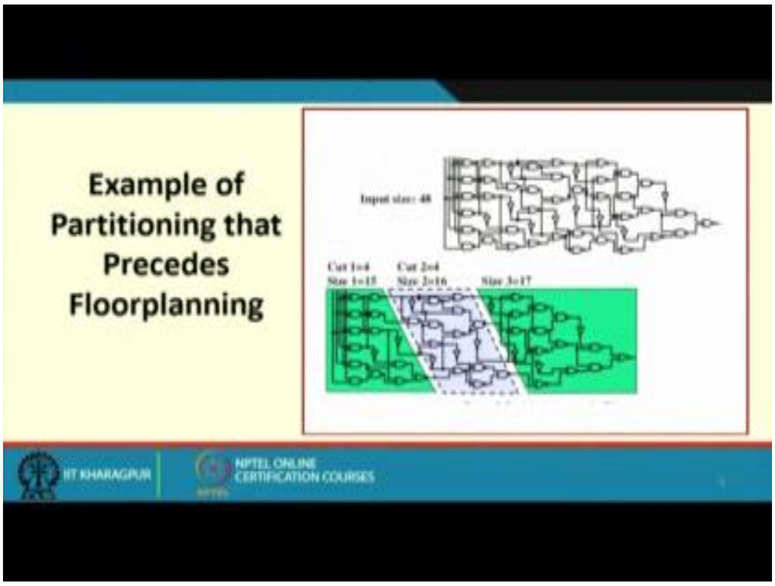

Example of Partitioning that Precedes Floorplanning

Now, before floorplanning or along with floorplanning, there is another steps call partitioning which are carried out. You see partitioning are carried out for various different reasons, before I explain this side this slide let me just tell you. Suppose I have a very big design, and I have a particular technology using which I can manufacture a chip, let say let say for example, I am capable of fabricating 1 million gets in the chip, but I see that in my design there are 2.5 million chips. So, what I know is that I have to break my design into 3 chips, that is what I need in 1 chip I cannot put.

So, how to partition my whole design into 3 you can say partitions, such that each of the partitions size will be less than 1 million and of course, another very desirable thing is that the number of connections between the partitions should be minimized; because I would not like a scenario where I need 1000 connections to be made between 2 chips; because whenever you go of chip the delay is increase by an order of magnitude. So, I would like most of the inter connections would be inside the chip only few connections will go between the chips right. Similarly here I have an example where you can see that there is a gate level netlist here.

So, there are 48 gates, suppose I want to divided it up into 3 partitions, the diagram below shows a good partitions, where you can see the 3 partitions in different shades where you see that the sizes of this partition are approximately equal in size 15, 16 and 17 and also you look at the number of interconnection words between the partitions, between first and second partitions there are 4 connections. So, we say that this cut size is 4, similarly between second and third there are 4 connections this cut size is also 4, first and third there are none. So, we can say that this is a good partition. So, this partitioning can be done at any level I talked about it at very high level in terms of chips you can do it, you can do it in any level in fact. So, this partitioning is a important steps before you go for mini placement or floorplanning typically.

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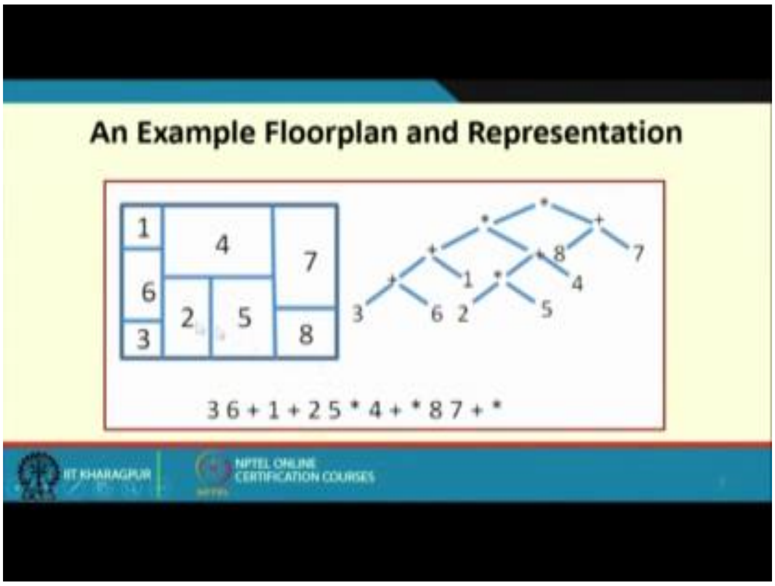

An Example Floorplan and Representation

3 6 + 1 + 2 5 * 4 + * 8 7 + *

Now, let us come to a floorplanning, in this diagram here we show the representation of a floorplan, how floorplan is represented. Like on the diagram here in the left you see 1 2 3 4 5 6 7 8 this represent 5 modules or blocks, there areas roughly indicate there sizes, right.

Now, this is the rough floorplan that I have arrived that, while in terms of the house again I can say this 4 will be my drawing room, this 7 and this 2 will be my say bedrooms like that, this 1 can be my kitchen and so on. So, once I have a floorplan like this, how do I represent it because in a typical VLSI circuit, I am talking about a situations where there are thousands and thousands of such blocks may be more; so how to handle them, how to represent them efficiently so that I can carry out some manipulations, I can arrive at a good or efficient floorplanning.

So, here we show one possible ways of representing of floorplan in terms of a tree, this tree represents a cut, see here you can see that the knowns are mark either as plus or a star.

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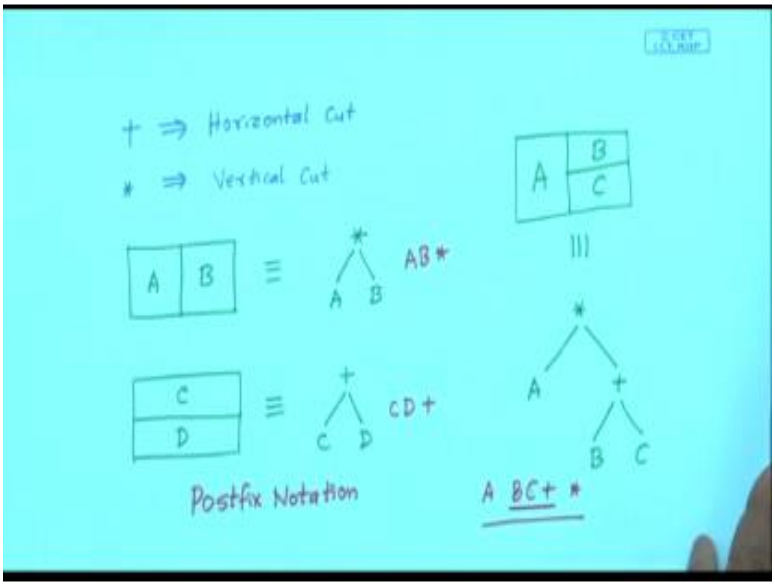

So, what I mean is that this plus means a horizontal cut, and the star means a vertical cut well what does this mean? Suppose I have a floorplan where I have 2 blocks A and B placed side by side separated by a vertical partition, so this I represent as follows. Similarly if I have a scenario where 2 blocks say C and D represent by horizontal partitions, I represent it as this. Let us take another example slightly composite one, let say I have this. So, the way I represent is that first I use this vertical cut. So, star. So one side it is A and the other side is this whole thing, this whole things again has a horizontal cut, so plus B and C. So, this is one way of representing a floorplan. So, let us now come to this example once more, in this example this is one possible tree representations because it is not unique like starting from the lower level, 3 and 6 are a connected by a vertical line by a horizontal line.

So, 3 6, 3 6 together is connected to 1 by a horizontal line. So, again a plus 3 6 and 1; 2 5 connected by a vertical line, 2 star 5; then this and 4 are connected by a horizontal line with the plus 4, and this whole thing and this whole thing are connected by a vertical line. So, again a star this and this and the other side 8 and 7 where horizontal line and this again with the vertical line right. Now this is a tree this is a graphical representation, now for those who have studied a computer science data structure you will know that any such tree this is a binary tree with some operators in the vertex notes, and some modules in this case in the leave notes this can be represented in the so called polish postfix notation. So, what is polish post fix notations? If you see this one this A B and star, this I represent as first the 2 leave notes then the operator on top A B star I write it like this, this I write as C D plus.

This one I write as first this 1 will go, B C plus I first do this then A and this, then A this whole thing star this is how polish post fix notations are written, and this is I unique notation this does not need any parentheses or brackets.

So, you know that that any operator if we encounter you operated on the previous 2 operence. So, plus will work on B and C you get something, star will work on A and this. So, you get this with. So, step by step you can go right. So, here you can also see this we have done exactly the same thing 3 6 plus means this one 3 6 plus, 1 plus that means, 3 6 plus and 1, plus 3 6 plus and 1, plus 2 5 star, 2 5 star is this, then 4 plus with that 4 is plus and this whole thing and this whole thing there is a star this, 8 7 plus 8 7 plus this whole thing and this 8 7 plus is star, so like that it proceeds.

So, here you can work out this is actually called postfix notation. So, a floorplan can be represent it as a postfix notation provided it is sliceable, you can slices it into horizontal and vertical lines like this.

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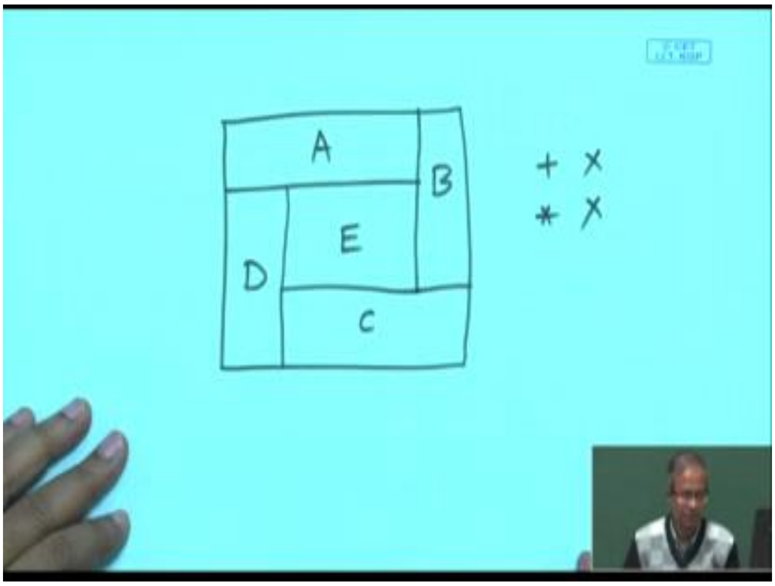

But we shall see later when you discuss in detail that there are certain floorplans which cannot be represented in this notation right I am showing an example. Suppose there are 5 blocks A B C D E, but there is no continues horizontal or vertical lines that can slice this floorplan. So, here you cannot use plus, you cannot use star, this cannot be represented like that. So, we shall see later that how to handle this kind of floorplan, right.

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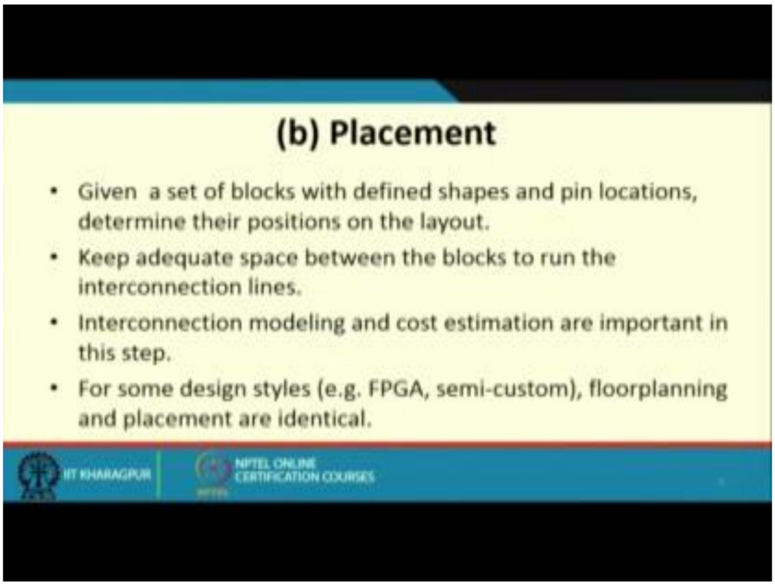

(b) Placement

- Given a set of blocks with defined shapes and pin locations, determine their positions on the layout.
- Keep adequate space between the blocks to run the interconnection lines.
- Interconnection modeling and cost estimation are important in this step.
- For some design styles (e.g. FPGA, semi-custom), floorplanning and placement are identical.

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So, after floorplanning the topic that we shall be discussing is called placement. See during floorplanning we have already fixed the approximate locations of the blocks; like we have said so again with respect to the design of a flat, I said that here I have my first room, here this second room, here the dinning space and so on. I have tentatively fix the locations, but the next question comes how do people moves from this room to that room. So, for that possibly I will need some additional corridors for places to work and reach their approach.

So, with respect to VLSI design, I needs some additional space through which I can inter connect the blocks this so called routing areas are required. So, the placement problem says given a set of blocks with defined shapes and pin locations, determine the position of the layouts; not only that you keep adequate space between the blocks to run the interconnections. So, here interconnection modelling and cost estimations are important because you see the exact interconnection you will be doing later during doubting, but now you are trying to keep some space, and place the blocks in optimum way such that your expected cost is minimised. We have to use some simple estimation of routing cost, so that you can evaluate and compare between 2 alternate placement solutions you can see that will this is more expensive than the other so you take this fine. And as it said for some design style like FPGA and semi custom standard cell based, floorplanning and placement problems are identical there are not different, but for full custom they have to be done separately.

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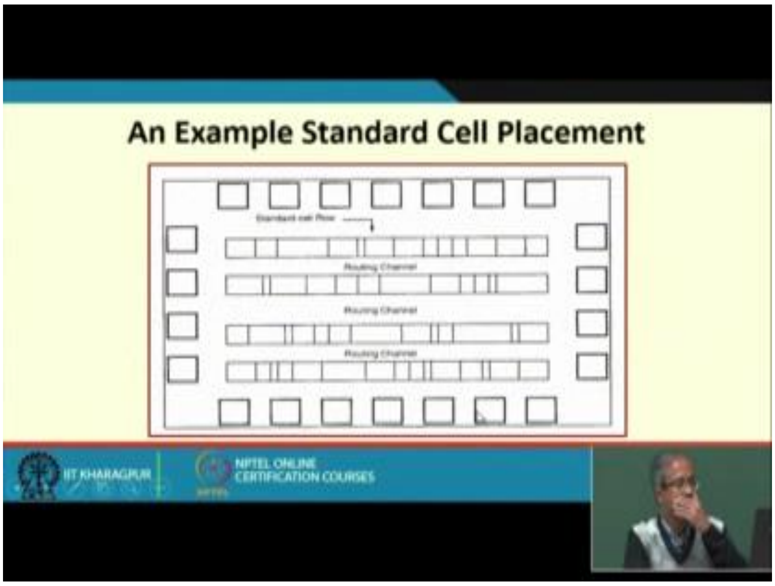

An Example Standard Cell Placement

So, let us look at this standard cell scenario once more, a standard cell chip floorplan would look like this with the I O pins, the I O cells on the boundaries and the rows will be this standard cells with routing channels in between. So, normal placement problem will be here has I mention again earlier, how to place a cell into one of the rows and once you are place this cells, you can estimates the routing channels cost and you can keep adequate space for that. If you see for standard cell the problem is not difficult, if you see later on that your space is a little less you can move the entire row a little up or down. So, you can do it later those adjustment you can do it later, but for a general say means full custom thing where there is so many blocks moving a block around is not so easy. Because moving a block to make space here, might make the space on the other side less that can create a problem right.

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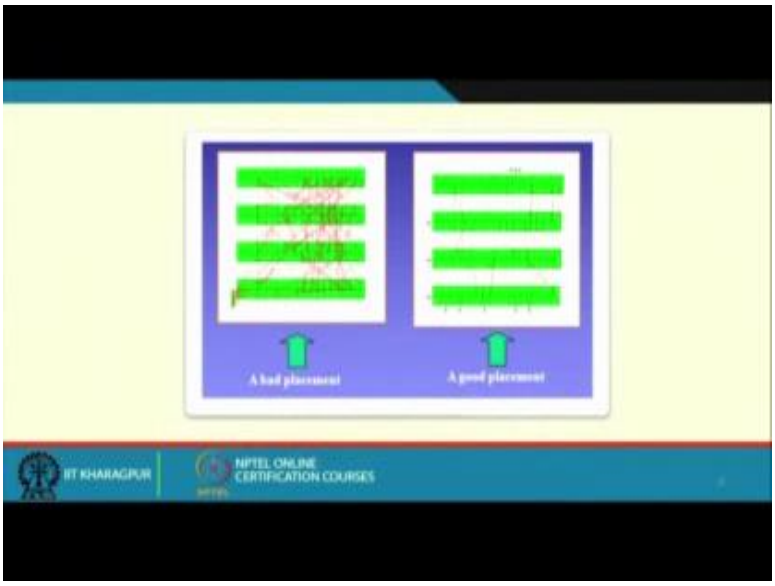

So, this is 1 and again here if you can see that I have shown 2 standard cell placements, this is so called bad placement and this is so called good placements. So, the interconnection here I shown by straight lines, just to see how complex the connections are; so in the first case you see there lot of zigzag lines large number, but in a second case you will see the lines are mostly local confine to the channels, and only a few connections are across channels. So, this is a good placement. So, the important of placement is quite cleared that if I have a good placement I can have the routing problem much easier later on, and also I can come or I can arrive at a final design, which will be more efficient in terms of performance; because today interconnection area and interconnection delays are dominating the total performance of the circuits. So, if I can keep my interconnection simple and short it will help me in the long run.

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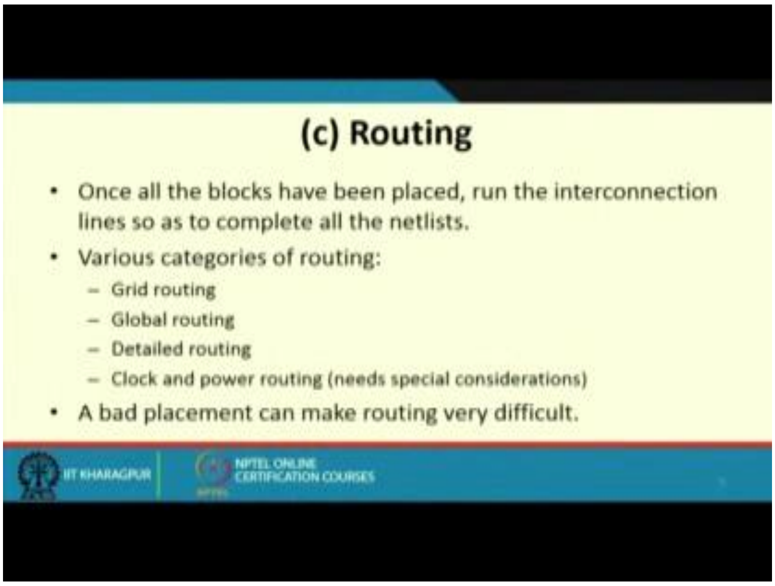

(c) Routing

- Once all the blocks have been placed, run the interconnection lines so as to complete all the netlists.
- Various categories of routing:
  - Grid routing
  - Global routing
  - Detailed routing
  - Clock and power routing (needs special considerations)
- A bad placement can make routing very difficult.

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Once your place the blocks, now comes routing; so once the blocks have been placed, you run the interconnections lines so as to complete all the connection for the netlists. Now there are various categories of routings: grid routing, global routing, detailed routing, clock and power routing etcetera that we can talk about. And the thing is that black bad placements can make the routing problem very difficult as I said, grid routing means grid routing is a problem which is quite general which says that I have.

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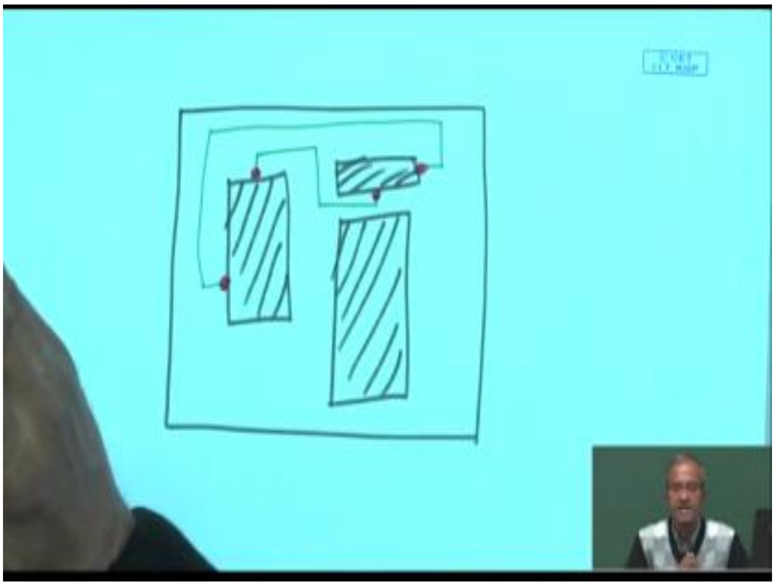

Let us say let me show diagrammatically, say I have a layout area this is my total silicon floor and I have already some blocks which have place, which means this are obstacles, I cannot run an interconnection through this blocks. Let say like this and suppose I have a problem where I want to connect a pin which is located here to a pin which is located say here.

So, normal problem will be this grid routing says that how to complete this routing over coming this obstacles. So, there are so many alternative paths. So, let say this can be one alternate route. Now once we have done this now say now so I have another problem next, but I want to connect a pin here with a pin here. Now obviously, since we have laid out this line on the same layer, you cannot follow the same route because there would be cross. So, here possibly will have to take a route like this.

So, this is the problem of grid routing; there are obstacles, there are points or pins to be connected, try to determine a path typically means as short as possible so that you can complete the interconnections right. So, when additions to this, there are global routing and detailed routing problem. So, I can given example here.

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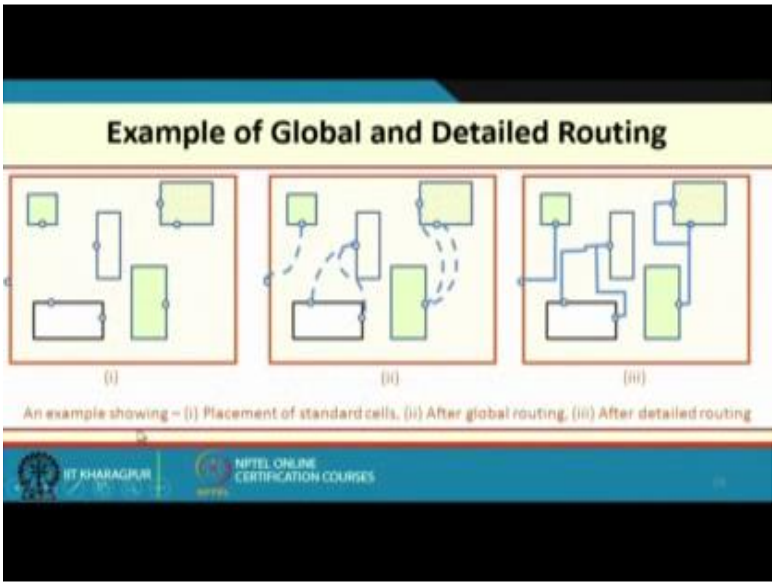

Example of Global and Detailed Routing

An example showing – (i) Placement of standard cells, (ii) After global routing, (iii) After detailed routing

Suppose there are blocks out here some pin locations are shown they have to be connected in some way. The second diagram shows the result of global routing, global routing what it does is that it does not means, it does not interconnect the pins in a precise way, but rather it tries to find out an approximate route; like you say these 2 pins have to be connected over this part, these 2 pin can use this part, this pin can be using this part, to connect this 2 pins I can follow this part, because there can be other alternative for example, this connection I could have used a path like this.

So, it approximately tries to find out the part, this is global routing. Now once a global routing is done then each of these individuals regions you consider 1 at a time and try to complete the exact wiring.

So, here I am showing all the wirings on the same layer, but when we took that example of the channel routing, you recall I used 2 different colours to show the words running on 2 different layers, one horizontal one vertical they can connect at certain points if required. So, this is global and detail routing roughly what it means. So, later on we shall be looking into this in much more detail and we shall be working out lot of examples.

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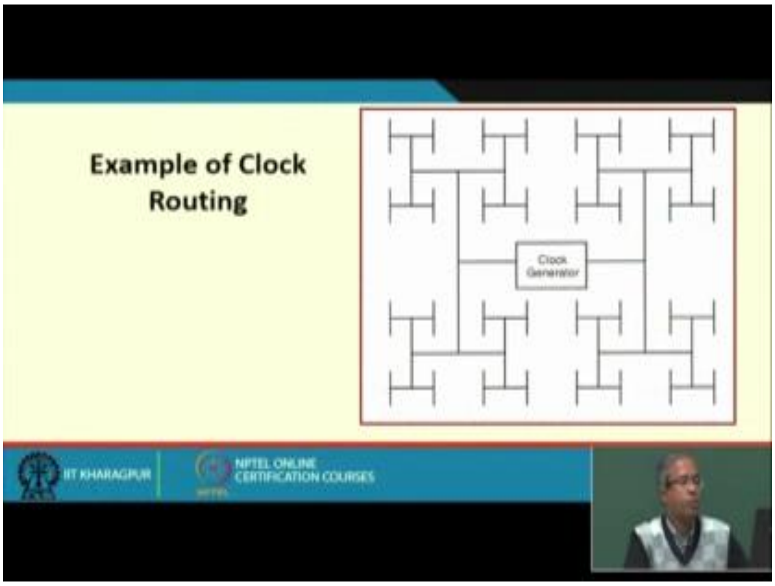

Example of Clock Routing

Of particular important is clocked routing, now you see clock is a very important signal there are many sequential circuit elements all throughout the chip; flip flop registers, counters they all required clock and because typically clocks are h regard many of the flip flop get regard by the edges, if there is a variation and delay of the clock signal to one flip flop as compare to the other, then may be one flip flop might get switched earlier than the other. So, in a circuit this might lead to incorrect operations, if all the flip flop that us suppose to switch together there is a delay in switching. So, there are many methods which have been propose, which we shall discussing to handle clocked routing. Like one method I am showing here this is called H tree, because you see every intermediate steps look like a H. So, the clock generated is the middle and all this points at the terminals of the H these are the points from where clock signals are taken.

Now, if you just measure if you just see from the clock generated up to each of the terminal point, the length of the interconnection is the same which means the delay of the clocks will be identical up to each of this points. But the trouble with this method is that in typical layouts you do not have the clock location so regularly placed, they will be f a z and random of n, you often do not get the opportunity to layout these h type layouts very neatly there, see you can have layout with there a lot of opposite things. So, we shall see all this things later in the next lectures. So, I thing we can just end today this lecture.