VLSI Physical Design
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Lecture – 44
Interconnect Modeling (Part 2)

So, we continue with our discussion on interconnect modeling. So, in our last lecture if you recall we looked at some of the resistive and capacitive affects on the different layers and as we move from one layer to the other, how the values and magnitudes of the resistance and capacitances can vary.

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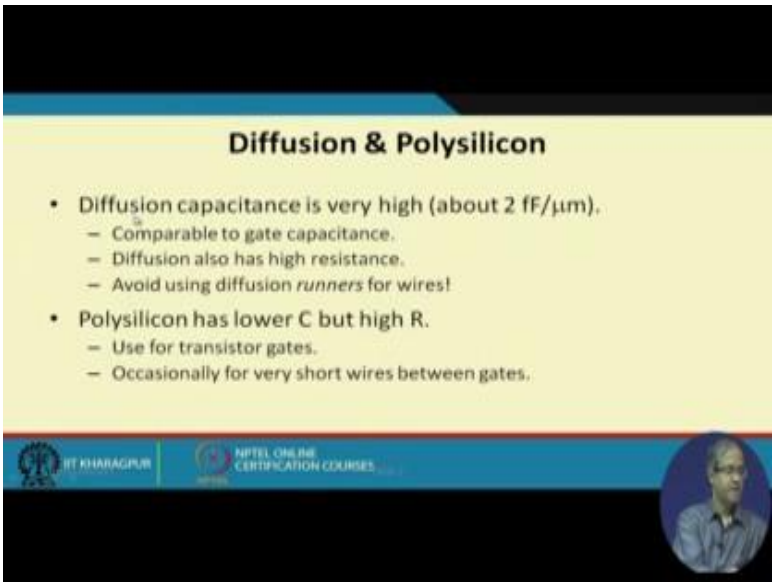

So, continuing with our discussions we now look into the diffusion and Polysilicon layers. So, we have seen that the diffusion capacitance for both n and p regions are very high. How high? The values are comparable to gate capacitances. So, another problem with the diffusion layer is that diffusion is also having high resistance. So, diffusion is one layer, where both the resistance and the capacitance values are higher. So, it is absolutely you can say discouraged that some interconnection between 2 elements in the layout should be made on the diffusion layer. But in contrast a Polysilicon layer has lower value of capacitance, but the resistance value is R is high still, but since the capacitance value is much lower than diffusion. So, for some cases where you need to

interconnect 2 points which are very close apart, you may use the Polysilicon line for connections like I shall give you an example.

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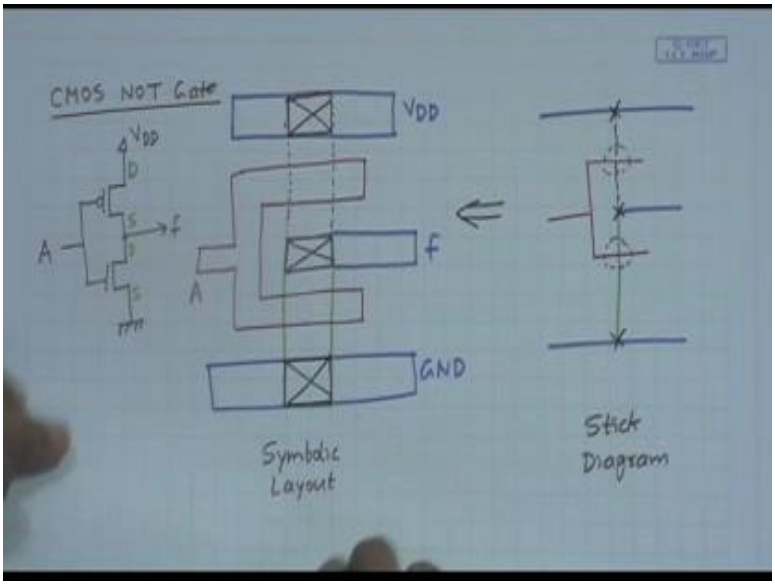

You look at this layout which we had seen during our last lecture, where we showed the layout of a CMOS inverter so how it looks like, right. So, well, I shall not be showing the actual symbolic this schematic layout, I shall be showing this stick diagram.

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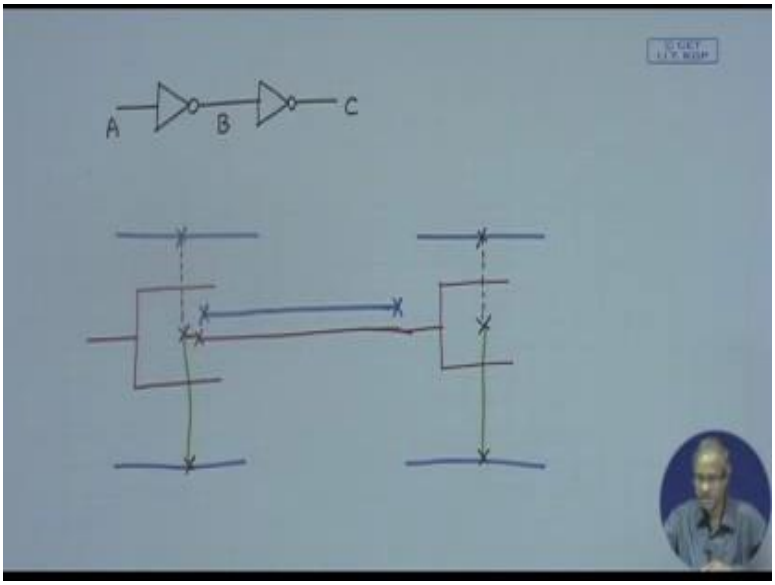

But the case that I shall be talking about now is let us say we have 2 inverters that are connected in cascade; maybe we are designing some kind of a buffer. Let us say this is A

this is B and this is C, let us try to draw the stick diagrams. So, the stick diagram these are the Vdd and the ground lines I am showing for the 2 gates side by side, these are the diffusion lines this is the p diffusion. So, there is a contact here, contact here, contact here and contact here then we have the Polysilicon line forming the 2 transistors, and there is another Polysilicon line forming the 2 transistors.

So, this is actually the stick diagram layout of this function. So, now, one thing you just see in our previous case this layout here we had shown that the output f was being taken out on a metal layer. So, this contact connection was actually a contact between a diffusion and a metal, so that is why this line was shown as blue. But if you look at this scenario here, so this output has to go to the input of the next inverter. So, this output has to be carried to this point. So, there are 2 alternatives I am showing them side by side. So, (Refer Time: 04:30) alternative is from here you carry a metal line and here you make a contact connection and here between metal and Polysilicon you make another contact connection.

Now the other alternative may be; so I am showing it just one below the other that you do not draw this line on metal at all, directly use a Polysilicon line. If you do that so on one side you do not need any contact it is already in Polysilicon. So, only on this side you may you need a contact between Polysilicon and diffusion. You see each of these contacts they occupy additional area and they also just incur additional RC over a delays and other things. So, reducing the contact is a good thing. So, if these 2 transistors are closer together, then you can possibly connect them directly like this and the output you can take on Polysilicon so that it can be fed directly to the next gate.

So, this is exactly what is being mentioned here, that you can use Polysilicon occasionally for very short wires between gates, but diffusion should be avoided as interconnections because both R and C values for diffusion layer is high.

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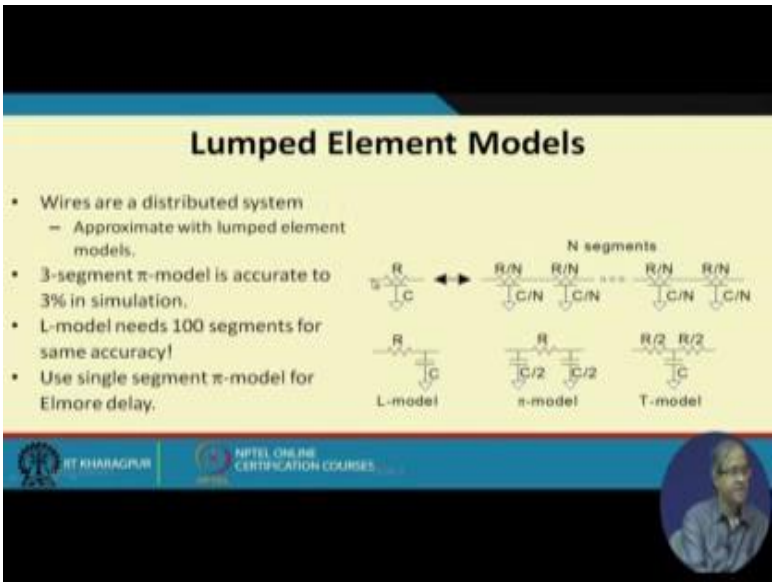

Fine now when we model wires. So, we have seen earlier also in the various delay models there will be distributed resistance and capacitance values. So the total resistance resistive load that is faced can be R, and the total capacitive load can be C, but when the wire runs over a long distance, so we usually represented by a model like instead of the total resistance R in one place, as if there are N segments and the resistance say R by N, R by N are coming in series N times. Similarly the total capacitance C this can appear as C by N, C by N, N times in parallel. So, these are some ways of modeling this interconnection wire.

So, wires are treated as a as distributed with this R C values distributed along its length and this is actually called lumped element models and the way you distribute this values there are traditionally 3 ways, one is called the L model, where for R and C you show it like this, this R is in series after that C is coming in parallel to ground. The pi model it looks like the pi this structure, the R is in series and the total capacitance is split into C by 2 and C by 2 they are coming in parallel before and after and T model is the reverse where the C is not split, where the resistance value is split it looks like a T. Now various models like these have been analyzed and with respect to the more accurate delay a characteristic which is obtained by extracted values resistance capacitance and other things have been compared. So, it has been found that this is one segment of the pi model.

So, if you use 3 segments one followed by another followed by other, that is seen to be accurate enough which is means 3 accurate to 3 percent, that is 3 percent of the actual. So, a 3 segment pi model gives very good results, but if you are using L model, then to achieve that same degree of accuracy you need 100 segment of this L model. So, this will be much more costly in terms of the computation time during simulation. And means earlier we seen that we often use Elmore delay model to estimate quick estimation of the of the interconnection delay when you are doing the clock routing and other things, when you are trying to balance the delay, but there we need some estimate we should be quick. So, if you say that you are using multiple levels of these models then simulation, it will take time. So, what is done for those cases is that single segment pi model pi model is used for estimating the Elmore delay in those cases short wire segments.

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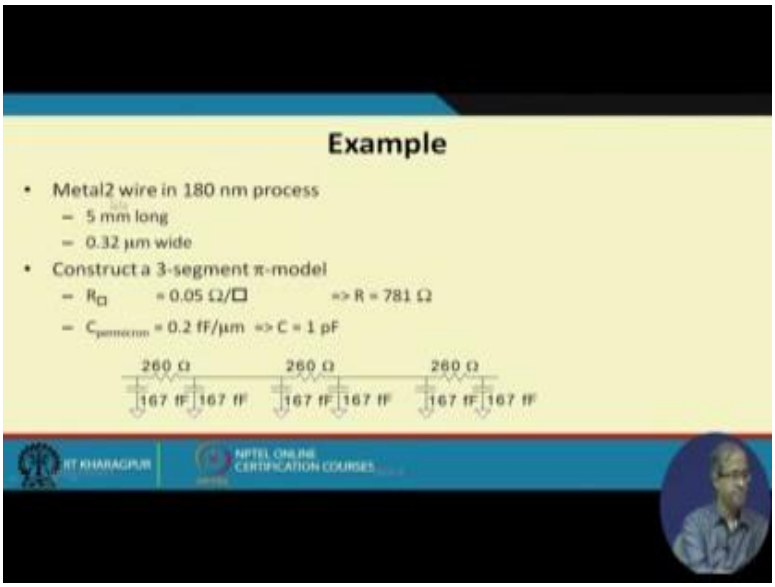

Now, this is an example where 3 segment pi model is shown. So, the example is like this let us say so we again take a 180 nanometer process, we consider the metal 2 wire. Let us say it is 5 millimeter long and 0.32 micrometer wide.

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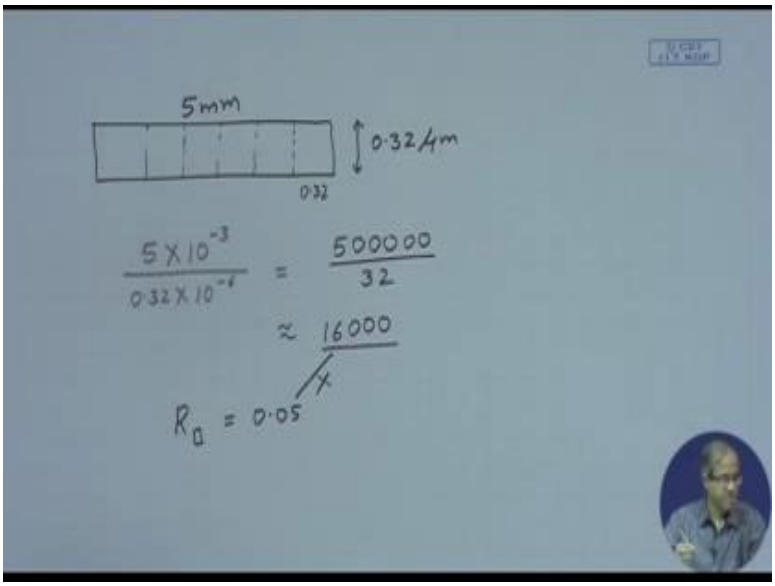

So, how does the wire look like? The wire look like this the length is pretty long 5 mm, and the width is 0.32 micrometer. So, if you again similarly as I said earlier try to discretize it in terms of square boxes, each of this square will be 0.32 micron into 0.32 micron this will also be 0.32. So, how many of such boxes will be there? So, if you divide 5 mm with this, 5 mm means what? 5 milli into 10 to the power minus 3 divided by 0.32 into 10 to the power minus 6, this comes to 5000 and if you just take out this 32 another 2 zeroes divided by 32. So, this will be this will be approximately 16000, right.

So, this is means if you consider that for metal 2 wire, the value of R box is 0.05 ohm per box right. Now number of boxes you have already estimated 16000 approximately. So, if you multiply 0.05 by that figure 16000, the total resistance comes to about 781 ohms, so this is how you calculate the resistance. Just estimate the resistance value of a box resistance value of the box is already given, R box is 0.05 and you multiply these 2; resistance of a box multiplied by number of boxes. So, this value comes to about 781 ohms.

And also the per micron capacitance here for this metal 2 wire is about 0.2 Femto farad per micrometer. Now because the wire is 5 mm long, which means 5000 micrometer if you multiply it becomes 1 Picofarad. So, in a 3 segment pi there are 3 resistances 781 divided by 3 is about 260. So, 260, 260, 260 and this 1 Picofarad divide by 6 it comes to 1 67 Femto farad approximately. So, each of this capacitance will be 167, because if you

add them up it will be 1 p F. So, this is how the model is created. Now once the model is created there are several ways to actually simulate spice simulation can be done or means other very quick estimation of delay can be done from this model.

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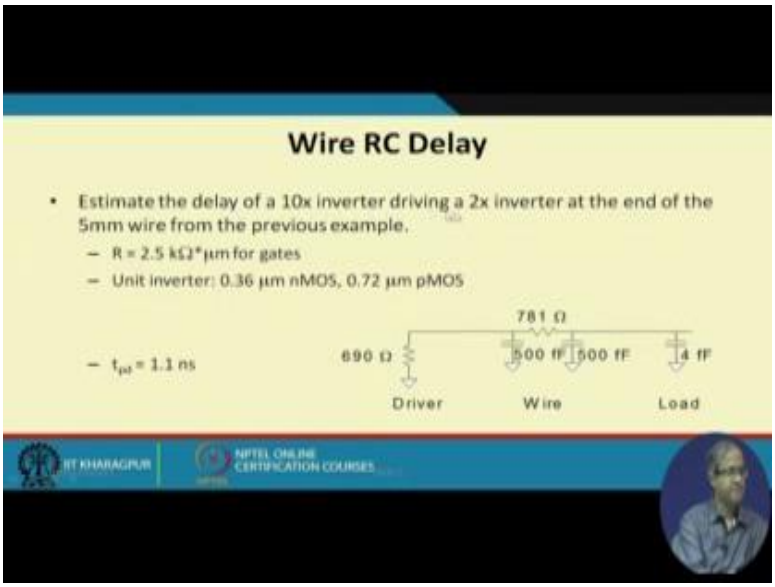

Next let us look at a way of estimating the, you can see the R C delay of a wire. So, let us take an example a 10 X inverter driving a 2 X inverter means.

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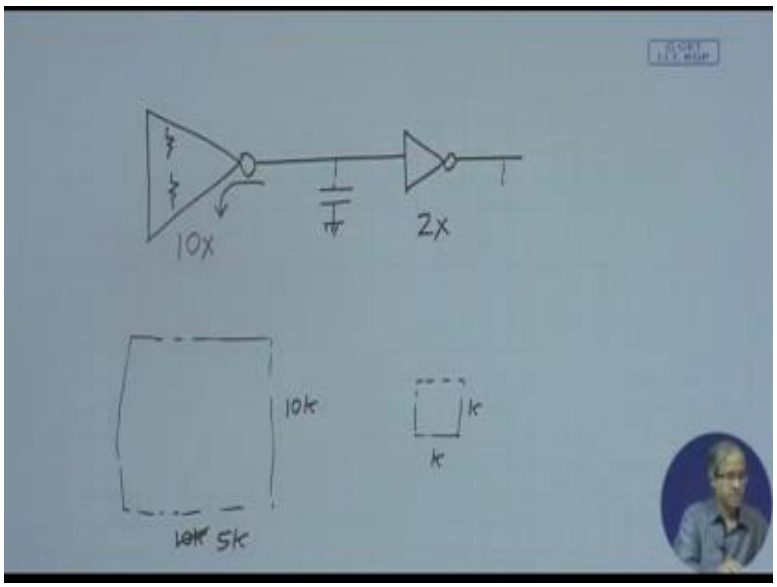

I have a large inverter which is driving a small inverter; this I am saying 10 X, this I am saying 2 X. 10 X is now you can understand, so here the area of the channel can be like

this let us say k by k, but in this case for 10 X the area of the channel will be 10 k by 10 k, this is what we mean by saying it is 10 X. It is 2 X of course; sorry it should be 5 k in that case 5 times. So, in this case we assume that the resistance value is 2.5 kilo ohm micrometer for gates resistivity, and here when you are considering the Elmore delay R for RC we usually consider Elmore delay. So, in the previous case we have already estimated this 781 ohms and 1 Picofarad. So, this is 781 ohm and 1 Picofarad is split into 500 and 501 stitch pi.

Now, for the gate here the features are 0.36 micrometer for nMOS, and now here we have considering the path to ground which is nMOS. So, if you 2.5 kilo multiplied by 0.36 if we just calculate, it comes to 690 ohm; so the effective resistive load here will be 65 ohm. Similarly on the other side there are 2 transistors which are of course, 2 x. So, if you similarly estimate the capacitance of those of those n and p type, this comes to of course here it is not shown, it comes to 4 femtofarad. So, if you simulate this whole circuit now. So, you have modeled the driver, there is an inverter which is driving effectively. So, what I am saying is that the there is a pull down there is a pull up. So, in this model I am looking the path to ground. So, pull down is 690 ohm, and here there is effect here there is a capacitive load, which indicates the sizes of the pull up and pull down transistors.

So, if you simulate this, the delay, comes out to be about 1.1 nanosecond. So, this shows that if we have a problem like this. So, using some modeling like this and then using simulation, there are tools available you can get the delay.

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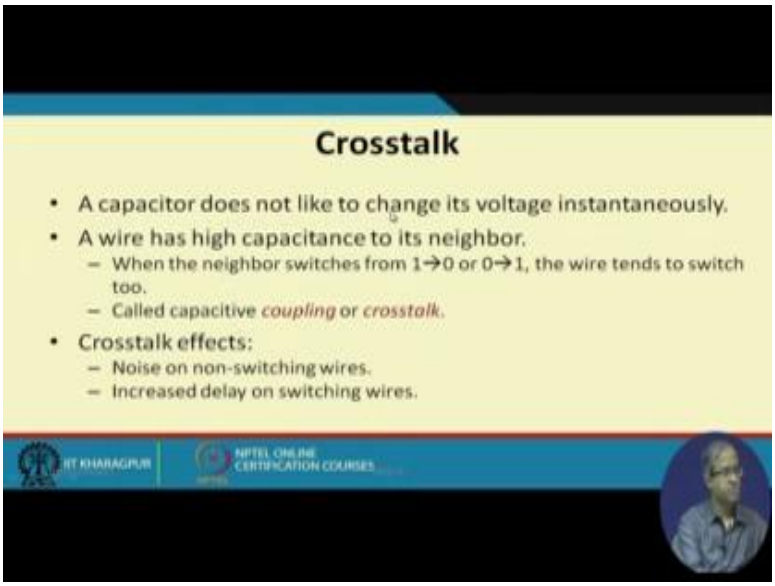

Next let us come to the issues for crosstalk. Now a capacitor holds the charge and it does not instantaneously change the voltage across it right. So, because the capacitor is holding a charge across its plates, it will take some time for the charge to move and dissipate. So, instantaneously you cannot say that the voltage will go from v to 0, it takes time that is why there is a decaying and charging discharging takes place.

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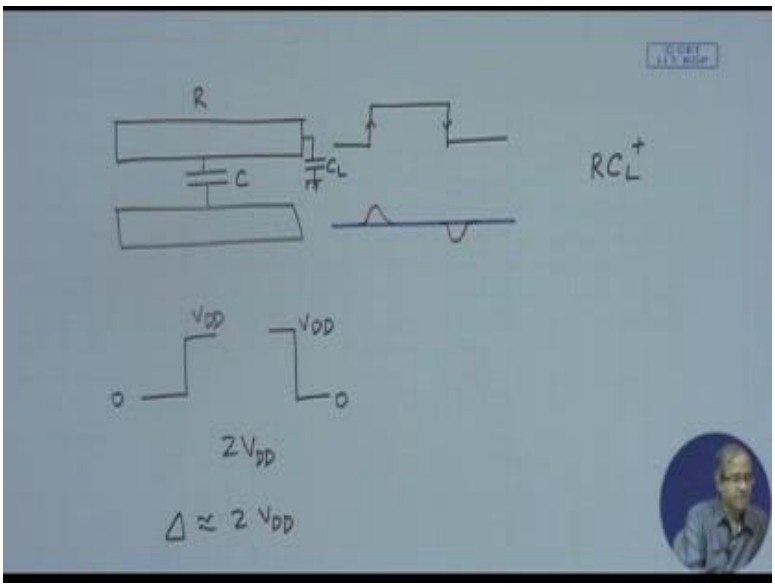

So, now if I if there is any issue like this there are 2 parallel wires which has high capacitance; like say let us try to show here there is a wire like this there is another wire

like this. So, between these 2 wires there is a high capacitance let us say. So, if on one of the wire there is a signal transition either from 0 to 1 or from 1 to 0. So, the other wire maybe carrying something let us say it was carrying a constant voltage signal, let us say it was carrying a constant voltage signal. But because of this capacitive effect what will happen is that. So, whenever there is a sudden rise in the other line, so here also there will be a disturbance like this, again here there will be a disturbance like this. This is called what is called the cross stock affect between lines right, this is capacitive coupling or crosstalk.

Now, this crosstalk results in what? Noise on non switching wires like the example I have said, this second wire was not changing state it was not switching, the first one was changing. So, some noise is induced on the non switching wire and secondly there can be increased delay on the switching wire why? Normally this interconnection wire was facing some capacitive load, so if this is C L and this resistance is R. So, there was the RC delay proportional to RC L, but now because of the C also coming into the picture, this C L value will be increasing. So, the RC value also will be increasing that is why the delay on the signal line will also increase.

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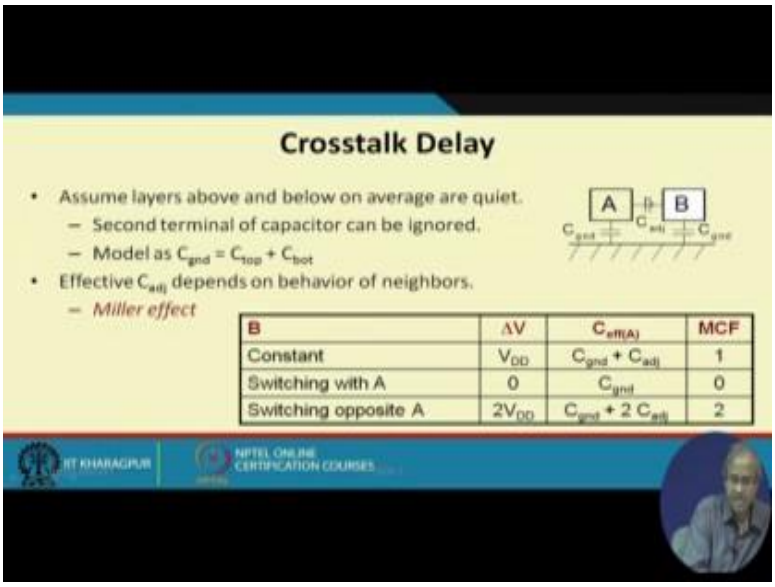

Now, let us look at it in a slightly more detail way, let us say these 2 wires which I have shown A and B. So, the capacitance between them is shown like this here like just like in the diagram I have shown, this is referred to as C adjacent and both these wires are

running on some layer all right and there is substrate below it, and substrate is typically connected to ground or some fixed potential. So, you can say that there is also a capacitance of this wire to this substrate. So, let us call it C ground and C ground. Let us say the value was same. So, the equivalent model looks like this, and this C ground whatever we are talking about although we are showing it as a single capacitance, but actually it will be the sum of the capacitance to its top layer and bottom layer taken together, pertain and equivalent circuit I am showing them as one.

Now, there is rule or a postulate by Miller it is called Miller effect, it says that the effective value of the capacitance between 2 wires it depends on their behavior. So, you cannot statically say that the capacitance between 2 wires is this, depending on how they are switching. There can be 3 situations you can say, if they are not switching at all no no induced (Refer Time: 20:51) no problem, but the problem comes whenever there is a switching. Now there are 3 situations, one is the first wire is switching say from 0 to 1 or 1 to 0, second wire is not switching just like the example I took.

Next case both the wires are switching and in the same direction 0 to 1 or both 1 to 0. Third cases both are switching, but in the reverse direction, first one is switching from 1 to 0, second one is switching from 0 to 1 reverse direction. So, these 3 cases are shown here where means I am looking at the affect on a now on the other line means this is actually changing. So, there is a transition on line A, now what B is happening is like in the first case B was constant, and in A there was a change in voltage equal to delta V let us say, let us say delta is V DD from 0 to V DD it was changing. So, the effective capacitance will be C ground plus C adjacent, because one of them was at ground and the other one is changing ok.

Second case is that both are switching together. So, delta V means change in voltage across this point 0. So, across this capacitive plate there is no voltage. So, C adjacent will not come in to the picture only the capacitance to ground, only C ground will come into the picture. But if they are switching in the opposite direction, so one of them is going from 0 to 1 and the other is going from 1 to 0, then the difference in voltages can be twice 2 V DD right? This is going from 0 to V DD; this is going from V DD to 0. So, delta the change can be twice V DD, because this is changing plus V DD this is changing minus V DD right. So, here the effect of the adjacent capacitance will get doubled.

So, the effective capacitance that will be expressed by A will be this, and the third column is actually referred to as Miller coefficient factor, because of Miller effect. So, when both are switching together the effect is the least. So, we denote it by a relative value 0; that means, this is the best situation. So, when one of them is constant and other is switching the effect is more represented at 1, but it is most severe when they are switching in the opposite direction we represent it by 2.

So, usually when we analyze a circuit with respect to crosstalk, we can designate the different situations by different MCF values, so that you can identify that which MCF value is more crucial and needs means immediate attention.

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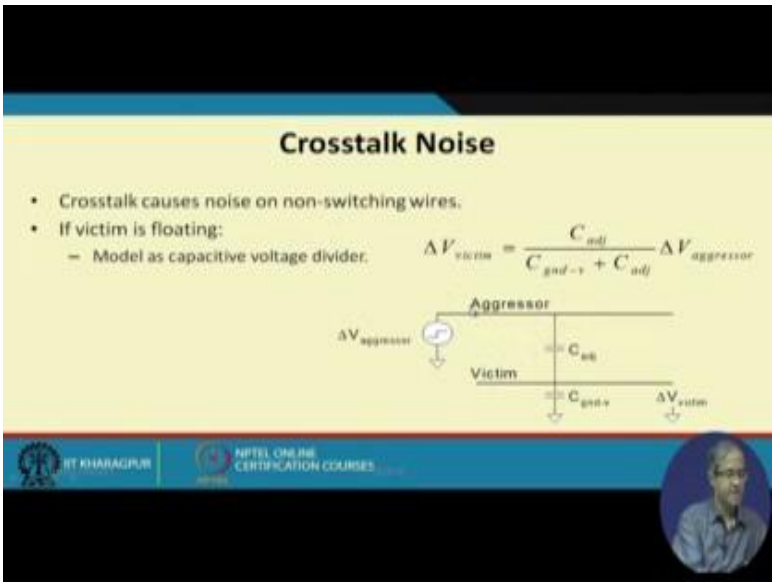

So, let us look at some more crosstalk noise means these equations and formulations, see this 2 wires change on one of the wire is effecting voltage on the other wire, they are typically called aggressor and victim. So, aggressor is the wire on which signal transition is occurring and victim is the wire on which the noise is getting coupled. So, just as a follow up to the previous diagram, between the 2 wires the capacitance was C adjacent, this is C adjacent, the victim is experiencing another capacitance to ground that is C g and d that is it.

Now, suppose the aggressor changes the voltage by an amount delta V aggressor. So, how much will be the corresponding change in the victim volt here the voltage here? So, it is a simple capacitor equation if you do a simple circuit analysis, you can easily see

that the change in voltage here will be they are 2 capacitances in series; that means, it will be like a parallel connection like this, C adjacent divide by C g ground plus C adjacent multiplied by this. So, larger the value of C adjacent more will be the effect of this, but if C adjacent is very small, then delta V aggress then this delta V victim will also become small right.

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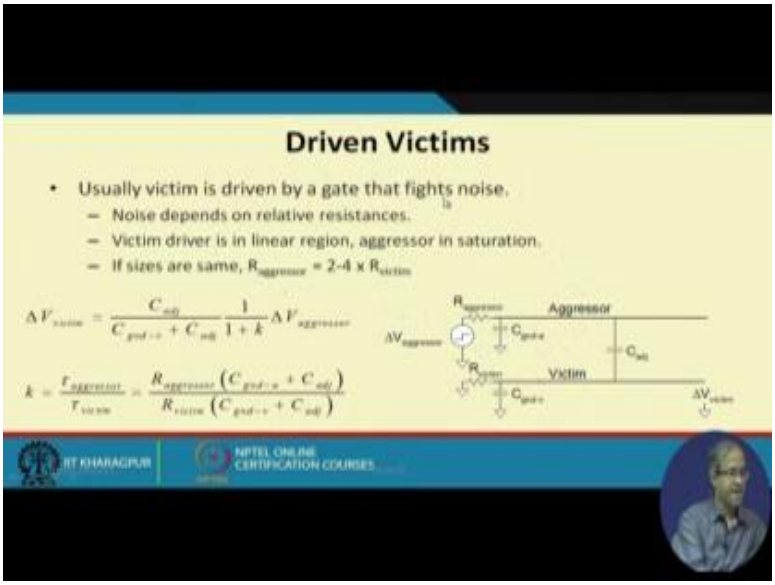

So, the other example let us take another case. So, here victim is driven by a gate that is driving noise fighting; that means, in the previous case I am assuming that the victim is a line which is floating. So, there are no gates whose output is driving this gate, but here I am assuming that let us say there is an inverter whose output of this is connected to the victim, and the inverter in the earlier case we said that we can model it by an equivalent load resistance like this R victim.

So, now, your equivalent circuit looks like this there is also R victim here. So, if you again make a calculation on this circuit analysis on this circuit. So, I means you can get an equation like this, the change in voltage in the victim will be this term is same, C adjacent by C ground plus C adjacent, delta the aggressor was there now this new factor has come in, 1 by 1 plus k where k is tau aggressor the tau victim; that means, the R c delay of the aggressor R aggressor into this total capacitance plus this R of the victim.

So, if this k is close to 0, then it becomes same as the victim floating, but as k increases you can say the value will change. This value will become less. So, actually this inverter

is trying to fight against this cross talk it is bringing the cross talk noise down because earlier when the wire was floating the value was higher, but now since it is fighting this k if it is greater than 0, the value will become less the denominator will be higher, all right.

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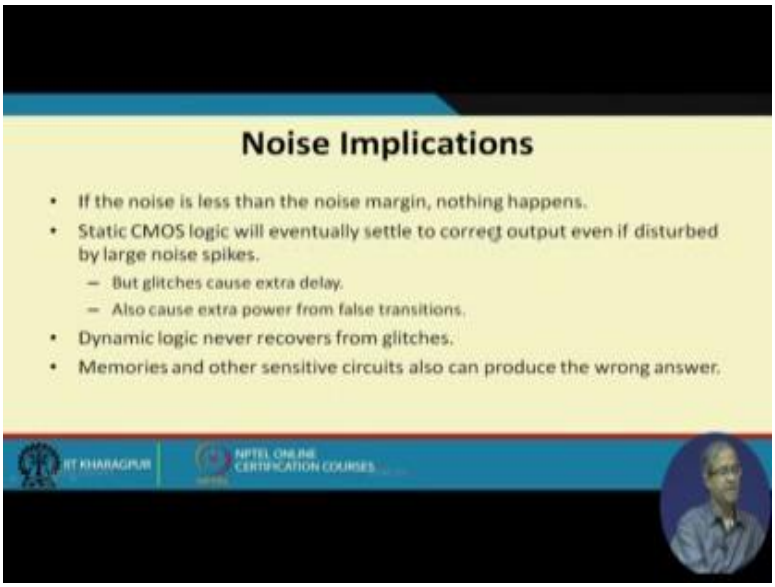

So, some simple noise implication says that if the noise is less than the noise margin, which your circuit is suppose to tolerate then you should not worry about it. And if it is a static CMOS logic then even if there is a noise then some spike. So, it will eventually settle down, the problem will come if you are using dynamic cmos logic like pre charge logic or something like that then this spikes might be discharging some of the voltages which otherwise is important. But because of these glitches and this noise delay might increase and similarly memories d ram the dynamic ram where data are stored as capacitance as charge on capacitance, because of this noise some of the capacitances might get discharged. So, the answer might be wrong.

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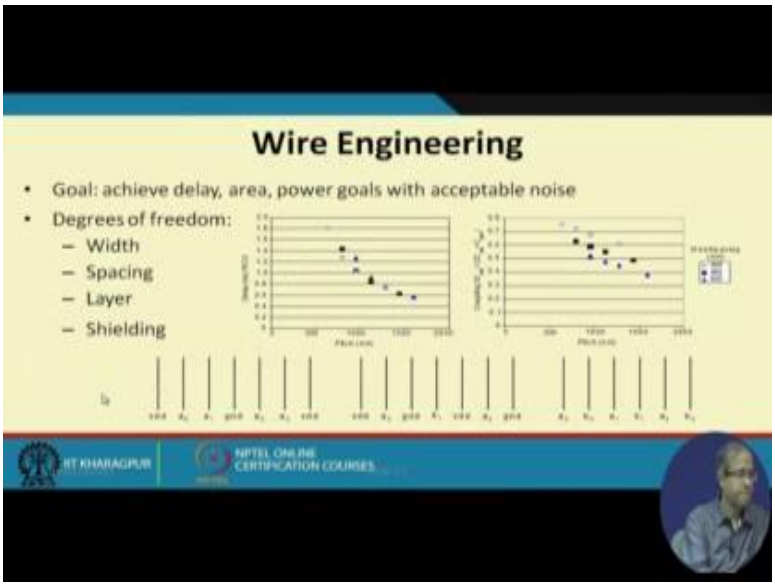

So, one last thing; that means, you can talk about something called wire engineering; like how do I control this capacitive affects then this noise. See there are a few things that can do play with width of the line, spacing of the line, so, on which layer you are drawing it as you have seen depending on the layer the capacitive and resistive effects will be different and something called shielding.

Shielding is important, shielding says that well I have seen I have shown several examples this case is no shielding a 0, b 0, a 1, b 1, a 2, b 2 are 6 lines which are laid parallel to each other side by side, but here let us say a 0, a 1, a 2, I am showing 3 of them V DD ground V DD ground. So, they are interspaced between power supply lines. So, there is some kind of a shielding. So, the noise on these lines will not propagate to the next signal line because of the shielding. So, if you want you can keep more than one lines between these shields V DD then 2 a 0 a 1 then ground then a 2 a 3 then V DD and so on. So, these are some of the techniques which are usually used.

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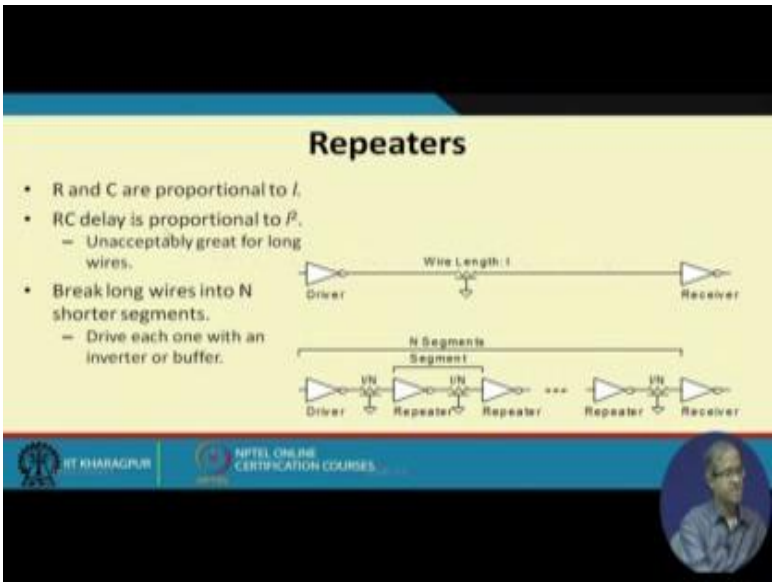

Repeaters already I have said, so I am not elaborating on this anymore. So, we have seen that the delay of a wire is proportional to the length. So, this R is proportional to length C is also proportional to the length. So, R C delay becomes proportional to l square. So, what you do we break up a long length of length L into N segments L by N, L by N, L by N this we have already seen.

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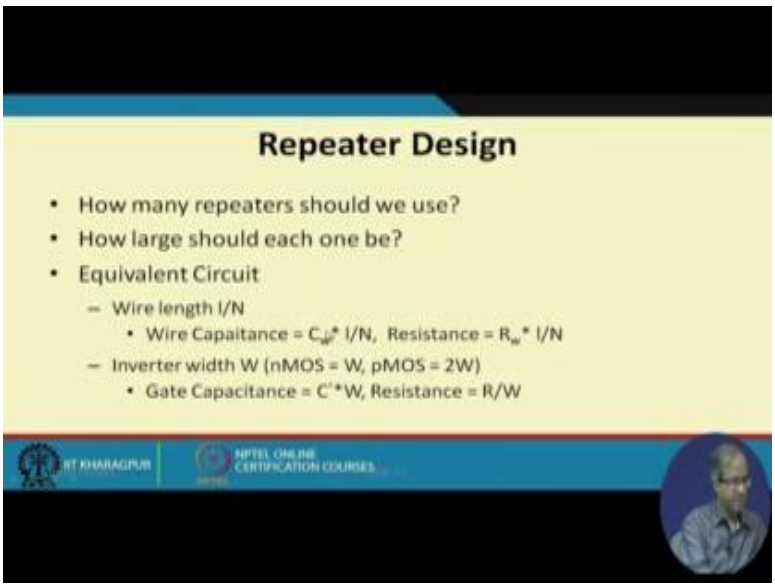

So, for repeated design, if we divide it into l by N; so, each of the segment will be of length l by N. So, wire capacitance will be the capacitance of a basic square into l by N,

resistance will be of a basic square into l by N. So, if the inverter width is W, typically pMOS is larges as said because of the slower mobility of the holds. So, W and 2 W is our typical value usually it is less than 2 W. So, the gate capacitance value will be line this the resistance value will be divided by W and capacitance will increase in proportional W.

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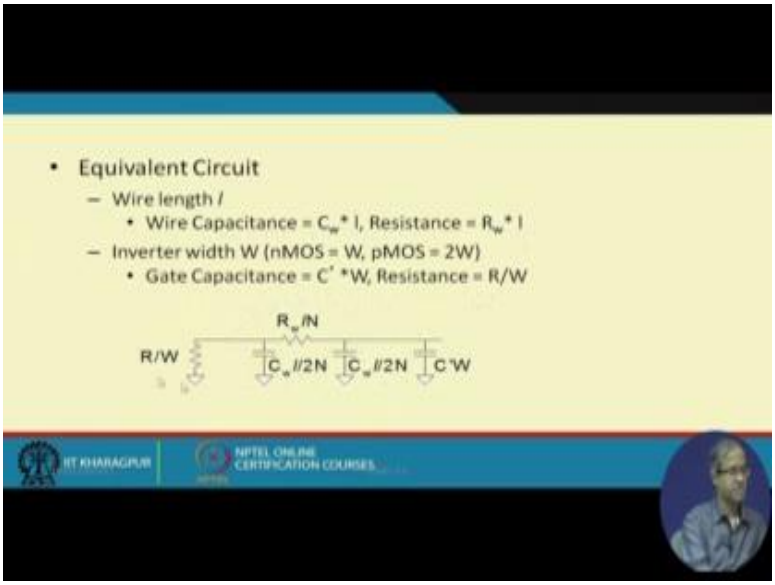

So, in the equivalent circuit for the whole wire the wire capacitance will be C w into the whole length, resistance will be R w into the whole length so the equivalent circuit will look like this. So, in the driving circuit it will be R by W the inverter, the load capacity will load C W and here for the R C delay for each segment it will be R w by N this will be C w l by 2 N, C w l by 2 N.

So, with this we come to the end of our discussion on interconnect modeling, in our next lecture we shall be looking at some related issues; so how this spacing and the width of the lines are determined. So, it is something which I have called design rules.

Thank you.