VLSI Physical Design
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Lecture – 31
Power and Ground Routing

So, we mentioned earlier that with respect to routing nets on a VLSI chip, clock and the power nets have very distinct characteristics. For clock the main requirement is balancing skew, the clock signals which are arriving at multiple points must arrive almost at the same time of course; provided they are related. If they are unrelated I really do not care, right.

So, the clock nets has a large number of terminal points, similar is the case for a ground or power net. So, when you are distributing the VDD and the ground signal across the chips, there is one similarity with clock is that the numbers of terminal points are large in number. If you consider this standard cell kind of layout, so every standard cell that you include in your design, they will be have a power and ground connection. So, you have to feed power and ground to all of them, but there is a difference from clocked outing. In clocked outing the issue was equalization of skew, skew minimization the clock should arrive almost at same time, but in power and ground the requirement is different.

So, there is no signalling, I am applying a constant voltage on the VDD and ground lines. So, I should as ensure that whatever current is drawn by the circuits which I am driving, my power lines or tracks should be wide enough to drive the required power. If I need higher power I make the tracks wider, if I do not need that high power I can make it narrower and again just like clock in power (Refer Time: 02:37) power (Refer Time: 02:39) also will not want, frequently to move from one layer to the other. So, wherever wire connections are essential you only use those rest you do not use and again most of the connections has to be on the same layer in a planner fashion, because as we switch across layers your delays on other parasitics is will go up, noise will increase on the power supply line you will be getting some noise also such things you can minimise.

So, in this lecture we talk about power and ground routing.

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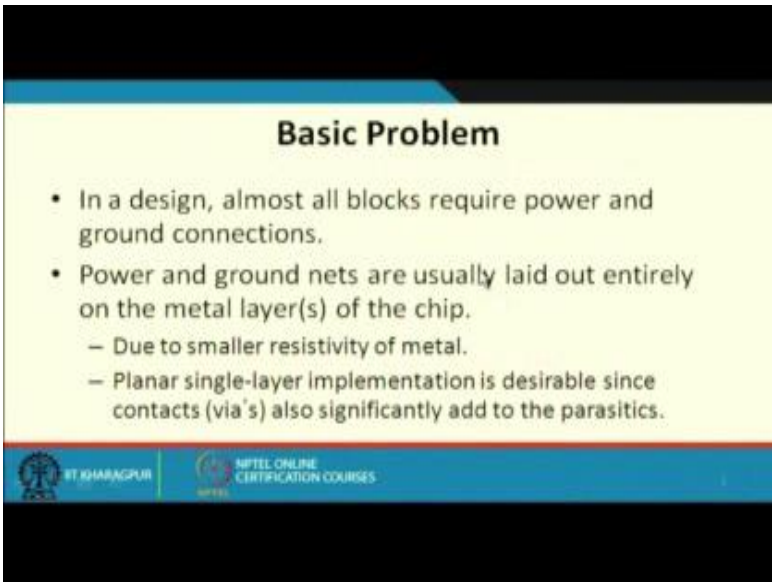

So, the basic problem I have already talked about; so almost all the blocks in a design that you want to layout on a VLSI chip, will be requiring the power and ground connections. So, the power and ground pins are only present across the chip there everywhere, and because of the reasons I just now talked about they are typically laid on the same layer and on the metal layer not on the other layers why? Because the resistivity of metal layer is very good, it is resistance is less so that signal degradation other things will be much less, it can also carry larger currents that is why all power net works are laid out on metal layer. Resistivity smaller and whatever possible we go for planar single layer implementation, we will try to minimise wire connection unless it is extremely essential, fine.

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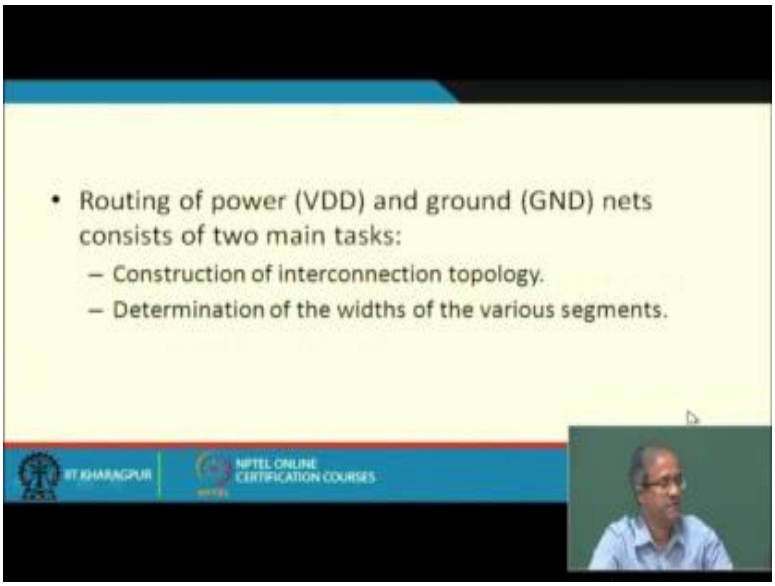

So, just like clock for VDD and power routing also we need two steps. So, in clock you require if you just recall your two steps was first was designing a clock tree, then distributing the clock tree to the actual terminals, but for power and ground routing these two steps are of course, the first step is similar you try to construct some kind of a topology, that will make connections to all the points were you need the power lines; second depending on the blocks where you are driving, and their current requirements you determine the appropriate widths of the various segments of the wires, this is very important for power outing.

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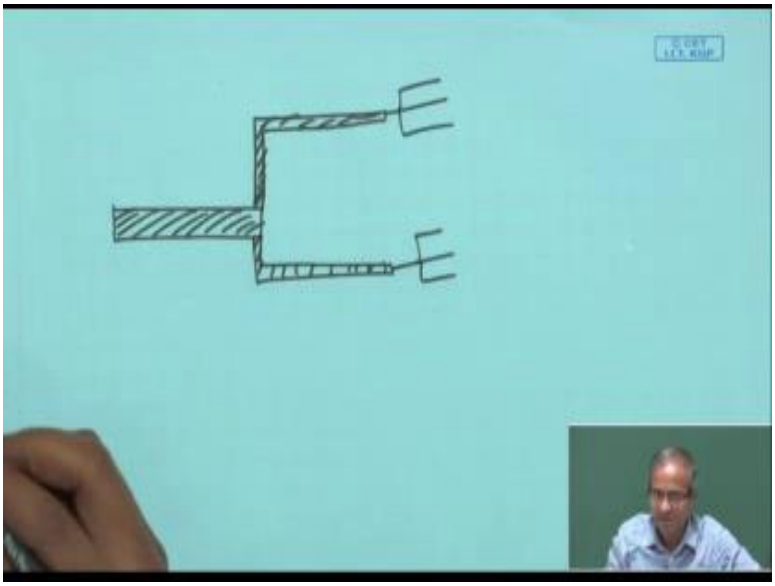

Like for example as I said you can say that for the power, your line may look like this start with a very thick line, from there you feed your power to two different lines this will be thinner, something like this. From there you feed to three different points, this will even thinner. So, the width of the lines will vary depending on the total current driving requirements right. So, it will look something like this.

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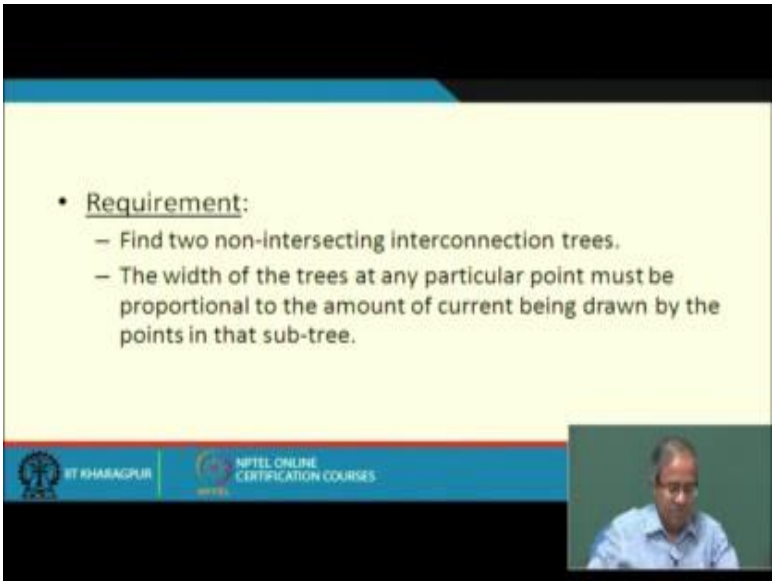

So, for power and ground routing one for power and other for ground, you need two interconnection tree; obviously, there will be inter non intersecting; because one for VDD and one for ground and as I just now said the widths of the trees at any particular branch must be proportional to the total current that it is expected to draw. So, from the root of the tree the widths will be wider, but as you moves towards the leaf, the wires will become thinner and thinner.

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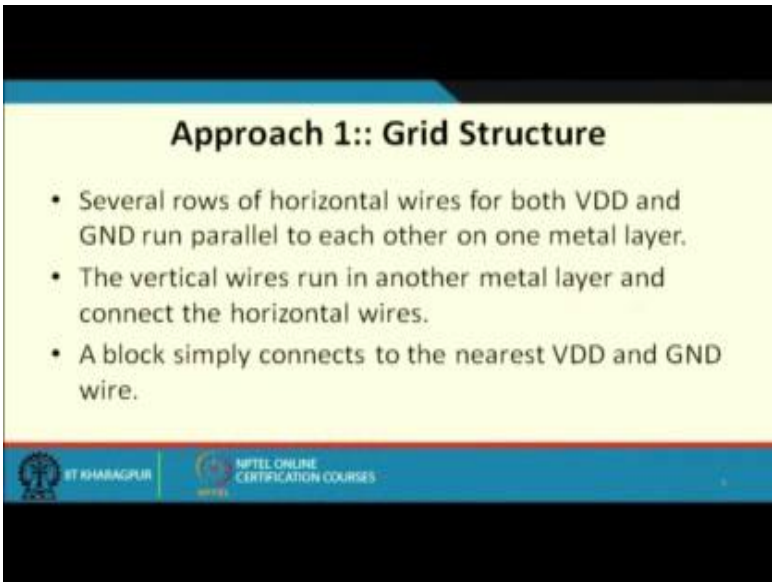

So, we talk about broadly two approaches; the first approach is referred to as a grid structure. So, what does grid structure says? It says that several rows of horizontal wires for both VDD and ground run parallel to each other on metal layer. The vertical wires run in another layer and connect the horizontal wires; block connects to the nearest VDD and ground. See this grid structure is very suitable for standard cell kind of designs; just let us recall this standard cell design so that you can appreciate why you need this.

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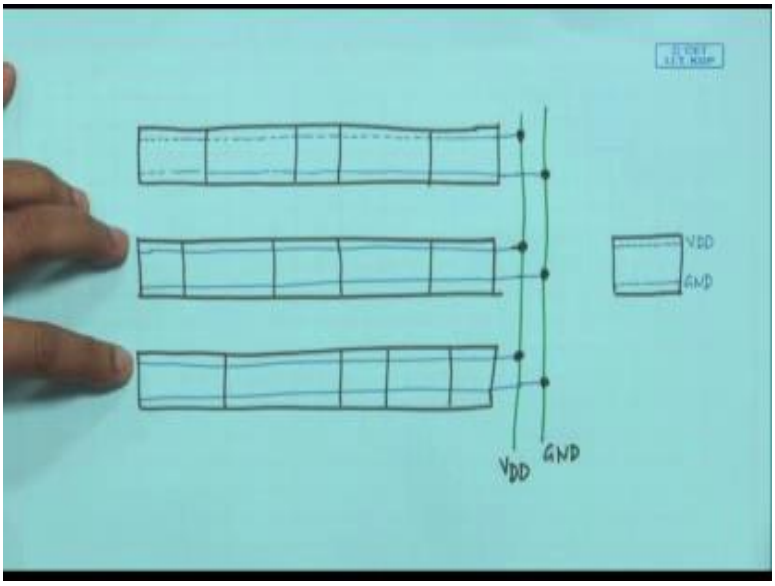

So, I am showing some rows of this standard cell in a typical design. So, I am showing 3 standard cell rows right. Now you recall I mentioned that whenever you place a particular standard cell, the cell has a particular property that its VDD runs somewhere in the top, ground line runs somewhere in the bottom and their relative positions across all the cells are the same. So, what does that mean? Suppose you place some cells across the rows. So, here also you place some cells, here also you place some cells. Now this VDD and ground lines you see since the placed side by side, they will be touching one another. So, for the horizontal routing across the cells it is already done. So, you do not have to do anything. So, it is like continues line. So, this VDD and ground lines are already connected horizontally. So, if you take them out these are all running on metal layers, right.

So, what you can do? You can use another layer. So, I am showing it in a different colour both will be metal layers of course, and this will be wire connection; here you cannot avoid the wire connections. This will be your VDD connection; this will be your ground connection. So, on one layer you will be running the VDD and ground connection say vertically and in another metal layer. So, all of the metal layers across the cells they will be running horizontally, they will be connecting wire connection to the vertical lines and you can see that the layout will be very regular in case of standard cell design, it will look something like this, right.

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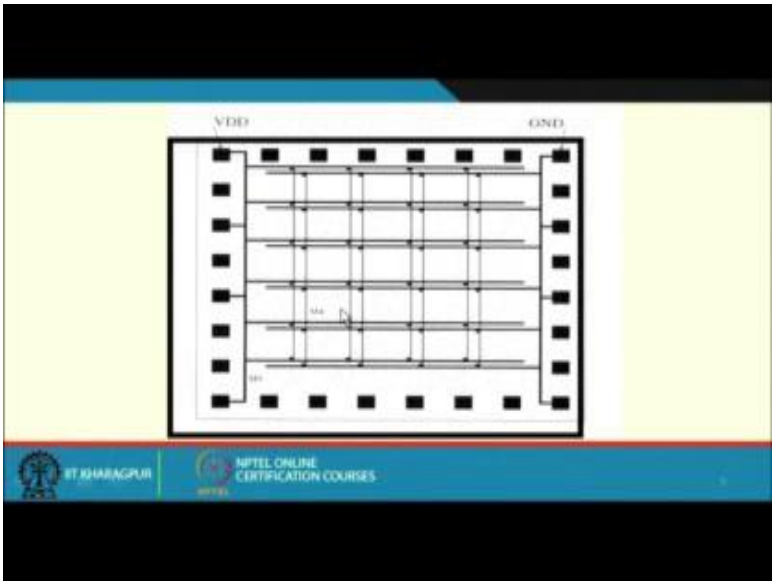

So, let us proceed. So, here I have shown something like this, see this are the two parallel VDD and ground I am showing here I am shown in the diagram that they are coming from one place, but you can do it like this also instead of; see here since I have try to connect them from one side, so I needed another layer and I need wire connection, but what if suppose I feed VDD from one side and ground from the other side, then do I did do I need connection like this see, then I do not need this separate layer. So, I can do it on a single layer like it is shown in this diagram.

You see that the VDD connections they are all connected to this left vertical layer, and the ground connection are connected to this vertical layer and the horizontal connections are typically on the in 4 metal; in 4 or in 5 whatever and in some places if you required you can also add some additional vertical connection, such that the impedances across the different power supply points they can be less, but this is optional again the way or out, but the basic concept I told you that you can feed it like this and as you can see that in the points on the left the wires are shown to be thicker, but as we drive to the cells it has become thinner. So, there is a wire sizing (Refer Time: 12:20). So, talking about the grid like structure, so I am showing you another kind of a similar approach.

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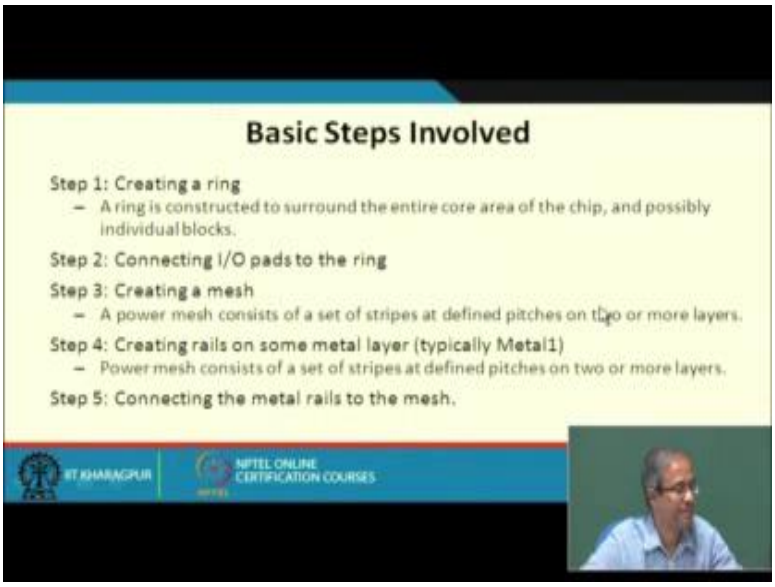

So, which is used in a slightly more general context not necessary for standard cell, that you can create a ring which surrounds the entire core of the chip like this, like the one on

the this whole surrounding thing is called the ring, you define a ring around a chip then you connect the I O pads to the ring.

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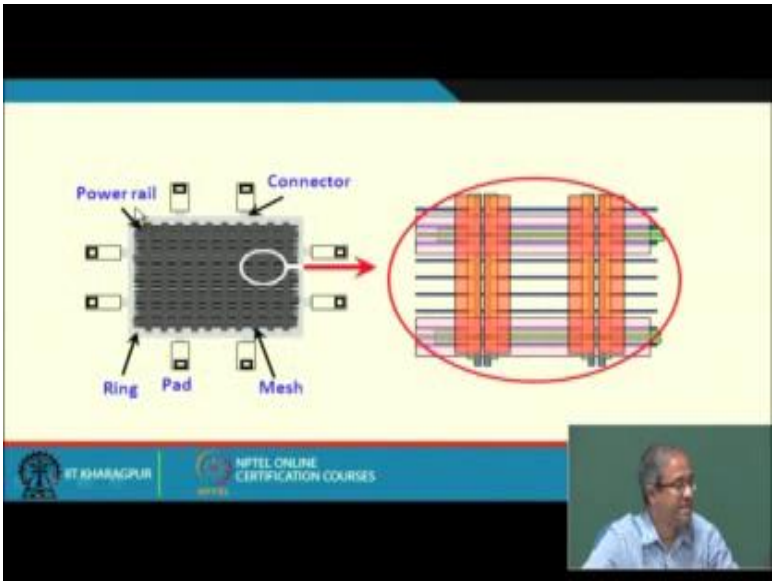

So, all the I O pads they are connected to the ring; the I O pads will be feeding the VDD or ground connections, they are all connected to the ring then create a mesh. So, inside the chip you create a power mesh just like a clock mesh, consisting of a set of stripes. Pitch means gap defined gaps on two or more layers. So, here so each of these this are stripes, you create such metal stripes on more than two or more layers, so that metal connections will be available power connections on more than one layers also; because in some cases you need this connections to be made available on more than one layer as well.

So, the mesh is created accordingly rails, the vertical lines that was shown these are created on some metal layers and the metal layers are connected to the mesh; something like this you create a mesh of power lines and also ground lines similarly, and they will be available on one or more metal layers, so that on the blocks wherever you need them, you can take it from one of this layers, right.

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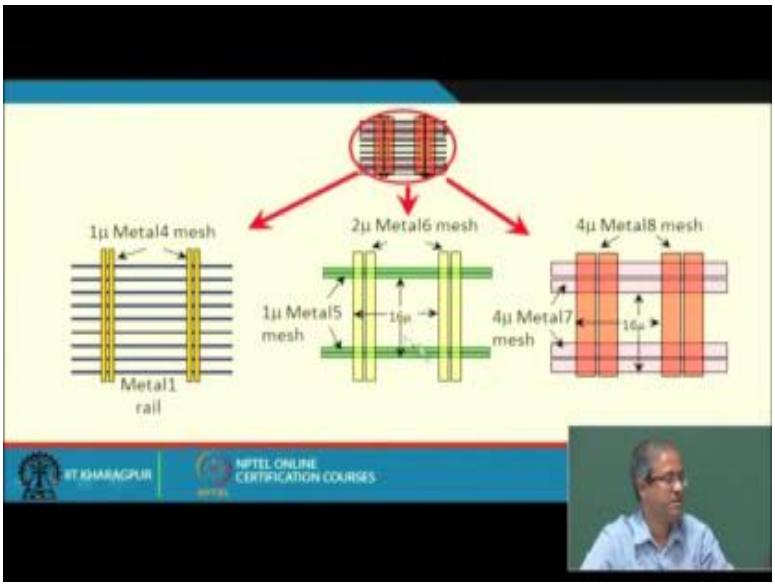

So, the idea was something like this and some of the designs which you are done. So, some of the metal layers they are separated like this block I am showing. So, metal 4, metal 6 metal 8 so many metallization. So, depending on which layer your using the kind of connection there width, their separation everything will be different. Now one thing is true for VLSI fabrications as you move up and up in the layers, the width of your lines become thicker and thicker wider and wider. So, it is better to layout the power lines on one of the top layers, because they will be they will be thicker in any case they can carry more currents. So, just the basic idea I told you.

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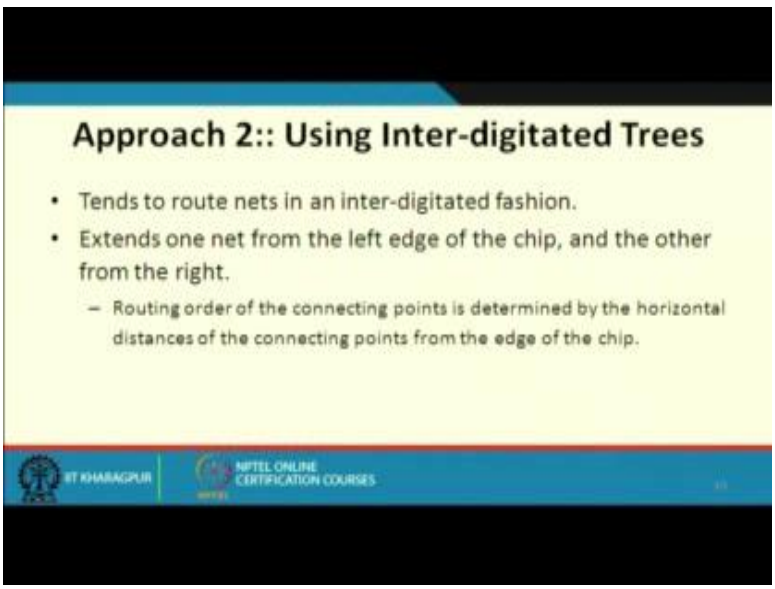

So, this second approach says that will we do not here we apply it for a full custom kind of design.

So, we do not assume that I have already pre laid out vertical and horizontal connection; from there I simply take the power and ground. Here I am saying depending on the requirements like I may have a scenario like this, that I have a block this is this is a full custom.

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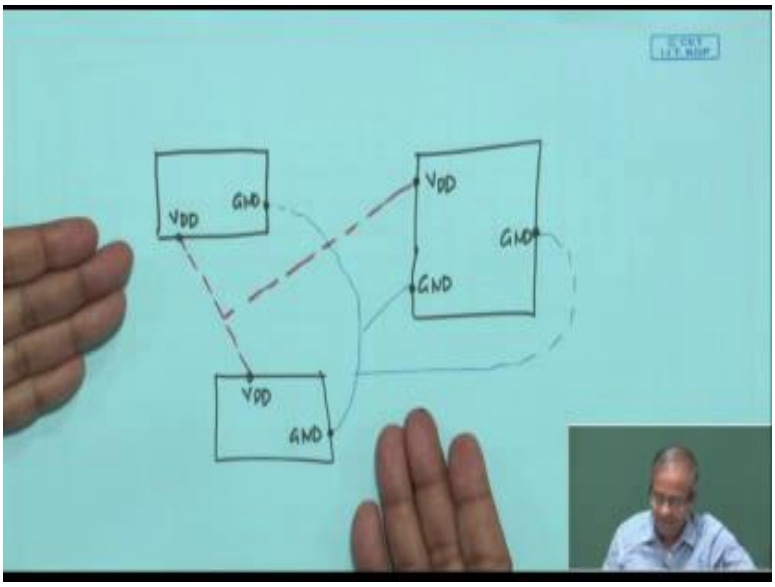

So, here I require a VDD connection here, I require a ground connection here let us say. Suppose I have another block here like this, so I require VDD connection here, I require a ground connection here; so I also require a ground connection here let see. Similarly I can have another block here VDD here ground here something like this. So, now, the requirement is that let us construct a tree depending on my actual problem at hand. So, where are the VDD next? This are the 3 point I have to connect for VDD and these are the 4 points I have to connect for ground. So, for these two let us try and construct two trees, that will move from two opposite direction these are called inter digit trees and if you able do this in a systematic way, you will be getting a layout of the power and ground lines on the same layer; and once you do it then you can consider the sizing you can analyze the current requirements for the different blocks, you can appropriately said the width of the different wires right. So, I mean one of the net VDD and ground one of

them starts from the left edge of the chip, and the other starts from right edge of the chip and show some examples.

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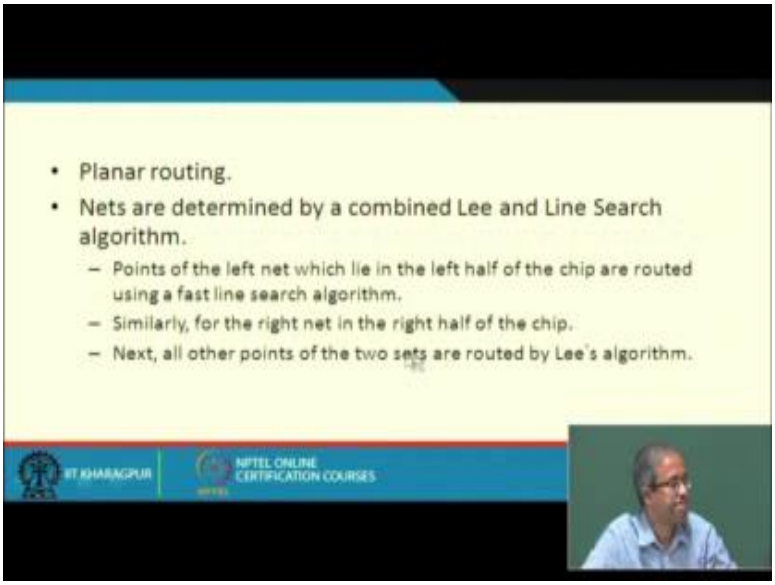

So, the routing that you get is planner, in the sense that you can do it on the same layer and sometimes to get the path you can use either lees or line search kind of algorithms or a combination of them. So, this charting is that you see VDD you start from left ground we start from right; let us say let us do the VDD first. So, initially there are few blocks most of the routing areas are available for me. So, initially let me use the lee not lees the first algorithm, the line search let say height hours algorithm are used. So, I will quickly get some paths, so how to connect the VDD nets. So, once I have connected the VDD nets, some of the line are already laid end they are blocked; from other side now comes the ground net. So, there sometimes the line such algorithm may find difficulty in finding a path, because some of the paths may be blocked.

So, here you can use a line such algorithm to find complex path if it is available because if you recall the lees algorithm will always find the path. So, for the ground net when required you can use the lees algorithm, that you will guarantee you a path if it exist at all right.

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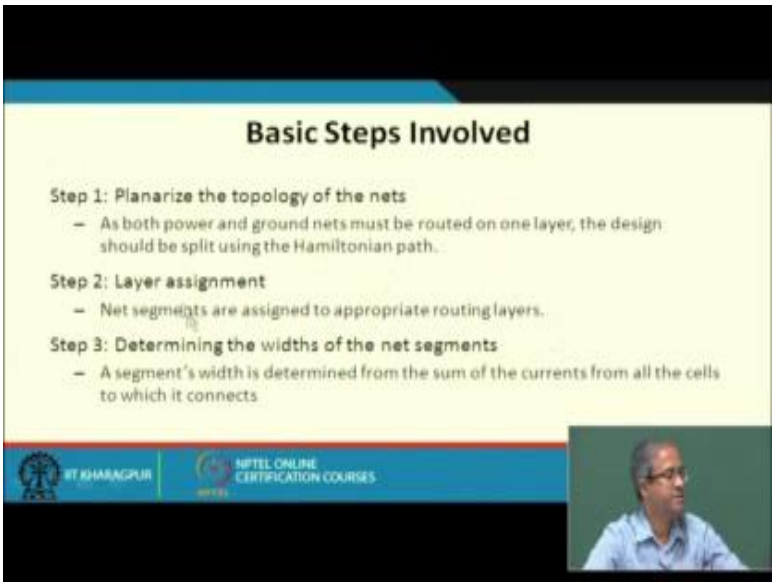

So, this is the basic strategy. So, this steps involved as follows you planarize the topology of the net, layer assignment you just assign them to one or more metal layers and as I had said depending on the current requirements, you said the width of the different nets segments.

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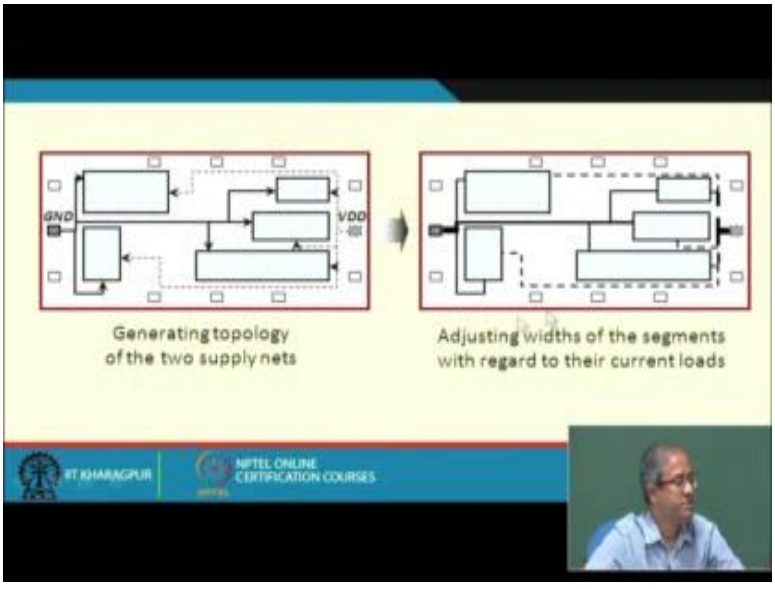

So, let us take a simple example say ground we are routing from the left and VDD from the right. So, this there are five blocks with some ground and VDD requirements. So, the ground is been routed like this you can see and VDD from rout VDD shown by the

dotted line and once you have done this, you can fix the thickness of this lines the thickness width of this lines can be set accordingly right.

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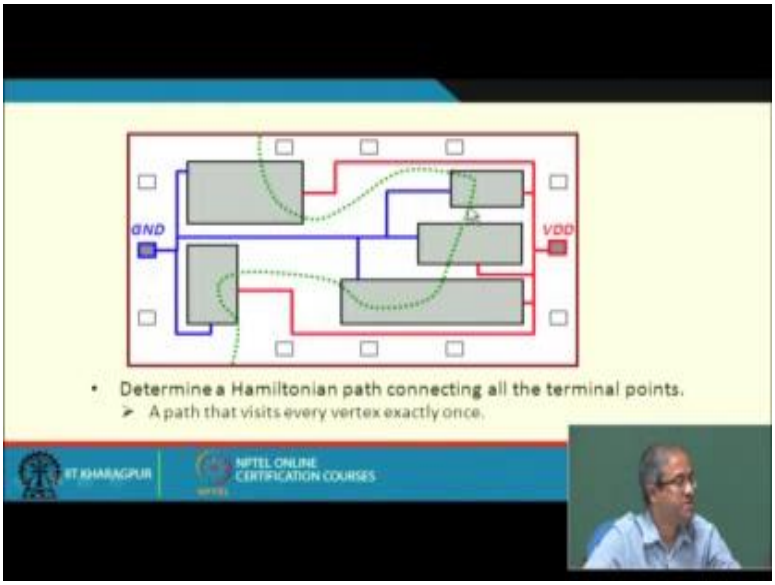

So, let us take another example; the same example in fact, this same example I am showing that whenever you rout a net let say the ground net. So, what was the requirement? There are some ground pins that are available in this 5 blocks, you required a connection. Similarly for the net for VDD, they also needed to connect this 5 blocks. So, what we actually need, something call a Hamiltonian path in graph theory. So, in graphs Hamiltonian path is defined to be a path, a path is what a sequence of edges. Hamiltonian path means you start with a vertex go on traversing the edges in such a way that a vertex is traversed only once, you do not cross a vertex twice.

So, once you get a Hamiltonian path you have one way of routing the power or the ground lines. So, here, once you got a Hamiltonian path, you embed some horizontal and vertical segments corresponding to this Hamiltonian path. So, the blue one corresponds to the ground line, and the red one corresponds to the VDD line. So, here as you can see that it is possible to put all of them together on the same layer. So, although they are shown on different colours, but there are not intersecting anywhere; there are two trees which are like a comp they are called inter digitated trees they are not intersecting, but they are setting side by side right. So, here there is another example where you can see VDD from this side ground from this side.

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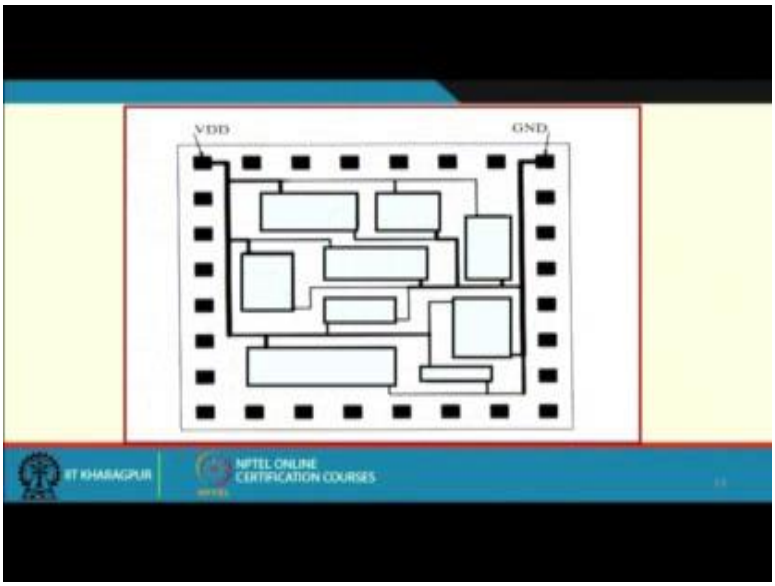

So, there VDD net you can see and ground net is coming from the other side. So, in the same way they get routed. So, the idea is this. So, you see that when we talk about VDD and ground routing, there are some other issues like routability trying to complete the routing on the same layer as possible and then sizing of the different segments of the wires.

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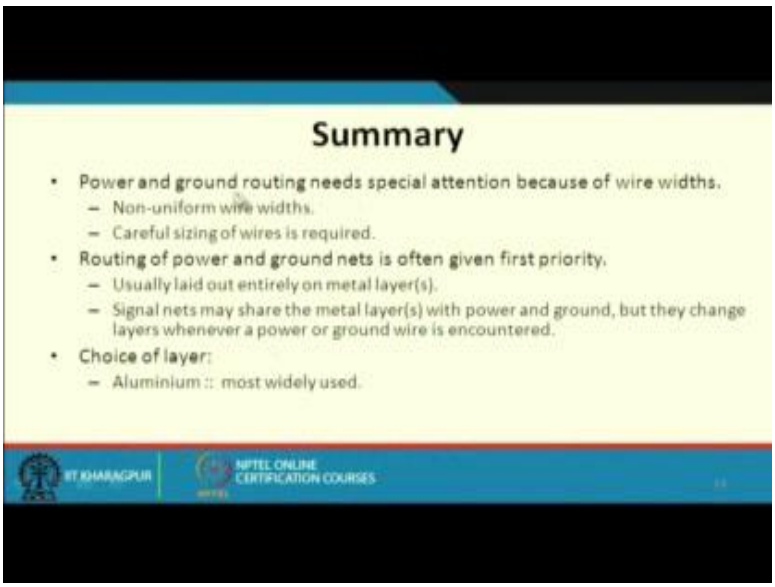

So, to summarize here for power and ground routing, we need special attentions with respect to the wire widths, because if the power supply wires are not width enough then

you will be trying to draw more current through the wires, which are not design to handle those high currents and there may be some physical break down in the wires. So, you have a routing algorithm where wire widths can be non uniform this is unlike clocks or signal nets where wire width are all same, we are not changing the width of the wires, but in power supply routing we are changing the width of the wires depending on our requirements.

So, the sizing of the wires is required, at usually in a routing problem the power and ground nets are first routed followed by all other nets and as I said they are typically laid out entirely on metal layers because of the low resistivity; and the signal nets like the channel routing that I talked about you just understand one thing, you think of on the channel routing like you again look at say means couple of standard cell rows with channel in between.

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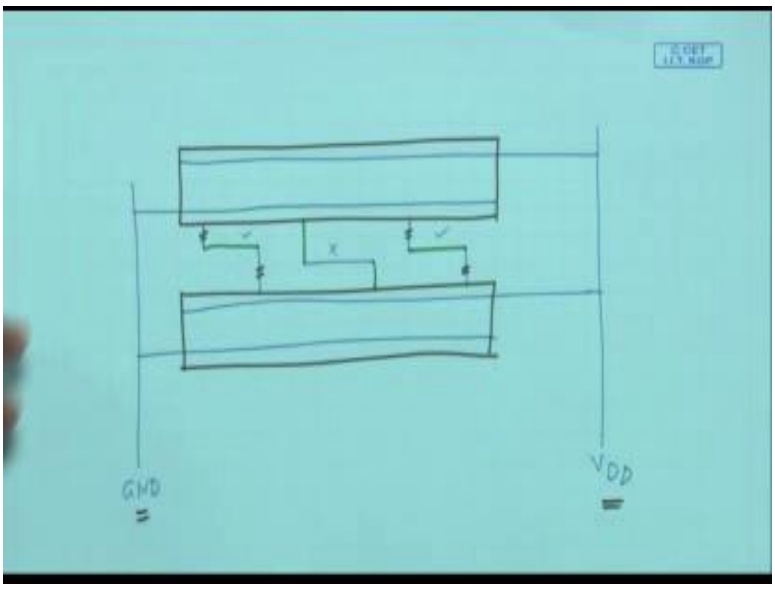

So, what you said is that the VDD connections across all the cells can be connected like this, this can feed VDD. The ground lines out here they can be connected like this, but the channels which is in between you see here also you need two layers, like you can have some connections like this right this is a the (Refer Time: 25:17) model I am seeing, but if you do not want to cross then you will be just using blue on the vertical segments, and green on the horizontal segments only in that case you will not be using this, you can use this and this.

Now what I am saying is that just if you see here what you have done; so, we are using the blue metal some metal layer for routing our VDD and ground connection, but during the channel routing also we are reusing that metal layer wherever you can. Because within the channel we are not routing VDD and ground, so the channel area is available for that, but if you are using over the cell routing we have we cannot use the blue line because already blue is used here, we will have to use some other layer right.

So, here we are saying that this signal nets within the channels may share the metal layers with power and ground, but if there is a power layer in case of standard cell not in standard cell, but for the full custom design they will have to change layers because power and ground will always have higher priority and you do not want to use wire connection on power and ground layers and; obviously, choice of layer is the metal layer aluminium, which is most widely used that has the lowest resistivity.

So, with this we come to the end of this lecture. So, in the next week we shall be starting our discussion on the timing analysis, the various ways you can carry out timing analysis static timing analysis, and ways in which you can annotate or modify a design so that they perform better with respect to timing. So, with this we come to the end of this lecture.

Thank you.