VLSI Physical Design
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Lecture - 20
Detailed Routing (Part I)

Here we continue with our discussion on routing which we have been discussing over the last few lectures so if you recall we talked about area or grid routing where we are able to connect arbitrary 2 points on a 2 dimensional grid like structure in the presence of obstacles. We also talked about global routing where once the blocks are placed and this so called channels and the routing regions are defined. So for every net we are trying to find out the approximate sequence of routing regions that needs to be traversed to complete that connection. Now once this is done we take every routing region one at a time and try to complete the exact inter connection patterns to route that particular routing region. It can be a channel or we shall see it can be another kind of a structure called a switch box. This step is called detailed routing and we shall be starting our discussion on this today.

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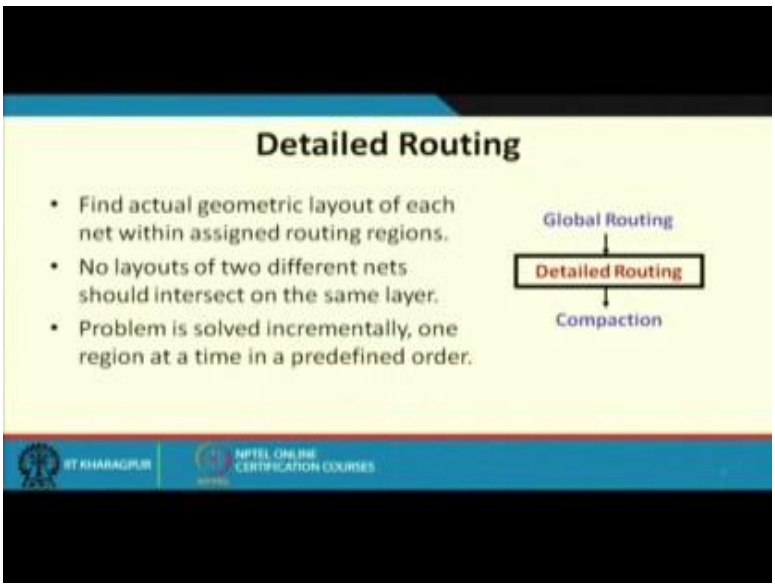

So, topic of the lecture is detailed routing, this is the first part of it. So just exactly what I have said this scope of detailed routing is to determine the actual geometric layout for every interconnection net for the routing regions and typically the routing regions are

handled one at a time. There are some obvious requirements 2 different nets they should not intersect on the same layer as otherwise you can understand there will be a short circuit between the 2 nets. So if there are, if there are 2 different nets they have to be laid out in a disjoint fashion with non-intersecting line segments. So this problem as I said is solved by considering one region at a time in some particular order. So the step of detailed routing will follow global routing and once this is done we can have some other steps like compaction which we shall be seeing later.

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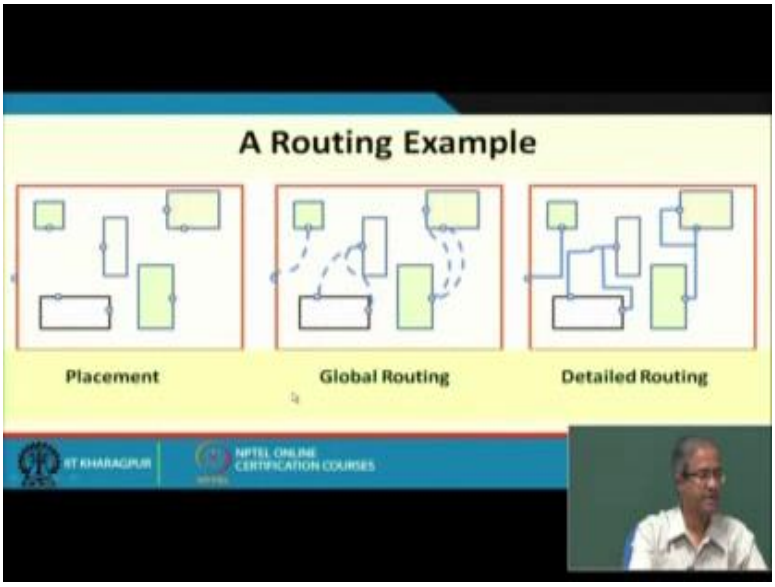

Now, here there is a pictorial demonstration or illustration of what exactly we have talked about. So after a set of blocks that are placed so scenario may look like this, so this rectangular boxes are the blocks and the small circles are the pins that need to be connected. So global routing will give you an approximate route for example, this pin has to be connected to this pin this is the approximate route. This is an approximate route; this is another approximate route like this. So global routing will give you the sequence of routing regions that need to be followed, but once you are in the detailed routing step for each of these nets the exact connection, the geometrical layouts of the wires horizontal and vertical segments typically they have to be finalized or fixed. This is the scope of detailed routing. So once detailed routing is done you can say that well my layout in terms of routing is complete so now, I can move on to the next step alright.

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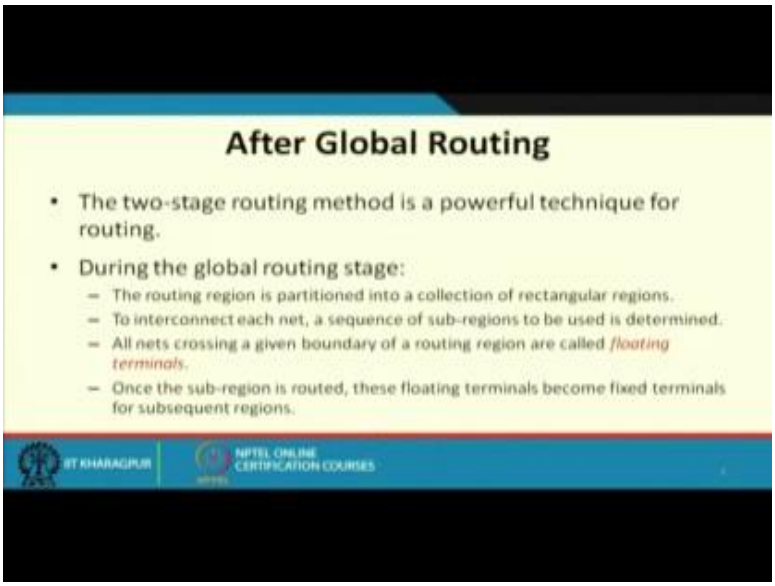

So, this is just a quick recap. So after global routing we consider the problem of detailed routing. Now there are some important concepts to understand I shall try to explain these concepts with the help of some examples. During global routing as I said you recall our earlier lectures the entire routing region or space that is available on the chip that is typically partitioned into a set of rectangular routing regions. We usually call them as r 1, r 2, r 3. Here the difference regions where we can carry out the routing. Now for every net we have to connect the corresponding terminal. So for connecting the terminals we have to determine a sequence of sub regions which are the regions that need to be traversed to connect the points corresponding to this net.

Now, there is a concept of floating terminals this I shall be illustrating very shortly. It says that if a net is crossing the given boundary of a routing region, then there can be something called floating terminals. Floating terminal means they are terminals whose exact location or position is not fixed as yet, but once the routing for that particular routing region is complete this floating terminals will become fixed terminals. Their exact coordinate or location will be finalized or fixed. So this is what is meant so once this sub region is routed the floating points will become fixed terminals. Now I shall be explaining this very shortly.

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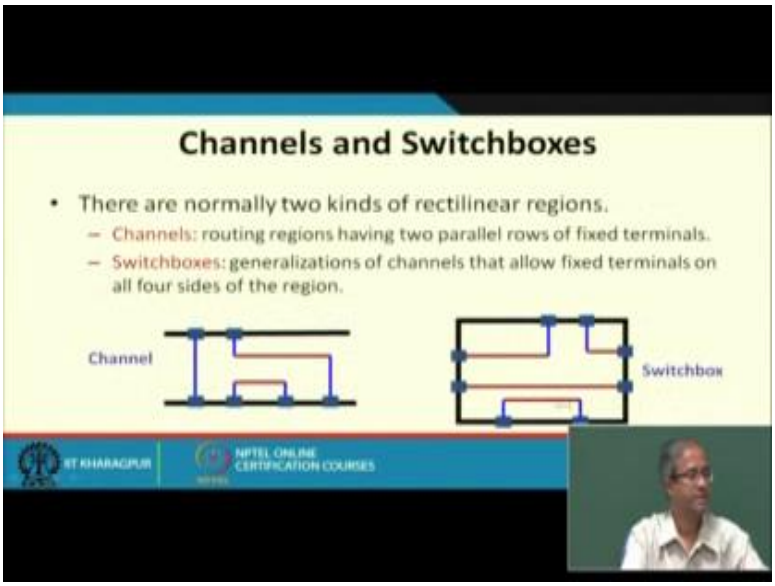

But before that let us talk about the routing regions, now depending on their geometric and the relationship between the consecutive routing regions, the routing regions can be of 2 types. They are called channels or switch boxes. So what is a channel? A channel is like a region where we have 2 parallel edges they can be either horizontal or vertical and there are some pins which are located on the boundary of this parallel edges. And our task is to interconnect some of these fixed points or terminals on this edges. Now this region within the parallel boundary is called as channel. So we shall be looking at a number of channel routing techniques. Well a more complex situation can arise in some cases where this terminal can exist in all 4 sides of a rectangular region. So this is called a switchbox. Switchbox routing is typically more complex than channel routing. And for a switchbox this is just an example. So I have shown some typical interconnections.

Now, one thing you see, that here I have shown the connections by different colors. Colors means these connections are laid out on different metal layers typically. These are all done on metal layers. So this blue and this brown lines they are on 2 different metal layers and their junctions. Junctions will mean there has to be a connection between the 2 layers. These junctions between one horizontal and a vertical layer is called a via connection via or some kind of contact connection between the points in the 2 layers. So wherever the blue and a brown line will meet, it implies that there is a via connection there. So these are channels and switchboxes.

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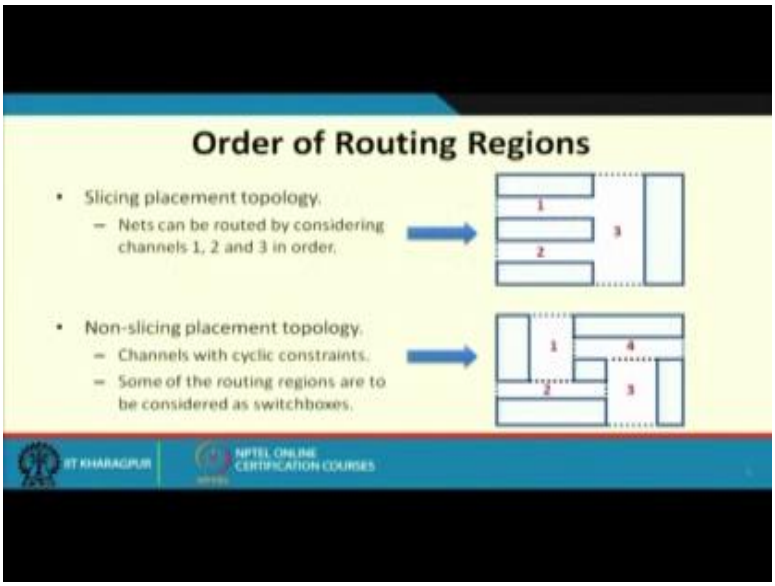

Now let us come to this very important thing. Depending on the relative order of the routing regions, their order of routing can be determined in some particular way. Like you consider this kind of a situation, where there are 3 routing regions 1, 2 and 3 and these are the blocks. So there will be pins along the boundaries. So here what he says is that the nets have to be routed in this order 1 and 2 first and 3 will be only after that. Why it is so? Let me try to explain it with the help of an example.

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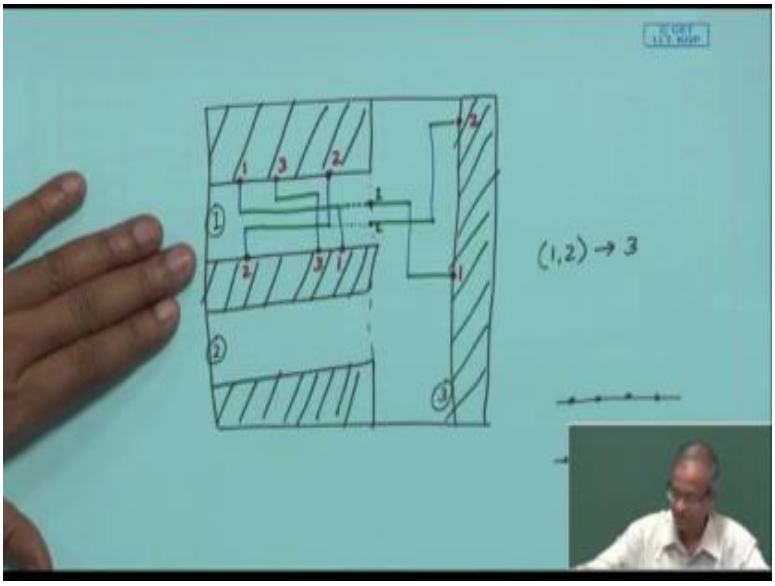

Let us take this same example. Suppose I have this rectangular region where these are the blocks. This is one block, this is one block, this is a block, and this is a block. Now for connection, let us take a specific example. Suppose I have a terminal called point 1 here. I have terminal point connecting 1 here. And also there is a 1 here. So these are the 3 points we have to connect. Similarly let us say there is a point 2 here, there is a point 2 here, maybe there is a point 2 here also. There can be other points which do not cross like for example; there can be a 3 here, and a 3 here. So I am just showing the scenario where you recall this we are we have called as in channel number 1 and this we have called as channel number 3 and this was channel number 2.

So, we said that we have to first route channel 1 and 2 followed by channel 3. Now let us see why? You see suppose I consider a channel 3 first, this is my channel 3, this is my rectangular region this entire thing is channel 3. Now in channel 3 what is a definition of a channel? There will be 2 boundaries parallel boundaries with the pins on some location on the 2 boundaries. Now you see on this side the position of this 1 and 2 are fixed, but what about this 1 and 2 here. So this along this line it can be anywhere. So we do not know exactly from where this 1 and 2 nets are coming. So that is why along this boundary this 1 and 2 are said to be floating terminals, but suppose we route net 1 first. So I am just giving an example suppose we route it like this one to vertical connection and one horizontal connection. This is the first connection. Then 3 will be connected. Let us say 3 will be connected like this. 3 is connected, then 2, let us say 2 will be connected like this right.

Suppose this connection have been done. Now once this is done you look at 1. Net 1 we have already laid it out on a particular track. So now, net 1 will be coming here this will be 1 and net 2, once this is laid out net 2 will be coming horizontally along this point this will be 2. Now you see now this floating terminal and 2 which are not defined, now this have become fixed this is 1 this is 2. So after 1 is complete we can move to 3. And in 3 we can complete the routing in a similar way. Like for example, for connecting 1 from here we can have a line here, we can have a line here, then we can have a line here.

Similarly, for 2, we can have a say line here, and here, and connection here. So in this way we can complete the connection, in fact this example will tell you why we need to route 1 and 2, first and then 3. Alright so this is for this particular scenario. This is a slicing placement topology, but suppose I have this second scenario, which is a non-

sliceable floor plan or a so called wheel. So here if you just check once you cannot route all the regions again in some particular sequence. Because there maybe terminals coming from some other directions. Say for example, I start with 1. This 1 may be having terminals coming from the left, coming from the right. Some maybe floating terminals and some terminals coming out here, floating terminals here, so this will be like a switchbox, where terminals maybe coming from all sides, not only vertical and horizontal, but on this side as well as this side.

So once you route 1 may be you find the order of the other. So once these terminals are fixed you can or these are fixed you can route 2. Once 2 is fixed you can route 3, once 3 is fixed you can route 4, but here some of the routing regions may be considered to be as switchboxes and not simple channels. This is what is the difference.

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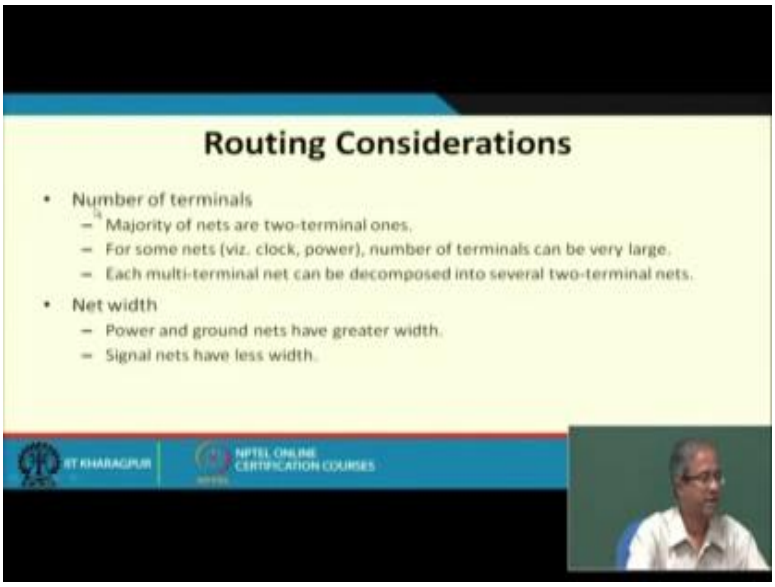

Some other routing considerations are as follows, one is related to the number of terminals well most of the nets may be 2 terminal nets, that connects only 2 points, but some of the nets clock and power are of course, obvious once, but there can be other connections also which corresponds to fanouts in some circuits, the output of the gate maybe going to 3 different places so, 4 points needs to be connected together, but clock and power are 2 examples where a large number of terminals may need to be connected. So clock and power shall be considered in separately because they require very special techniques, but otherwise the multi terminal nets are typically decomposed into 2

terminal nets and then they are routed one at a time. The 7 consideration is rated to the width of the vias or the lines. Some of the lines which carry higher currents like power and ground they may need to be of greater width, but the ones which are carrying signals they may be of less width no problem.

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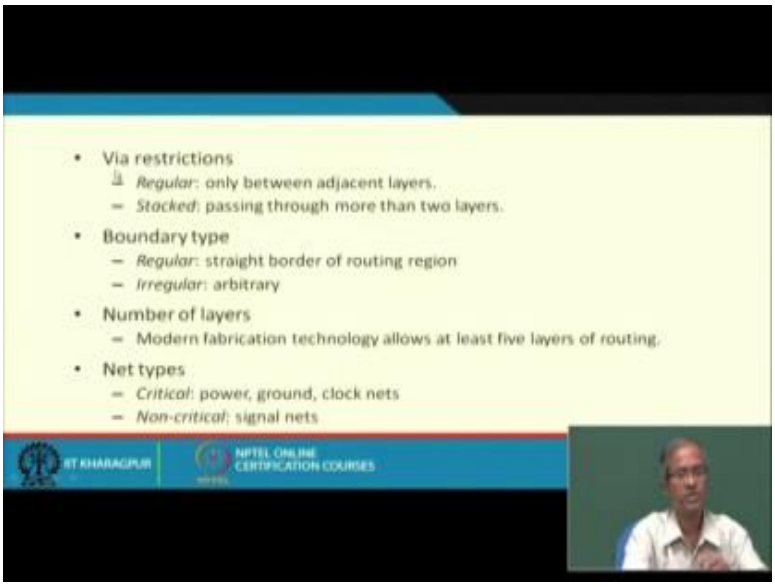

Then via, via means recall what I said via is a connection between 2 points on 2 adjacent layers. There has to be some kind of a hole with a metal in between that connects 2 points on 2 different layers. One thing you remember having via is a layout in a fabrication process is a little difficult, so less the number of vias the better.

So, via again can be of 2 types. One is the regular vias which are only between adjacent layers which may be easier and stacked means connections which maybe passing through more than 2 layers which means we have to drill much further and make a connection. So stacked vias are more difficult.

Boundary types again the examples we have taken so far they have all straight line boundaries, but in general they may be arbitrary. Number of layers may be different may vary. Modern technology allows 5 or more layers and again regarding net types. Some of the nets are very critical like the power and ground lines clocks. They need to be addressed separately and very carefully. And there can be other nets which are not so critical like the signal nets.

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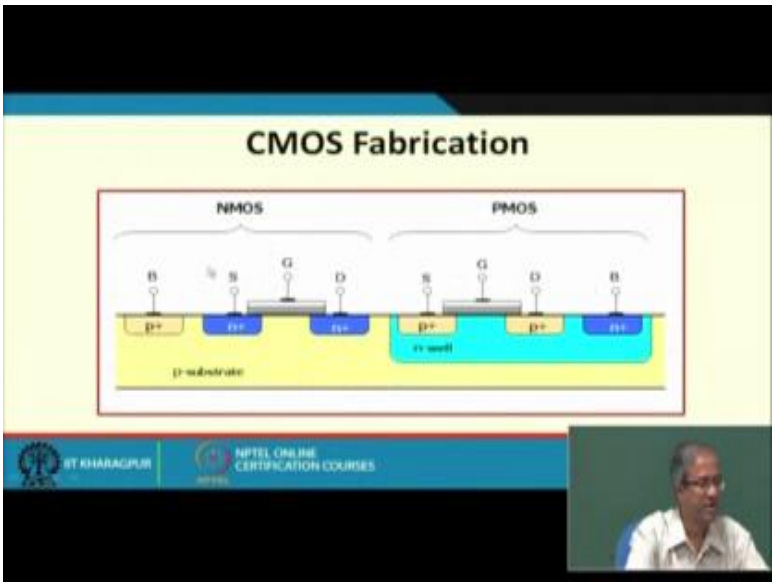

Just a very quick look, this diagram shows you the typical cmos fabrication of a n type transistor, NMOS transistor, and a PMOS transistor. So you can recall, we need to have a substrate, where you have the gate and this source. Here gate and the source, drain and the source, this is drain this is source. And gate in between and gate has to be fabricated on top of a insulating layer. Similarly for the p type transistor PMOS, we create an n well, within this we create 2 p type doped regions one is source other is the drain and again a gate in the similar way.

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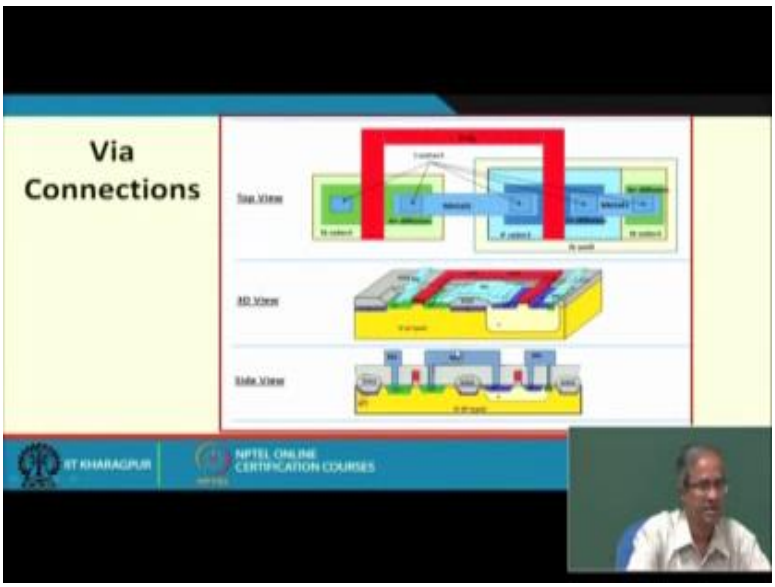

So the reason I am showing this is that when the transistors are interconnected, like I am showing another picture very quickly. This is the top view of 2 transistors one is an n type transistor one is a p type transistor. There source and drain are connecting by a metal. And their gates are connected together by a poly silicon line. So 3D view it looks like this. The gate is connected like this. This is your source and drain of the of the n type transistor. This is the source and drain of the p type transistor. And this metal on layer m 1 connect this source and the drain just like I have shown here.

Now, side view you can see that for connection you need to drill holes like this m 1 to take connection you have to have a connection like this, from this drain you have to have a connection like this. This needs to connected to the source like this. So there can be multiple such connections. This is the example of via connection that I had said. Via connection can exist between any pair of layers or for routing we are more interested in metal to metal connections, via connections between adjacent metal layers.

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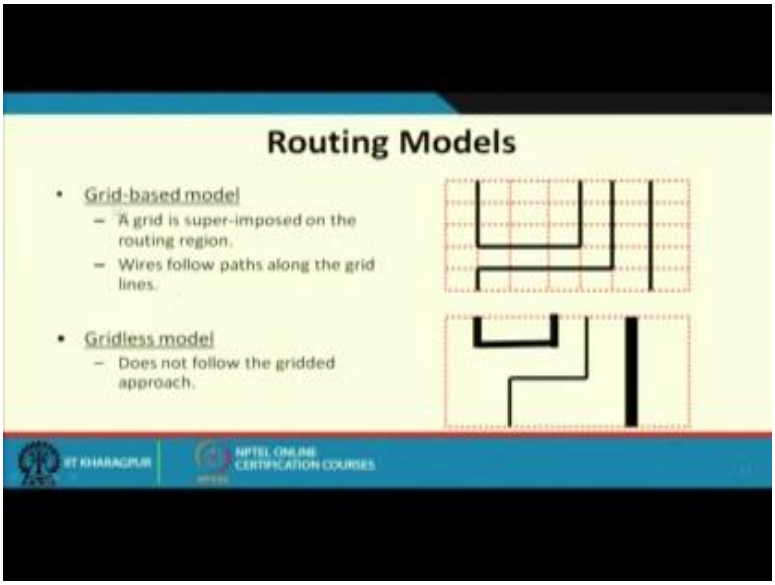

And regarding routing models, well most of the routing techniques we shall talk about they use a grid based model, where all the lines are considered to be of equal width and they are aligned to grid boundaries like this. But in general the lines can be arbitrarily placed and also arbitrarily shaped in terms of the width the heights and also need not be aligned to the grids. So typically the power and ground nets follow this approach.

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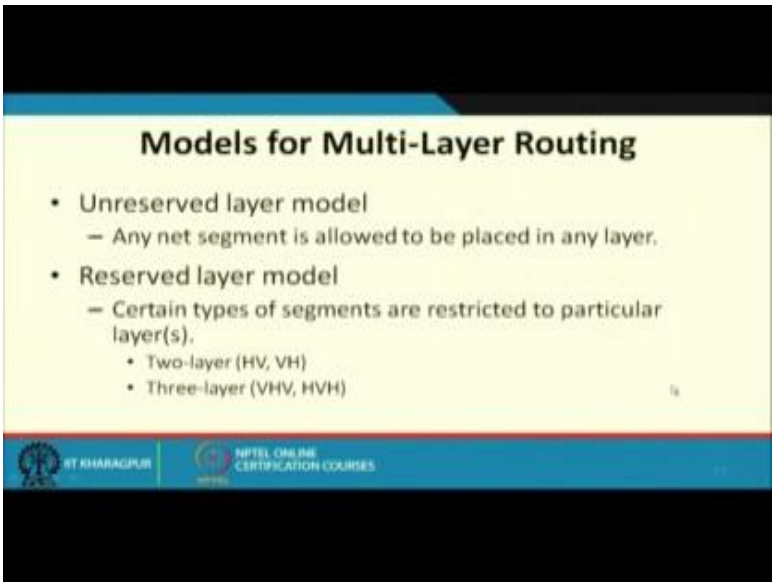

And next, when we look at multilayer routing means we have more than 2 layers available with us. There are some models for that also like the examples that we have said the blue line and the brown line. We told that they are located on 2 different metal layers, but in general there can be more than 2 let us say 3. 3 layer is quite popular. So there you can have 2 broad approaches, one is unreserved means that any net segment can be placed up on any of the other layers.

The second one is the reserved layers where we have some restrictions. That is reserved layer model for example, in a 2-layer case you can say HV; that means, horizontal connections on metal 1, vertical connections on metal 2 or vertical on metal 1 horizontal on metal 2. There are 2 layers if you recall, so you make a convention that all horizontal lines will be on the metal 1 which is below and all vertical lines will be metal 2 which is above. In case of 3 layers' m 1, m 2, m 3, you can have some similar conventions. Like you can have either VHV, vertical on m 1 horizontal on m 2 vertical on m 3, or the reverse horizontal vertical horizontal.

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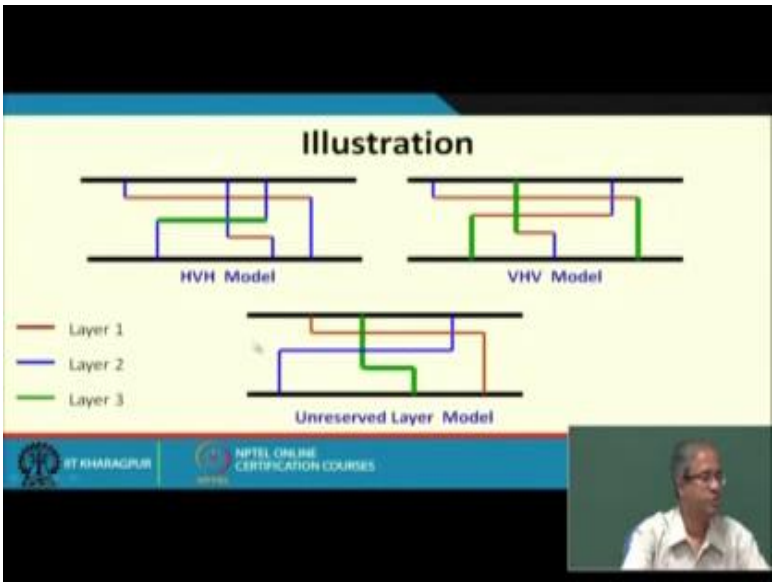

So, usually most of the algorithm we talk about will be following some reserved layer model. These are some examples for a 3-layer routing. This shows HVH. Where you see horizontal is brown vertical is blue this third horizontal is green. So these are the 3 layers VHV is let us say blue is vertical, brown is horizontal, green is also vertical. VHV, but you can have unreserved layer model where you can lay out an entire net on a same layer like blue, so some segments are horizontal some are vertical. Similarly, this brown, same layer, green on the same layer, so unreserved layer model means this. So you can layout both the horizontal and vertical segments of a net on this same layer.

Now, see unreserved layer model maybe little difficult to handle algorithmically, but has some obvious advantages. If you can lay a net entirely on the same layer you will not need any via connection for connecting to the other layer. So there are some obvious advantages there, but again most of the algorithms they do some kind of a systematic transformation of the problem to some kind of a layout that uses some kind of a reserved layer model, that we shall see later.

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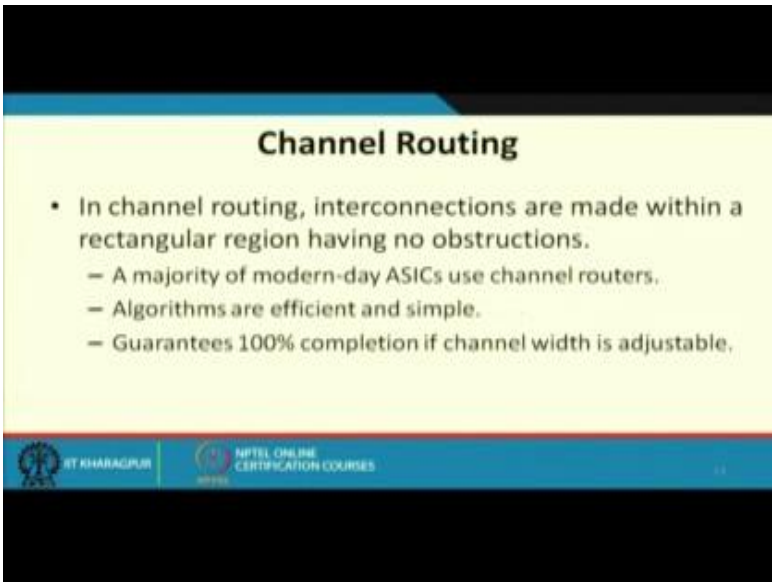

Channel routing is the most important kind of detailed routing problem that we encountered because as I said most of the VSLI chips asics that we fabricate or design today, they use the standard cell or the semi-custom design methodology.

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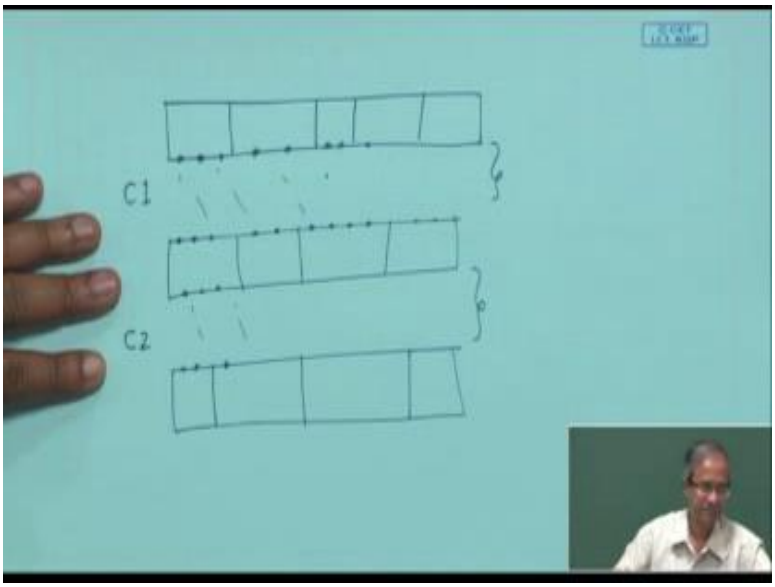

They are the cells are arranged in rows like it looks like this. I have one row of cells. There can be multiple cells varying with. There is another row of cells; there is another row of cells like this. Now one thing we can; obviously, see that the space that is there in between 2 consecutive rows, this is naturally a channel. It is a horizontal channel with

pins are coming from top and here the pins are available here. And you will have to connect them; you will have to interconnect them.

Similarly, there are pins here. There are pins here you will have to interconnect them. So there will be one channel C1 in this case there will be another channel C2 in this case. So the problem boils down specifically to the channel routing problem here right. So as I said that here in channel routing case, we carry out the interconnections within rectangular region.

Now inside the channel the way we have defined it there are no obstructions. There are no blocks which you have placed inside the channels right. So this as I said most of the modern chips that if I fabricate, there we have channels and that is why we use channel routers. The advantage is that the algorithms are very, I mean say efficient in terms of their speed and quality. And if you can adjust the width of the channels which in standard cell is possible, then hundred percent completion of routing is guaranteed which is indeed a problem in general routing case. Say I mean ensuring hundred percent completion of routing is one of the milestones that we usually select for the problem of routing.

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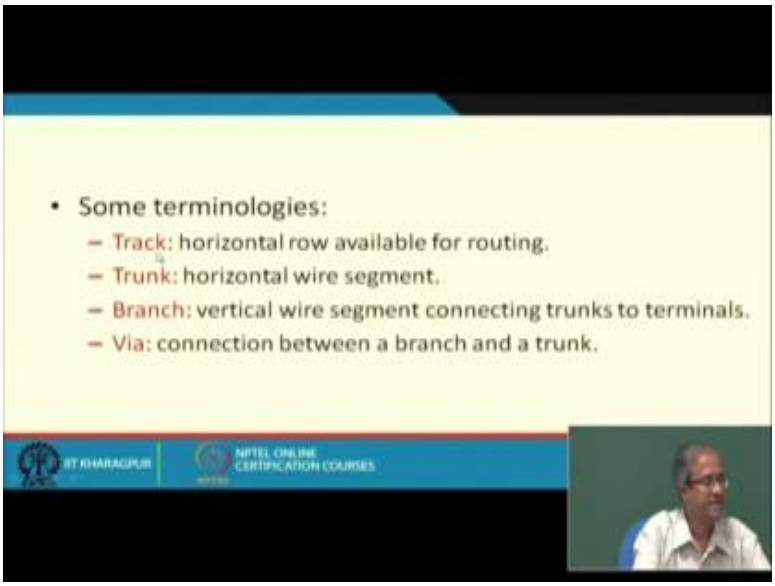

So, there are some terminologies that we use in channel routing. Track, track is a horizontal row that is available for routing. Trunk is a horizontal wire segment, so one net maybe connected using multiple trunks. Branch is a vertical wire segment that

connects a trunk to a terminal and as I said via is a connection between 2 layers between a branch wire between a trunk wire. So let us take an example.

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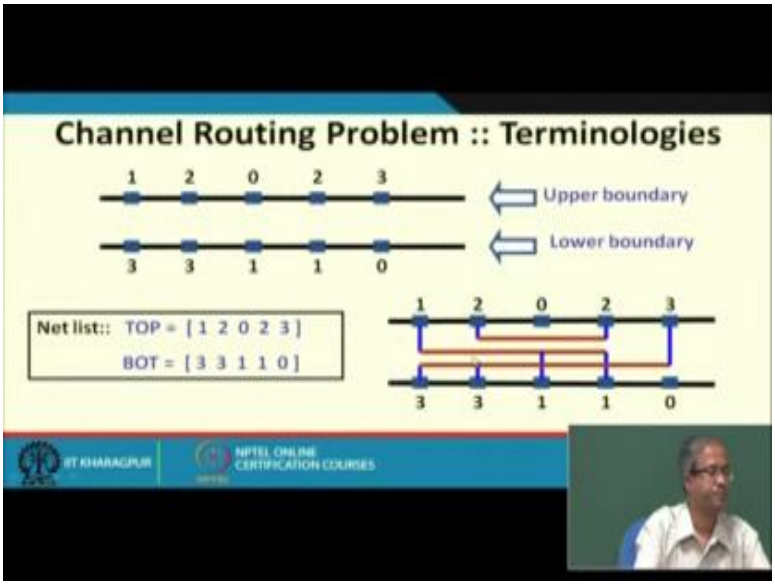

So, so a channel routing problem is diagrammatically depicted like here. So I have 2 horizontal lines with some numbers which indicates pins. This one will indicate the pins that have to be connected, the first net 2 indicates the pins to be connected, and 3 also have to be connected. 0 means no connection. So this can be represented by 2 lists. Top and bottom 1, 2, 0, 2, 3 is a first list. 3, 3, 1, 1, 0 is the second list. So if you are trying to write a program to implement any of the channel routing I mean instances of algorithms. Then the input problem you can represent it by 2 one dimensional arrays. And one possible solution is this. So here you see these are the like you recall the definitions branch is a vertical wire segment and trunk and tracks are horizontal wire segments. So these are the branches blue are the branches. And this is trunks, but you see track means the horizontal row trunk is horizontal wire segment so what is track.

Track here I am saying that the 3 tracks available to us, but on the 3 tracks we have laid out 3 trunks. Track means the space that is available to us on the rows and trunks maybe I am not using the whole space a part of it I am using to layout a horizontal segment for a net, that is a trunk.

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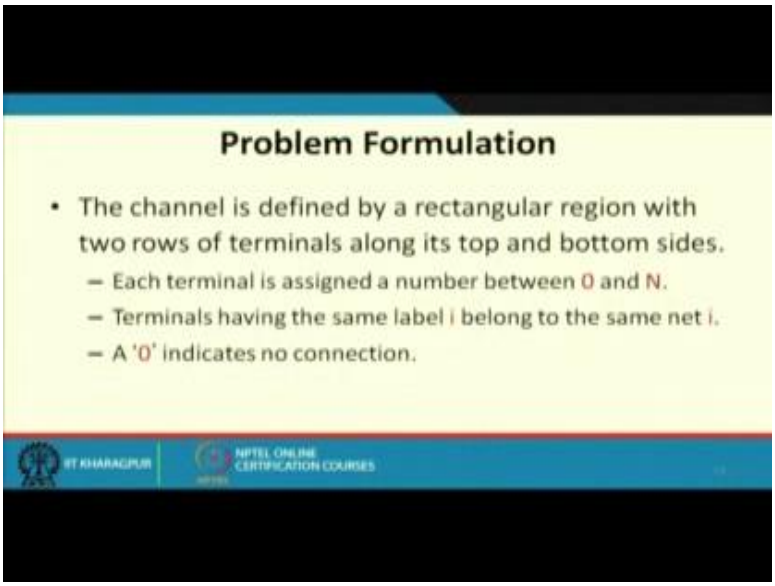

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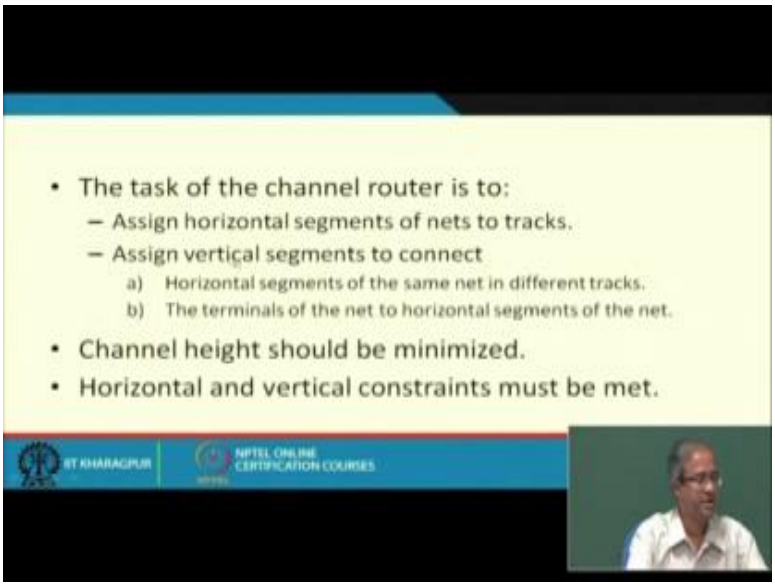

So, this already I have mentioned. So the task of the channel router will be to assign the horizontal segments of net to tracks, and assign vertical segments to connect the horizontal segments of the same net which may be placed in different tracks, and the net terminals to some of the horizontal net segments.

The objective is to minimize the channel height, and we shall see later there can be some horizontal and vertical constraints that must be met.

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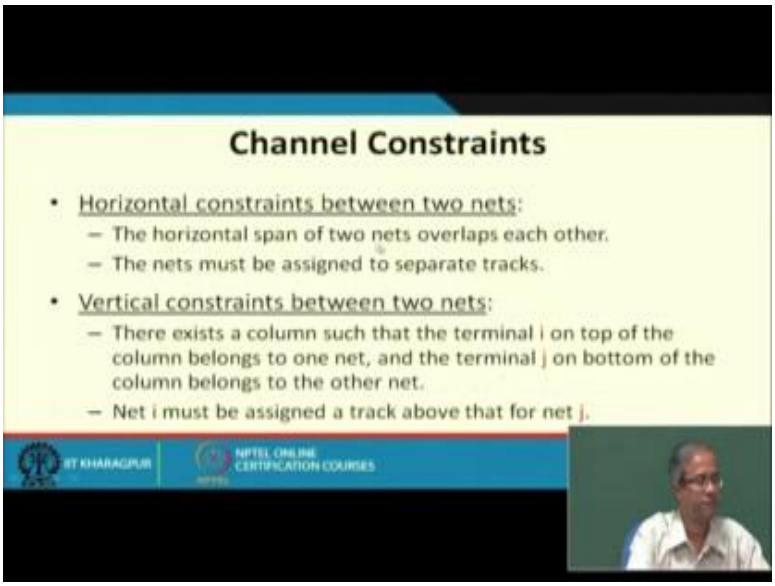

So, let us quickly see what are these constraints. The horizontal constraint says if the horizontal span of 2 nets overlap each other, then the nets must be assigned to separate tracks.

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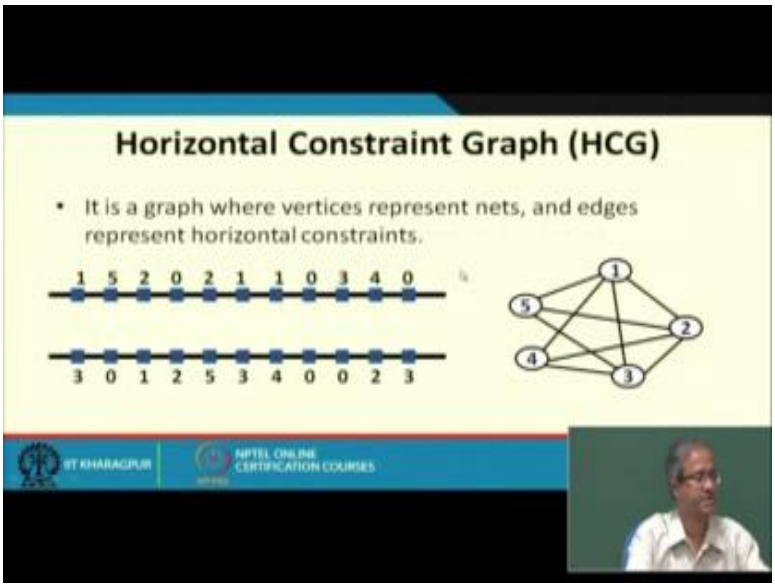

Let us take an example suppose I have a channel routing problem like this. I see the net one is here and here so the span of net 1 is from here to here. So and net 2 is here, here and here, net 2 is here. So there is an overlap between the ranges. It means you cannot layout 1 and 2 on the same track. You need minimum 2 tracks.

So, the HCG horizontal constraint graph is a graph, where the vertices indicate the net numbers. And edges will exist if 2 nets they intersect somewhere in some column. Like for example, there is no edge bit in 4 and 5. Let us see 5 is from here to here. And 4 is from here to here. There is no intersection; they can be laid out on the same track if required. So this is what is the horizontal constraint graph. Then we have something called the vertical constraint, where it says if there is a column where the top terminal is i and the bottom terminal is j, it means net i must be assigned the track above j this we shall see later through examples.

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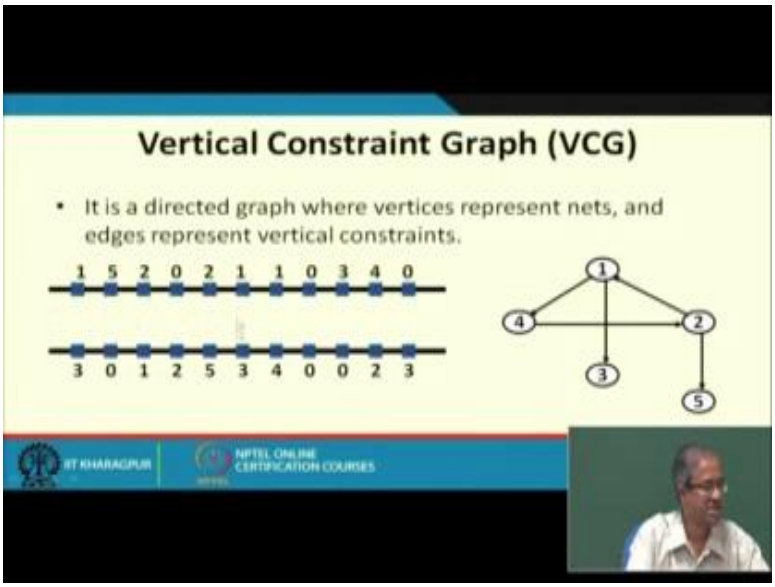

But vertical constraint is like this. If again this is the channel routing problem, you say one is above 3, 0 is no connections. So ignore this. 2 is above 1, 2 is above 5, 1, is above 3. So in this graph the edges will be having directions 1 is above 3, there will be and arrow from 1 to 3, 2 is above 1, there is an arrow from 2 to 1 like this. This is a vertical constraint graph. And you can see these graph can also contain cycle, like one is on top of 4, 4 is on top of 2, somewhere here, and 2 is on top of 1 somewhere. 2 is in top of 1, 1 is in top of 4, 4 is in top of 2. So there can be cycles in the VCG also.

So, we shall see later in our next lectures that how we can use this HCG and VCG for channel routing problem to device simple and re-efficient algorithms for channel routing.

Thank you.