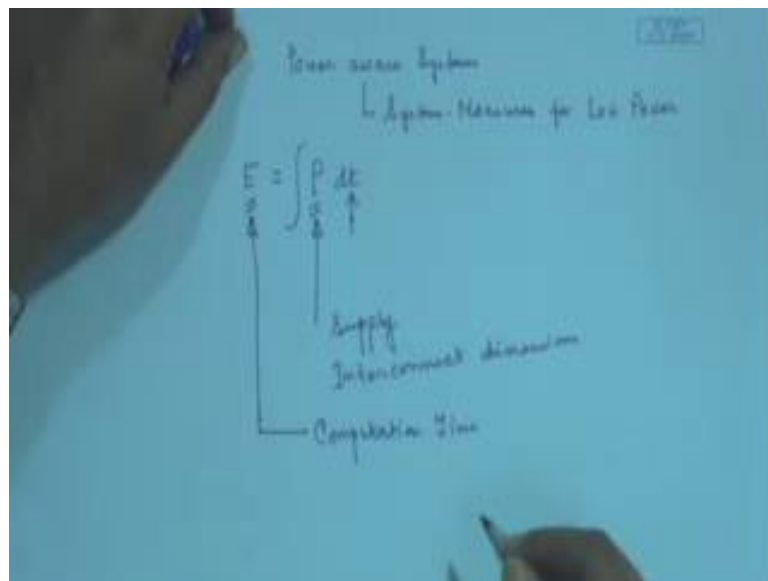


**Embedded Systems Design**  
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**Lecture – 20**  
**Power Aware Embedded System – I**

Let us start it. So, we will start discussing today about a very important aspect of embedded system design that is Power Aware Systems.

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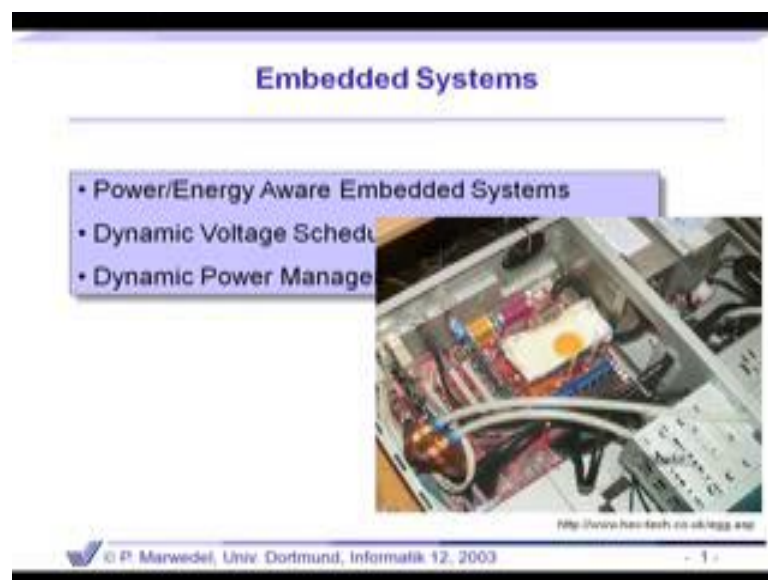
Or the system measures that can be taken for low power. Now there are two things that we have concerned about: one is power. Now all of you know what relative power is right. And another factor is energy. And you know that they are related energy is the integral of power over time. But both of these are important, so therefore three things are important: one is the power and one is the energy, and the power and energy are related by the time for which you use it. So, if you are doing net searching on your mobile for a long time then more power will gain out.

Now, net searching doing on your mobile it is actual intension may be at you will, but there are some programs which are taking more time to done. Therefore, they will affect the time component and for the same power mode energy will be drained. So, why are we concerned power? Power as such will affect the design of the power supply, how to design the power supply alright. It will also be determined by inter connects their

dimensions. If there be I mean depending on inter connect dimensions and the way they are drawn more power may be consumed.

Energy on the other hand is an integral of the power; therefore we will also be concerned about the computation time. So, you want to minimize both of them. Now we will see in today's lecture and maybe a sequence, through a sequence how we can approach the management of power. Because power is becoming all the more important for embedded devices which are portable and mostly run on batteries, and the battery life's are very important even when we go for say mars expiration or wavelength spacecrafts. We have got the power supplies and they have got a life. So, we have to enhance that life.

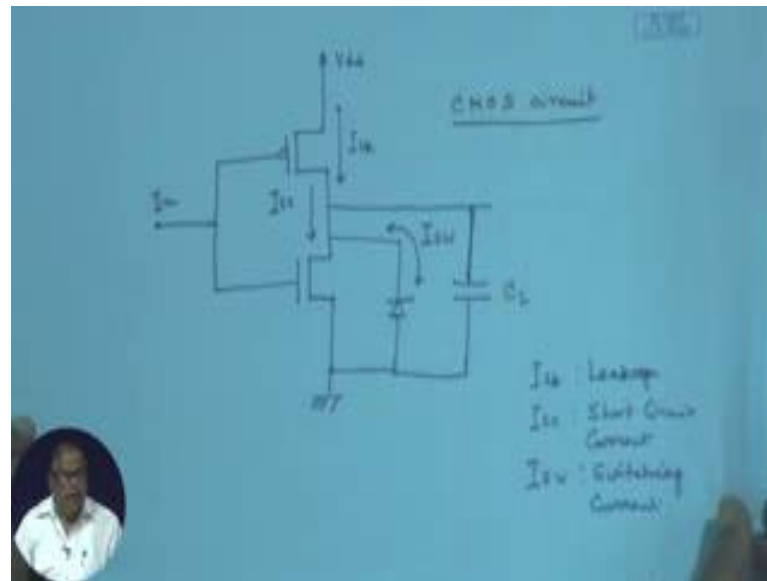
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So, our objective is to study power or energy aware embedded systems, dynamic voltage scheduling; the two approaches and two approaches dynamic voltage scheduling and dynamic power management by which we can approach solving this problem or at least approach try to solve this problem. There is a very important picture here that so much heat is generated in a Pentium processor that we have got a egg poacher, so you do not really need a kitchen here; you can put your egg on the heat sink and you can get your breakfast ready.

So, next let us come to the fundamental solve power consumption of a gate. Where from does it comes?

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So, let us have a look little look at the circuitry without going into the integrities. We have got a supply voltage and we have couple of transistors, now this is negated and there is another one and we are giving the input at this point alright, this is a transistor. So, from here we have got some current that is flowing even when the transistor is off that is the leakage current, I write it as a  $I_{lk}$ ; the leakage current. Whenever this transistor is on then there is a short circuit current that is the current is flowing through this. And across this transistor I have got some load through a ballet and from here I can take a capacitor sorry, and that is a actual load and we have to put the ground. So, that is the  $C_L$ ; the capacity of load.

Now, whenever we are making excursions in this circuit, the excursion is between 1 and 0. So, whenever we are switching from 0 to 1, so this transistor then we are having a switch in current flowing through here. So, that is it can be either way it will be switching current. So we have got three components: one is  $I_{lk}$  which is a leakage current, which is there all the time, there is a short circuit current; we do not have much to do with that and the other is the switching current. More the switching activity in a circuit the more will be the power consumption.

So, this is the basic circuit behind any component of an embedded system if you assume that, then we can come to a couple of equivalence.

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Handwritten equations and definitions on a blue background:

$$\Rightarrow P = \alpha \cdot C_L \cdot V_{dd}^2 \cdot f$$

$\alpha$ : Switching activity  
 $C_L$ : Load Capacitance  
 $V_{dd}$ : Supply Voltage  
 $f$ : Clock frequency

$$\tau = k \cdot C_L \cdot \frac{V_{dd}}{(V_{dd} - V_t)^2}$$

$V_t$  = threshold voltage  
 $V_t \ll V_{dd}$

$$P \approx \alpha \cdot E = \alpha \cdot C_L \cdot V_{dd}^2 \cdot (f \cdot t) = \alpha \cdot C_L \cdot V_{dd}^2 \cdot \# \text{Cycles}$$

Below the equations, there are two small diagrams of CMOS inverters. The first is labeled with  $(100)$  and  $(001)$  at the inputs and outputs. The second is labeled with  $(111)$  and  $(011)$  at the inputs and outputs. An arrow labeled "time" points from the first inverter to the second.

Say, we can write the power can be expressed as alpha which is a coefficient denoting the switching activity. The load capacitance that you have shown here the load you know as much as the load increases the power consumption will increase, we have to drive more the load impedance. The other component is the supply voltage and it varies as a square of the supply voltage times the frequency at which we run it. So, what are the things? Alpha is a switching activity, CL is a load capacitance Vdd is a supply voltage, and f is the clock frequency. These are very important equation that we have to remember.

So, this tells us a couple of things. This tells us that if we increase the circuit switching then power consumption will increase. It also tells us the CL, but the CL is basically this is a hardware component. So, whenever we design it if we can reduces the CL part; then obviously P will be reduced. The supply voltage- now we will have a lot of things later on coming where we can play with the supplied voltage and the frequency. Now, the supply voltages of the frequency are also related.

Now this is one parameter the power and we can see that the power consumption increases quadratic quadratically with the Vdd. And there is another thing which is the delay let us call it tau, delay of switching in a CMOS circuit, this is nothing but a CMOS circuit. So, the delay of switching delay in a CMOS circuit can be given as some constant k times the load capacitance times Vdd divided by Vdd minus V; let me call it t,

$t$  is a threshold square that is beyond this voltage nothing will happen but switch will take this.

So, here again  $V_t$  is the threshold voltage that is dependent on the device design. And actually  $V_t$  is much much less than  $V_{dd}$ . So, what we observe from here is that while the power is quadratically related to the  $V_{dd}$  it increases quadratically as the supply voltage increases; here it the delay is increasing or decreasing?

Student: Increasing.

Is inversely proportional linearly, of course it is linearly. So, decreasing the  $V_{dd}$  will reduce if I decrease the  $V_{dd}$ . It will reduce the power quadratically, if I reduce this part. If I reduce this part then delay will increase. And as the delay your increases that is causing an imperilment to the frequency at which you I can drive the circuit, that is actually determining the frequency. So, this  $f$  and this  $\tau$  are therefore very close; very closely related. So now, for energy optimization let me keep this side on and say  $P$  is alpha whatever we have that I did not write that can be here, but energy is  $\alpha CL V_{dd}^2 f$  into  $t$  where  $t$  is a time. Now, if I look at this component  $f$  times  $t$   $f$  is number of cycles per second and  $t$  is the time, therefore I can conveniently write it as write it here  $\alpha CL V_{dd}^2$  number of cycles. But this gives us a lot of insight here, one thing is we will playing with  $V_{dd}$  a lot, but we can see a number of things coming up here which will take up in detail later. Say number of cycles; number of cycles or program will embed a program we will take to RAM will be how, will be dependent on what?

Student: (Refer Time: 14:46).

Complexity of the instructions, the number of instructions that are there in the machine level; who determines number of instructions that will be there at the machine level? The compiler, so given a task an efficient compiler will generate an efficient code, whereas an inefficient compiler will generate an inefficient code. Therefore, depending on that my number of cycles will vary and that will be affecting energy. So, you see the energy the battery life is not only depending on the hardware, but it is also dependent on compiler and we will see how it is also related to operating systems.

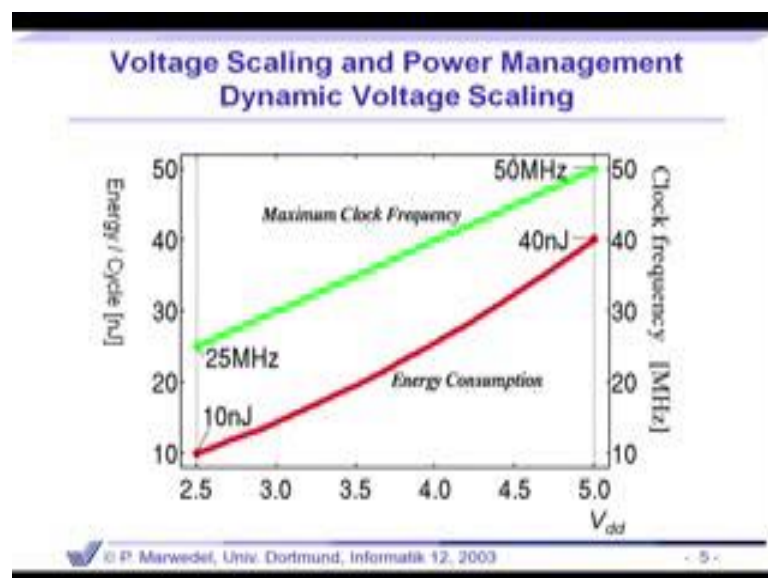
Now again, alpha it is a switching I mean the switching frequency. Now if I have just giving you an insight; if I have 1 1 1 1 to be one instruction, and immediately after that I

have the next instruction is 0 0 0 1. There is situation 1, and the situation 1 in another one is 1 1 1 1 and I have got 0 1 1 1 is the next instruction. In which case is there more switching?

In the first case I have to switch between each of them, whereas here I have to switch between only 1. Now where is this switching taking place actually? It is taking place on the bus wherever you are transmitting there also this switching is taking place. So, corresponding them bus will be actually number of components right. So, at every component that switching is taking place is alpha is becoming here.

Therefore, if we can quickly say that if the having the sync can be minimized between the consecutive instructions like where the alpha will reduced, but that is a very one angle to look at that but there are many other issues. So, when we design the machine code that is also very important. But, even never know which instruction will come after what. So, that you can probably over large segment of codes you can try to make to some estimates. So, those are number of interesting issues are coming out over here right. So, saving energy how can I save energy under a given timing constant; I have to take some time. We can reduce  $V_{dd}$ , we can reduce a switching activity, we can reduce the CL or we can reduce a number of cycles. One thing is that I take is cycles thereby we can gain.

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So, assuming that this part is clear we can look at a slide here; you see let us keep this also side by side and let us look at this what does this slide say- again taken from Peter

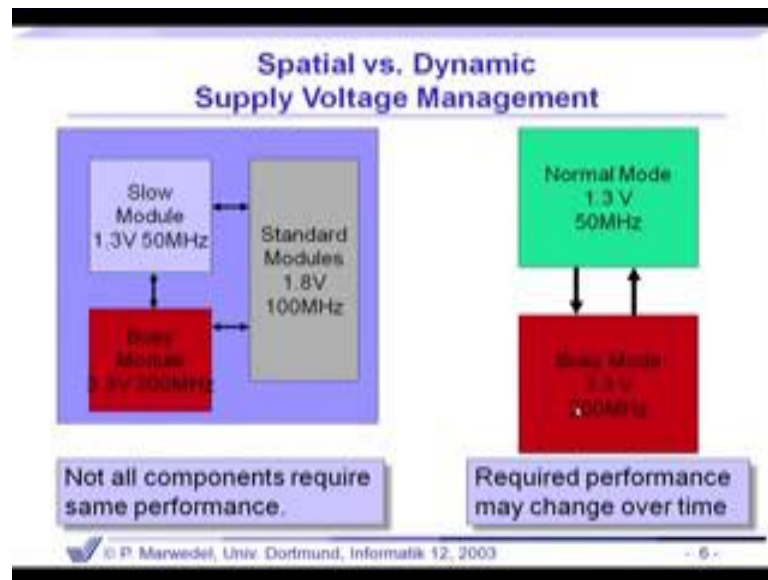
Marwedel with his permission. Now you can see this green one is showing the increase in frequency, the clock frequency and the Vdd. Here we can see that as we increase the Vdd; that means I am referring to this, I am referring to this equation. This is pertaining to this equation right. So, it is increasing linearly this one. As the Vdd is increasing the maximum the delay is inversely proportional to the frequency; so that you can understand with.

So the frequency, the moral of this is what that if I give higher Vdd I can probably operate this thing at a higher frequency. On the other hand as I increase a Vdd and if I look at this axis which is energy per cycle in nano Joule it is increasing quadratically more or less. So, here at 2.5 volt I am consuming 10 nano Joule, where at 5 Vdd I am consuming 40 nano Joule alright.

So, there are two aspects of sync: one is depending on the Vdd I am also constrained to the maximum frequency where up to which I can go. If I can increase the frequency my thing will be solved faster, but that may not always be the case. So, that is the challenge; first of all let us try to realize the challenge and then we will look at the solutions. Now how can we handle this? Once again it may quickly revise this part. This part tells me that the power of the over time energy will increase in the square of Vdd, because here I find that the delay will be linearly I mean it will be inversely proportional so the frequency will be linearly proportional to the Vdd, as I increase the Vdd I will get more and more frequency.

Now the frequencies are important because as the frequency increases my energy consumption is increasing. So, all these are interrelated. So, how can we manage this?

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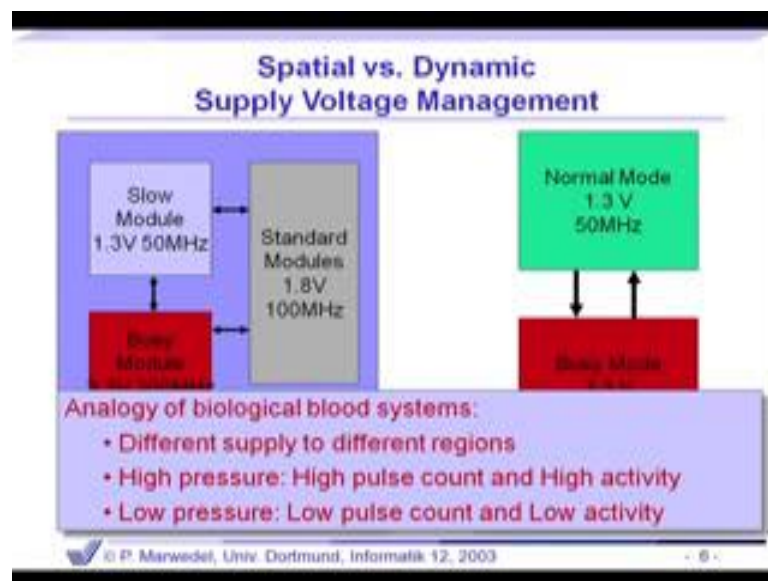
One thing that we can think of is spatial and dynamic supply voltage management. All the first parts of the circuit need not be given a uniform Vdd, the same Vdd. We can have say for example, this part is a very busy module and most this is a hotspot, most of the computations have been done here in the red one. So, I want to make it faster. So, I put it at 3.3 volt and 200 megahertz. Now if I go from this sort of curve I can say that at the particular Vdd what is the frequency that I can take.

So here sorry, here I can have at 3.3 volt I can run it a 200 megahertz. Whereas, this one is a standard one not that busy, I run it at 1.8 volt which allows me to run at 100 megahertz. So, I am slowing it down, I am reducing the Vdd also, but I ultimately lead to see for most of the embedded systems there may be a real time constrain. So, we have to meet the dead line right. So, I can do a mix and match of my allocations of Vdd's so that I can meet the dead line at the same time I consume less power. And for the slow module you see I have put 1.3 volt and my slower frequency 50 megahertz.

In another, if there is a three level it can be also there are two modes are busy mode and there may be a normal mode. So, depending on what is a performance here the performance is reduced, therefore this part this module I do not know do not need any longer.

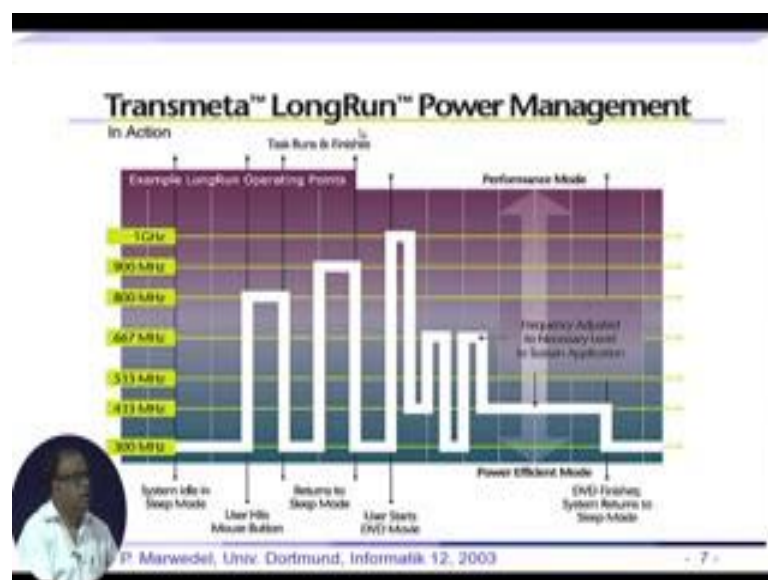


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So that sort of thing takes place. The analogy for this is the biological blood supply systems. Different supply to different regions, depending on the activity whichever parts are more active and wherever you increase the activity of the particular point then the more and more blood supply goes there. So, accordingly you can adopt your policies at the (Refer Time: 23:46).

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So here is the another example to illustrate this thing, that is a Transmeta is a processor and for a particular benchmark what is being shown is we can see that; if we look at the

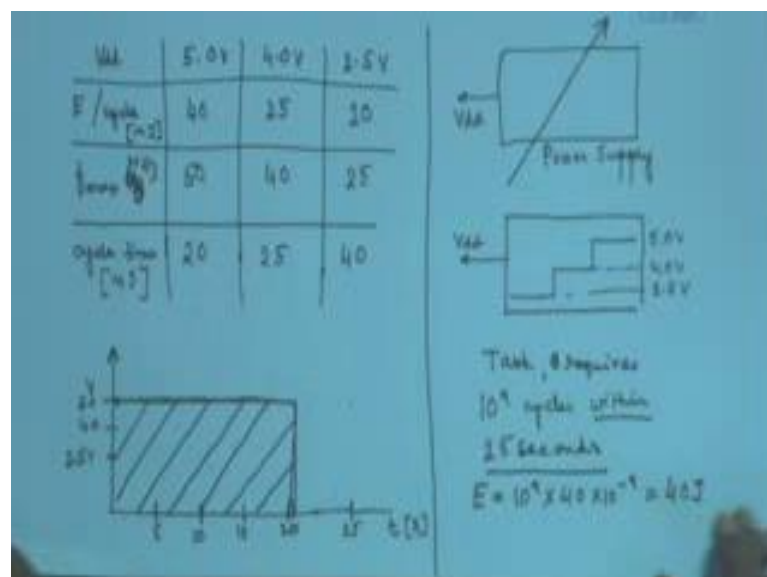
power initially we are running it at 300 megahertz why, we can see that the system is idling as a sleep mode here. And here comes our request use a hit of a mouse button. So, some tosses have been ambiguated. So, immediately we can see the frequency, I have changed the frequency to 800 megahertz. So, I am adopting the frequency. Now here the task runs this task that was initiated at this point runs and finishes here. It cannot be (Refer Time: 24:49) right now. And then it returns to the sleep mode.

Again here it might be something has started. Here at this point user starts a DVD movie immediately if it solved. Now just in the earlier slide I had shown if the performance requirement is not the same all the time. So, when the DVD started you needed to start this DVD and all those we needed more power, therefore at that point I short it up at 1 gigahertz alright. So then, later on when it is stabilized then I can come to much lesser frequencies; frequencies are just in to the necessary level to sustain that application, and that is going a steady state.

And then ultimately it come DVD finishes and I go back to the sleep mode. So, in that way we can change the frequencies. So, it is not necessary that when you have got a 1 gigahertz processor; that means, all the operations. If all the operations are done at 1 gigahertz a huge amount of a power will be consumed. So, that is automatically adjusted.

Now, ideally we can think of a processor for the sake of power management to have a power supply which I can continually change.

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Suppose I had a Vdd box here, a power supply box for the Vdd; some Vdd comes out of this, it would be ideal if I could continuously control it, if you do linearly controllable for every point. But that is practically not very feasible to have such continuous supply. For that most of the systems that we have we have some discrete levels of say may be 3 levels of power supply, see 5 level, so whatever.

So, here we can switch between any of these levels and we can get the Vdd. Say it can be this one is 5 volt, this one is 4 volt and this one maybe 2.5 volt alright. So, if we assume that sort of scenario then let us assume this- that we have working in a scenario at Vdd I will vary there are three possible Vdd's: one is 5 volt 4.0 volt and 2.5 volt all these are volts. And by the equations that we have shown we can have energy per cycle and we can have the  $f_{max}$  in hertz; the maximum frequency that we can run and we can have the cycle time.

Once again coming back to this here; so we are playing with a Vdd and depending on the Vdd we have some frequency component and so consequently will have the cycle time and set a time is the inverse and we will have the energy per cycle. So, as you know that we can have, say at this we have got 50 this is megahertz I am sorry, frequencies in megahertz; so it can be 50, 40 and 25 megahertz by the characteristics I found that these are the values.

So, the energy per cycle here we found is 40 nano Joules, for this it is 25 nano Joules, and for this is 10 nano Joules. And the cycle time therefore this is 20 in nanosecond; 20 nanosecond, 25 nanosecond and 40 nanosecond. Now we have got that, so I have got this choice right. That I can run it at 5 volt, I can run it at 4 volt, I can run it at 2.5 volt. And consequently corresponding to each of them I will have so much energy consumed per cycle this is a maximum frequency at which I can run it etcetera.

Now I am given a task; a task has been given that requires 10 to the power 9 cycles to be run within 25 seconds. So, my deadline is 25 seconds. I am given a scenario where I have to run the task within- say this is 25 and say this is 20 my scaling is wrong. So, this should be 15, this should be 10, this should be 5 and this carrying a line sum up. So, these are the different this is time in second.

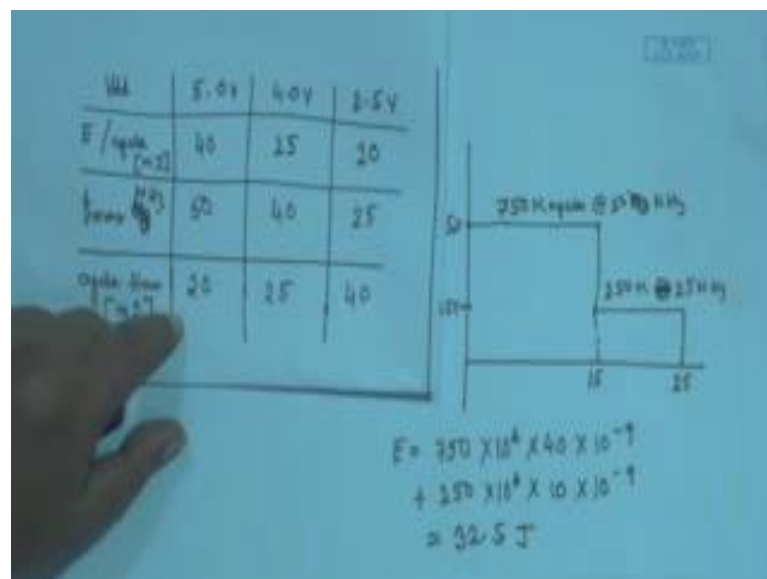
Now, if I have to run 10 to the power 9 cycles. So, if I run it at 5 volt say here it is; so this is 2.5 volt, maybe this is 4 volt, then this is 5 volt. If I run it at 5 volt can you tell me

how much time it will take to complete, 10 to the power 9 cycles. And I am running it at 5 volt; so 20 nanoseconds per cycle. So, it will be over by 20 seconds. Although my deadline was 25 seconds, so I have run it at 5 volt and I put finish it off within this time.

So, the energy consumed is this I will be getting from here. So, this is the energy consumed is actually will come from; not from this, this is a task area Vdd taken 5 volt I will compute some energy here how much will that be 40 per cycle and I took 10 to the power 9 cycle. So, my energy consumption will be 10 to the power 9 cycles every time it is 40 nano Joule; energy was in nano Joule. This was I did not write, this was in nano Joule; I am sorry the energy given here is a nano Joule so it will be 10 to the power minus 9 so that will be 40 Joule.

So, I am consuming 40 Joule of power, 40 Joule of energy by running it at 5 volt, but was it necessary? If I had I mean since I can run it at a frequency of 50 megahertz I could finish it much earlier which I need not do. If your constraint is that you have to finish the job as early as possible in that case certainly you can reduce it. But otherwise I had the scope of reducing it, so let us try to do that. With the same distribution if I take; the same distribution remaining here alright as earlier if I had scheduled it in a different way I am sorry.

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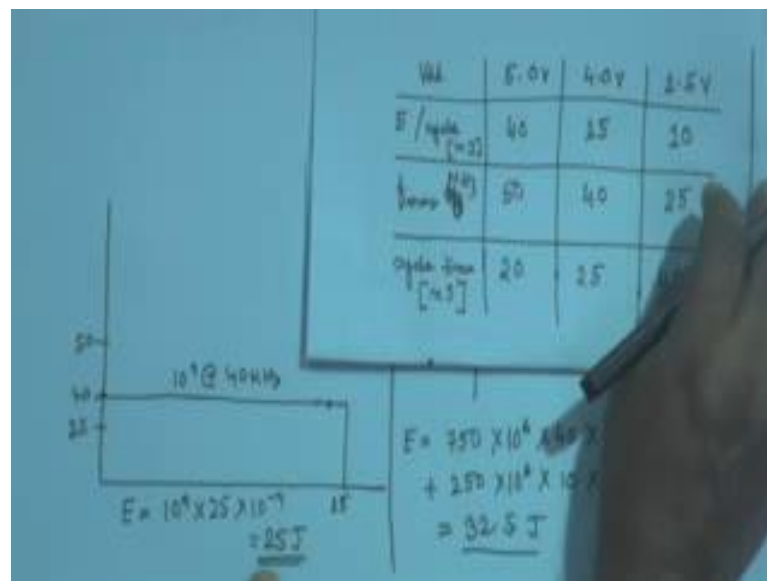


If I have scheduled it here say I run it at 5 volt for 15 nanoseconds; for 15 nanosecond I run it 5 volt and then for the remaining 25 nanoseconds, here is 25 my criteria was to

complete it within 25 seconds. If that be the case that here I run it for 2.5 volt and here I run it for till 15 I run it for 15 seconds I run it like this, what will be my energy consumption? What will be my energy consumption? I have run 750 mega cycles at 50 hertz; 50 mean 50 hertz, 5 volt means 50 hertz. So, I have run actually 750 megacycles here I mean 750 million cycles I am sorry; whenever we see capital M is mega, 750 million cycles we had run at 50 hertz and only 250 million cycles at this is at 50 hertz because of this at 5 volt I could run it here and this much and 25 hertz megahertz; sorry 50 megahertz centered to the (Refer Time: 37:49).

So, my energy consumption will now be 750 into 10 to the power 6 into 40 per nano cycle, this a part cycle and 10 to the power minus 9 plus 250 into 10 to the power 6 into 10 into 10 to the power minus 9. So, that will come to 32.5 Joule. What did you get earlier? We got 40 Joule earlier. Now the last option another option we take. So, by this we get 32.5.

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And if I keep this again here and just run the whole thing at 4 volts there is 2.5, this is 4 and this is 5. So, instead of running it at 2.5 the whole thing for 25 seconds I run it at 4 volts.

Then how many cycles am I expending at 4 volt for 25? 4 volt gives you 40 there is a frequency. How many cycles are you spent? You need 10 to the power 9 cycles. So, all the 10 to the power 9 cycles at 40 megahertz, what will be the energy consumption? Let

us compute that in here it will be 10 to the power 9 times 25 into 10 to the power minus 9. So, that will be 25 Joule. So, you see for the same task I had three possible voltages: 5, 4 and 2.5. So, by adjusting by combining into them I can get different energy consumptions; one was 40 Joule, one was 32.5 Joule, another is 25 Joule.

Stop here, and we will carry on with some algorithms which can be use to find out what will be the optimal one.