Electronic Design Automation
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Lecture No #19
Backend Design Part-V

In our last lecture we were discussing about the floor planning problem. If you recall we had looked at some of the representation of the floor plan. We had looked at some of the methods of floor planning like the 1 which uses integer linear programming, like the 1 which uses the concept of the rectangular dual graph. And lastly we looked at a method which was some kind of a hierarchical approach starting from smaller floor plans we merged the blocks together into bigger blocks. And then systematically we got the complete floor plan. And finally we were talking about another approach which is based on simulated annealing base technique. There we had mentioned that the approach is based on a very unique representation of the solution namely for a given floor plan you have the slicing tree topology assuming that it is a sizable floor plan. And you take the polish post fix equivalent representation of the tree. And that polish expression will be your representation of the solution. So the basically the simulated annealing formulation is based on that polish post fix expression.

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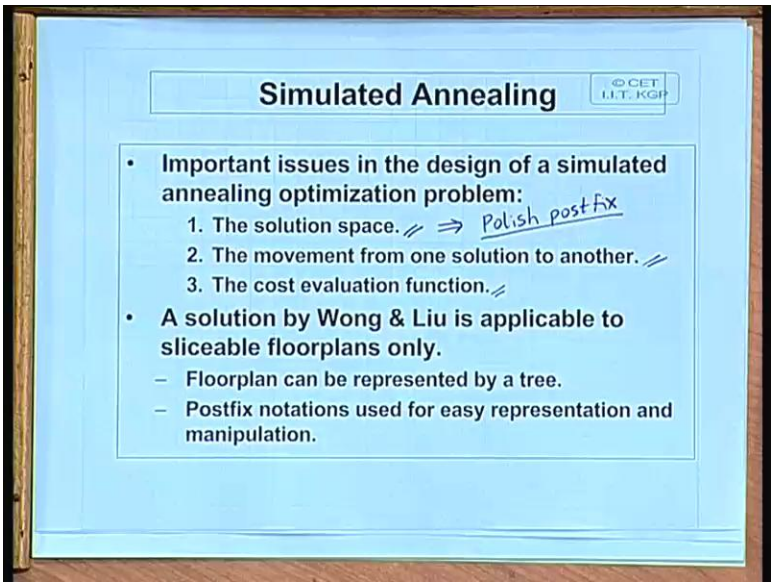

So just to recall once more simulated annealing based technique must talk about the solution representation which I have just mentioned. Here they use the polish post fix notation. Corresponding to the slicing tree of course moves will have to be defined which will change a particular solution into another and finally a way to evaluate the cost. Fine. So now let us straight away come into some of the details of the algorithm. Now the solution representation I have already mentioned it is the post fix notation of this sliceable floor plan tree the slicing tree topology.

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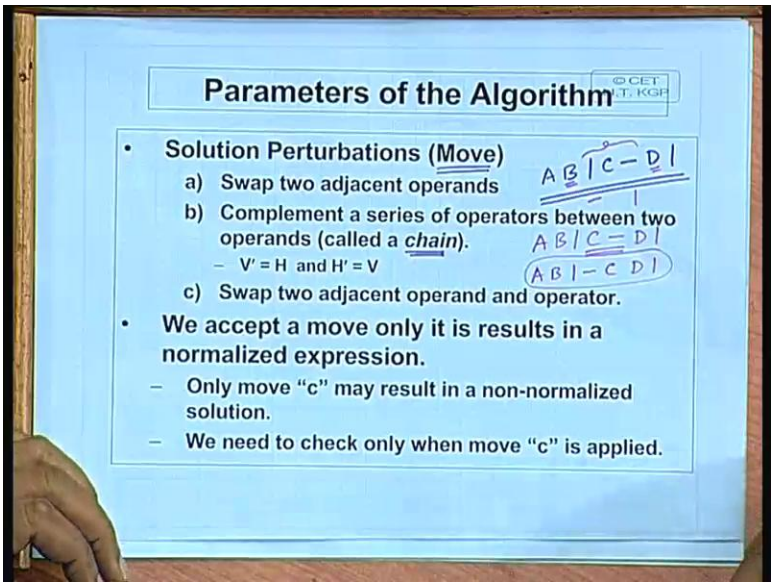

And regarding the other parameters first let us define the various moves that you can have a defined for going from 1 particular solution to another. Well in terms of the polish post fix notation there are 3 different moves which are defined. See a particular polish notation may look like this. A, B say vertical partition C horizontal partition D vertical partition suppose this is an example post fix notation. So the first 1 says that you swap any 2 adjacent operands. Well in terms of the expression you take any 2 operands AB or BC or CD and simply swap them. So here for example if you swap B and C it will become AC vertical B ok. So the first 1 simply exchanges 2 operands. Second 1 it works on a so called chain. Now a chain is defined for example I take any 2 operands. For instance I take the operand B. And the operation D so whatever lies in between that is called the chain. Ok. So the second kind of the move says that for a chain which means for a given pair of operands say B and D.

You compliment the operators like this bar will become dash this dash will become bar. So if it is a vertical operator it will become horizontal 1 horizontal will become vertical. So compliment a series of operators between 2 operands. And third 1 it says swap 2 adjacent operators and operands which means a say your expression was AB bar C dash

D bar. Suppose I select this 2 C and this bar so this will be transformed into dash C D bar. But 1 thing you understand the third 1 it is not necessary true that anytime you apply this. This will become a valid expression. So every time you apply C you will have to check for the validity of the resultant expression because for example this is not a valid expression. Because on the left there are 2 few operands right. While another thing we talked about something called normalized post fix expression. Normalized expression if you recall.

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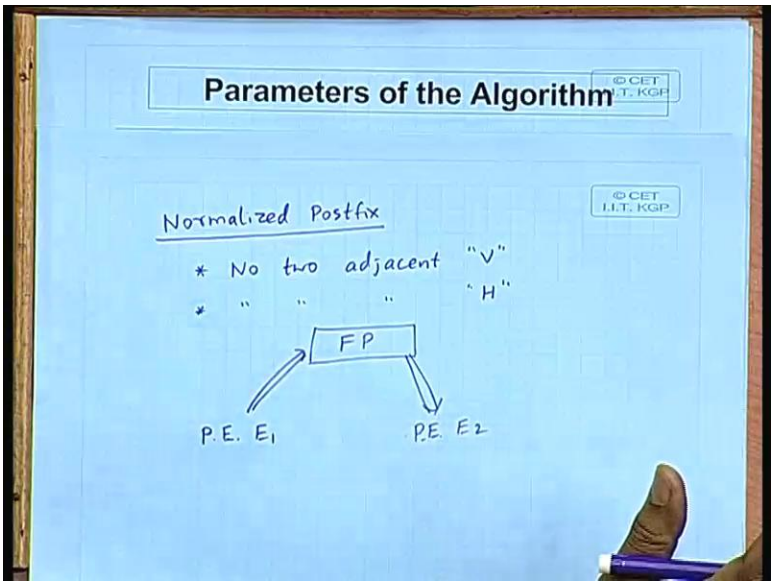

What we said normalized post fix. So here the requirement was that there should not be no 2 adjacent vertical or no 2 adjacent horizontal. And in this scheme all the solutions are constrained to be corresponding to normalized post fix expression because we had seen that if you have an un-normalized post fix expression. Suppose you have a post fix expression say E one. E 1 is un-normalized ok. Corresponding to that expression you will be having a floor plan. This will be a floor plan. Now for most of the floor plan I had mentioned that it is possible to find another polish post fix expression. Say E 2 which is normalized.

So for this same possible floor plan you can have another alternate representation which is a normalized one. So if you constraint ourselves only to normalized expressions it does not really harm. Means the advantage gain is that we can restrict the search space. So there are to this so searching for a solution will be faster ok. Now looking at the definition of this normalized expression if you just look at this moves once more. If you swap 2 adjacent operands so a normalized expression remains normalized right. Similarly if you compliment a series of operator some means some of the dash you make bar and some of the bar you make dash that will also leave it normalized. Because it is always enclosed with in 2 operands. Fine.

But there is a possibility the third 1 may convert the expression into an un-normalized one. Like of course in this example you cannot have. But in general you can have. So in the third case so for the first 2 case you need not do an thing if you choose to make move a or move b you can do it blindly. But for move c you will have to first check the validity of the polish post fix expression where there it is well formed or not and number 2 you will also have to check whether it is normalized or not. So only if both the conditions are satisfied then only you can accept move c as a valid move ok. Fine. So these are the moves which are defined. And regarding the cost function they had selected a very simple cost function.

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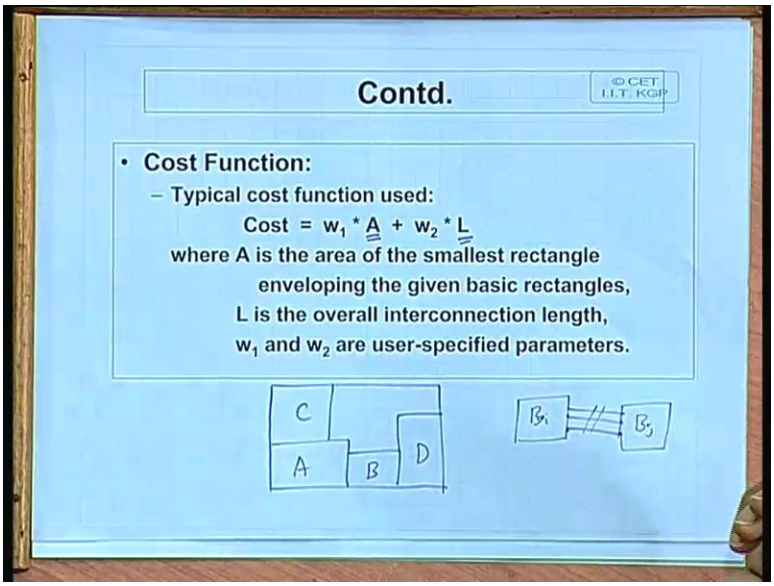

You take a measure of area and the interconnection length. Now area the way you estimate is that well you are finally placing the blocks on the surface of the floor. So you are trying to have a floor plan suppose block is A is being placed here. Block B is being placed here. Block C is being placed position of the smallest enclosing rectangle in the area of the floor plan. Say suppose D is again here. So A is the area of the smallest rectangle which envelopes the given basic rectangles. And L is the overall interconnection length we had earlier said that you can have a very course measure of interconnection length in so means when you are at the floor planning level.

So here for every pair of blocks say Bi and Bj the way you would proceed is that there can be several interconnection lines. You take the centroid of this rectangle take the center of this rectangle take the center of this rectangle. And you assume that all this interconnecting you can say pins they are residing at the center. And you just measure the center to center Manhattan distance. Just multiplied by the number of lines that goes that gives a measure of the length. So you do it for every pair of blocks I n j and that will give you an estimate of the overall interconnection length.

And of course w 1 w 2 are some parameters which uses can specify whether you are more interested to minimize the area or the length. Or equally you want to give weight age to both. So w 1, w 2 can be anything ok fine. So this was how the simulated annealing algorithm was framed. Of course the initial temperature number of iterations those are fixed out through experimentation. But I am giving an example to show that these moves A B C which we had just mentioned this really help in moving from a bad solution towards a good solution.

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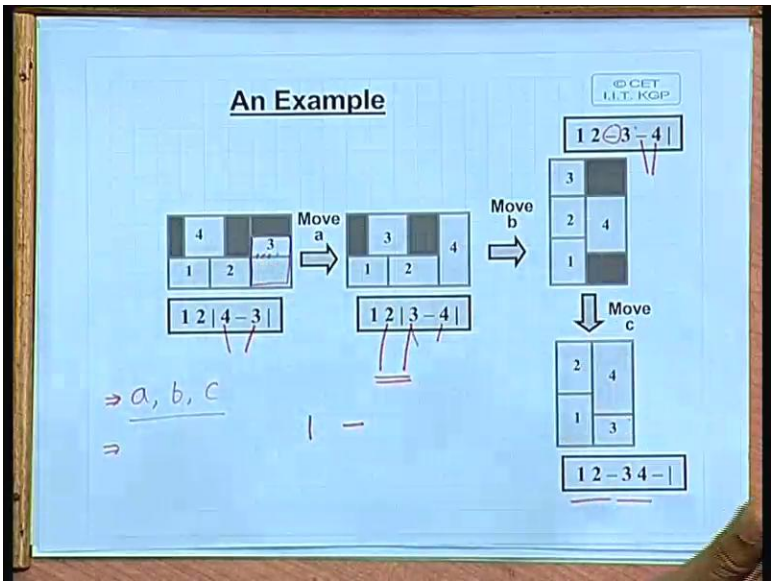

Of course in this example I am not illustrating the simulated annealing algorithm. But I am illustrating the 3 moves how they can make a solution improve ok. Suppose this is my initial solution. This is an initial floor plan suppose this is 3 this holder is 3 ok this. So this 1 2 are separated by vertical slice. This and4 are separated by a horizontal slice. And this entire thing and 3 are separated by a vertical slice. So this is the resultant floor plan. Now suppose I see in simulated algorithm the algorithm at each step you will have to randomly select which move you want to make A, B or C. Now once you choose to select 1 of the moves then you will have to randomly select the pairs of operands and operators where you want to make in the move on.

So there are actually 2 steps of it. First you select the move number then you select the 2 points of the solution where you want to make the move. Like for example in the first step when you make move a say you choose to swap this operands4 and three. Ok so the modified solution becomes this where 3 comes here and4 comes here in terms of the floor plan. You see now means the position of 3 and4 gets exchanged. Now assuming although this is now this diagram you cannot see the exact dimensions on a relative scale. Suppose4 was bigger than 3 so may be4 will be filling up this space more fully than three, 3 will come here. Next move b. Mover b means yes (()) (13:24) May be because the simulated annealing is a randomized algorithm you can always go from a good solution to worse solution.

This whether we accept it or not that depends on the probability there. (()) (13:38) Yeah, yeah sure, sure. There are some solutions which are not feasible you can check those things here fine. From here if you want to move make move b you have to define a chain again. Well here the way the chain is defined is that say you define a chain between 2 and 3 these 2 operands. Well incidentally within these 2 operands there is a single operator. You change it to horizontal. So now this says that 1 2 and 3 all will be separated by horizontal slices. And this entire thing and4 will be separated by a vertical slice something like this. And finally if you make moves c on this say you swap these two. These 2 operands and operator make it 4 dash. Now instantly this becomes a feasible solution and what happens this 1 2 will be together with horizontal slice, 3 and4 will be again together with horizontal slice.

These 2 will be together with a vertical slice. So maybe you will be fitting them very nicely like this. So just to show you that these moves can make a solution improve yes. (()) (15:03) See at each step we look at the cost function. Cost function takes cares of area as well as interconnection. Yes (()) (15:22) Move b? Move b says if you recall mover b says that you identify a chain. A series of operators between 2 operands they are complimented. So in this case you have chosen, you have chosen to select these 2 operators 2 and 3. So here in this example there is 1 operand only. So that 1 operand you

exchange you must swap. You compliment it in fact in the vertical you make horizontal so it becomes this. (()) (15:54) Yes (()) (15:56) Yes, yes. (16:03) See here you mean?

See in this example just for illustration we are only looking at the area the area just minimized but interconnection will also come into play. So if there is a strong interconnection between 1 and 3 then in terms of the cost function a good solution will require 1 and 3 to be together. So just this say for the sake of illustration but once implement we will have to take care of everything and the final solution which will be getting that will take care of the cost function you are defining. Ok it will try to find out the solution which is good in that respect ok. So we had looked at number of solutions for floor planning and I had mentioned that most people what they do now is that either they do floor planning or placement together or they use some kind of a hierarchical approach. Well this simulated annealing approach is also been reported by.

But I really do not know whether anyone uses this in means in any commercial tool. But in placement they do use it and simulated annealing is the most important you can say the algorithm used in placement ok. But in case of floor planning I do not think simulated annealing is used in any commercial tool. But these are interesting scheme or approach you can say. Yes (()) (17:36) Yes after move b it becomes this. Yes. (()) (17:45) See this is not but if the expression was 1, 2, 3, dash, dash, 4 bar this was un-normalized. Because these 2 dashes were consecutive. But here there is an operand separating them this is normalized but this is not. But actually these 2 are equivalent you see both mean the same thing. Ok so we had looked at the different algorithms for floor planning. Now there is another step to be done either during floor planning or immediately after that.

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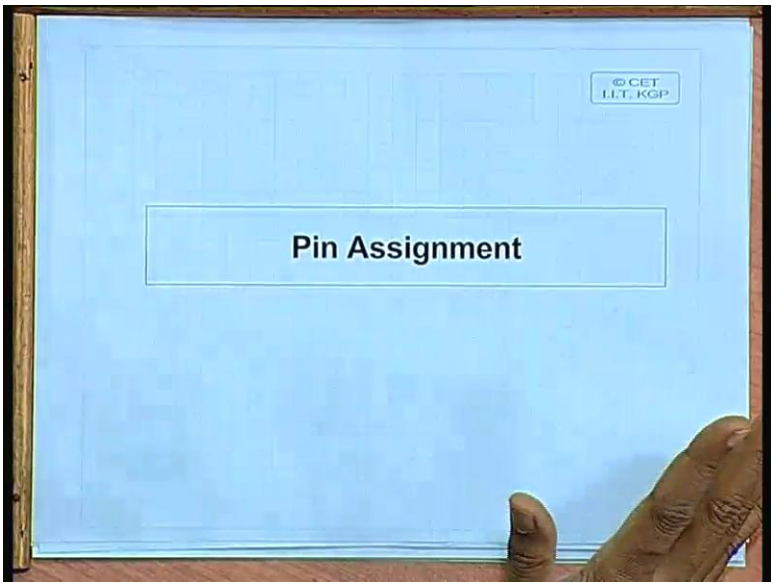

This is called pin assignment. Well apparently pin assignment is a much simpler sub problem as compared to floor planning. But you will see this is also important because a good pin assignment can give you a very good layout finally. So first let us try to understand what pin assignment means what is the problem all about. Ok.

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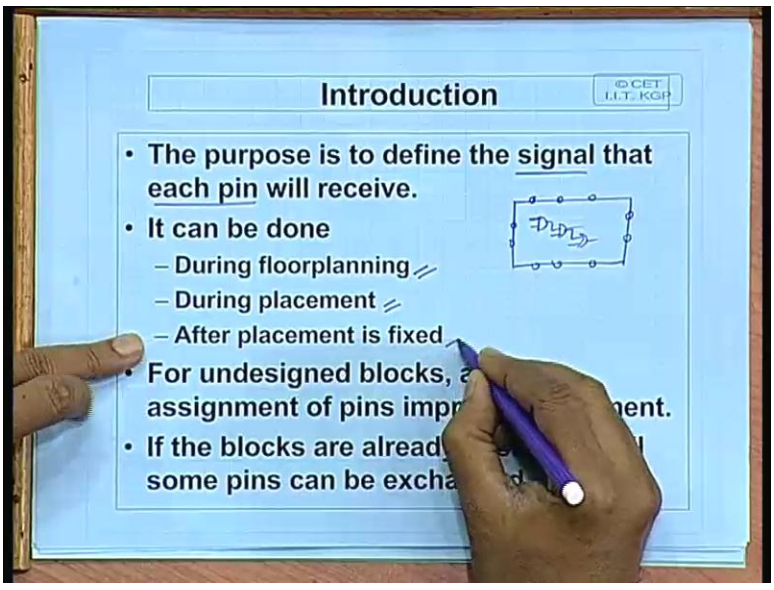

So in pin assignment the basic problem or purpose is to define the signal that each pin will receive. What does this mean? You think of a block. Well to the external world this block is nothing but a rectangular area structure with some pins on its periphery. Right there is some circuit inside there is a net list inside. Now which of the signal lines will be connected to which pin? That is essentially the pin assignment problem. Because if the block is fixed and pre design you do not have a choice it is already done. But in case of flexible blocks or wherever you can make this change you can possibly as for example this input to this gate you can assign either to this pin or to this pin. It depends on the interconnection of the other blocks. You try to reduce the routing complexity or the congestion so that with that in mind you try to have a good pin assignment.

You are trying to define or you are trying to assign a signal to the individual pins of a block. This is the pin assignment problem ok. Now this can be done during floor planning or even during placement. See after placement is fixed you can also do that we will see how. Because after placement is over what I have said earlier that in floor planning where making a tentative placement of the blocks on the floor plan. But after the sizes of the dimensions of the box have been finalized, the locations of the pins have been fixed and also the area the routing areas between them have been finalized that we say that we have got a placement like what I mean to say that I am taking a very simple example.

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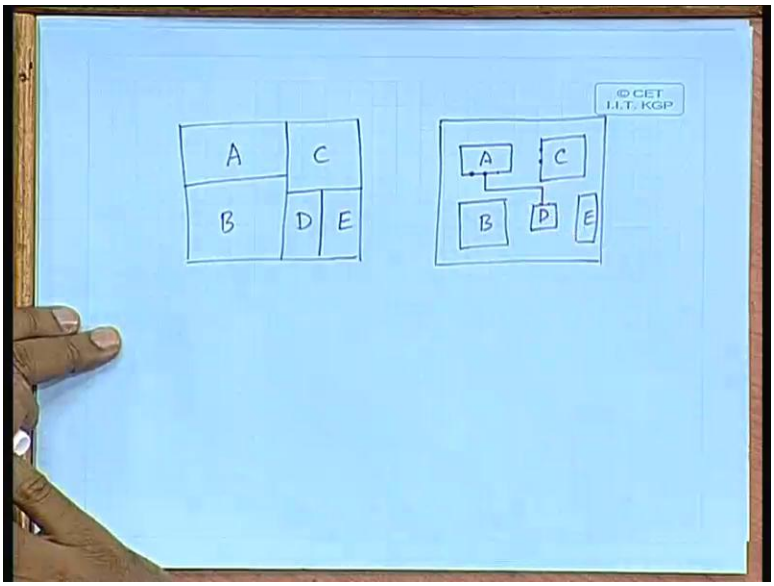

Suppose we have a floor plan like this. This is a sliceable floor plan. Suppose there are 5 modules. This is a floor plan. Now if we have a refinement where by we get something like this, this we call a placement. In a placement the exact pins have been defined. The net list are defined you also know that which pin you have to connect to which other pin of the other block and the routing of the interconnection areas are also defined which are the places which are available for interconnection ok. So this is the difference between placement and routing. Now here what you say that even after placement is complete still there is some scope for pin assignment we will see how. Ok. So we are seeing that the scope for pin assignment does not end even after placement is complete even after placement there is some scope for pin assignment fine.

So if the block is flexible not yet designed then a good assignment of pins will give you a better placement obviously. So interconnection to the other blocks will be more, easy to do. But if the block is already designed you do not have any choice of re-assigning signals to the pins. Still you can do some exchange of the pins will see how to improve the routability. Some pins often already design block and still be exchanged. (()) (23:02) Less pin has been done or the block you have taking from a library. For example where

the internal circuit is known and which signal goes to which pin that is also known. But still you can make some manipulation in terms of and in terms of assigning signals to the pins. Will see how? Ok just to look at the problem once more.

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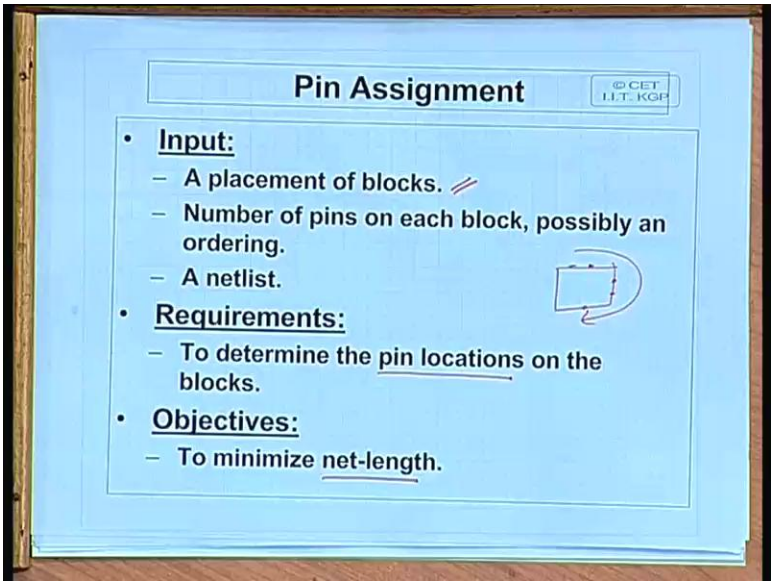

So for pin assignment we have the tentative location of the blocks it can be during floor planning it can be during placement. So you know how many pins are there on each block. For fixed block you know the exact locations. For flexible block you know that well this pin will be having this block will be having 5 pins. Now the exact location of the pins may not be known. But may be you will specify a ordering that that your pin signal a will be first, then b, then c, then d, then e. But the exact location you can fix up that whether it will be here or here. But the ordering can be specified by the user.

And of course net list how this blocks are interconnected. So requirement is to find the exact pin locations or to talk about in slightly more general term to assign the signals to the nets. Objective is to minimize the net length. Minimize net length as a bi product you will also reduce the congestion in routing. Ok. Now I have said that if your blocks are

already designed and the locations of the pins are already fixed, still there is some scope for exchanging some signals with respect to the pins how.

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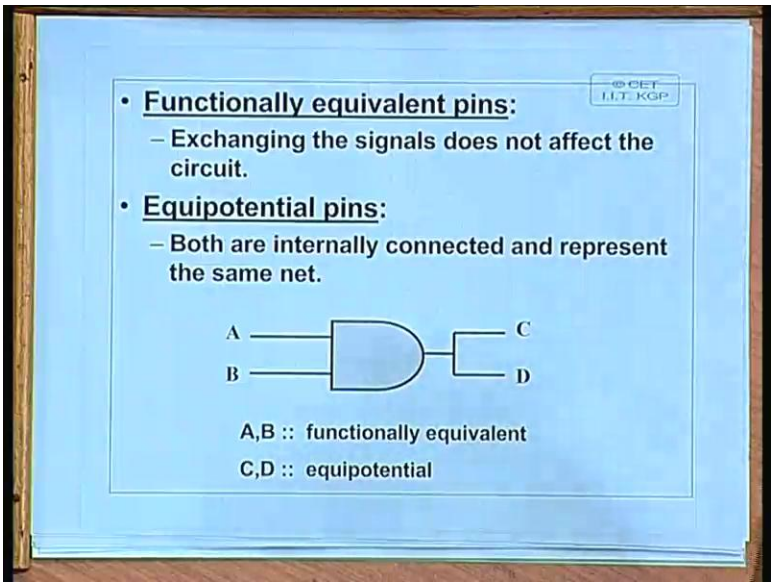

Well the concept is very simple you can define functionally equivalent or equipotential pins these are 2 different concepts. Functionally equivalent pins are 2 distinct signals but if you exchange them it does not change the functionality of the circuit like the 2 inputs of a NAND gate. So if 1 is A, and 1 is B it does not matter if you call this A and call this B. So if the function which is realized by this block is commutative then you can do this. AB and BA are the same. They are said to be functionally equivalent pins they are not they are not equipotential. Equipotential pins are C and D they belong to the same net. So the pins are the signals which belong to the same net they are called equipotential. But signals whose exchange does not alter the functionality of the circuit they are called functionally equivalent. Right? Now let us see how does this matter in terms of you can say, final placement or routing. Well I am taking a very simple example.

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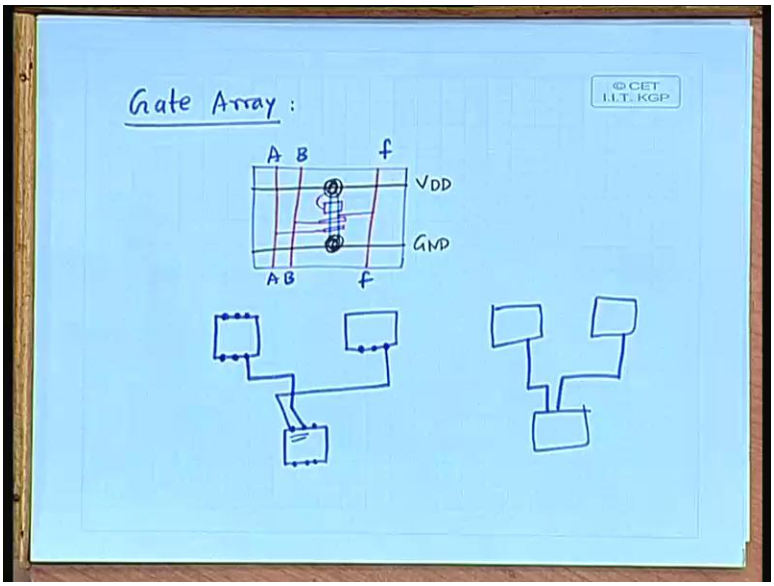

Suppose I talk about gate array designs. Now in a typical gate array the chip will consist of a large array of say simple gates NAND gates 2 input NAND gates. So in terms of the area in terms of the layout for example. So a particular cell for a gate may look like this. This red indicates poly silicon lines. Well I am showing the power supply lines by black and in the middle you have say. Well, the transistor laid out so lets say this is the diffusion layer. There is a connection with VDD this is VDD. And this is ground this is under connection here. And there are some transistors which will be the pull ups and pull downs. So there will be pull up transistor here it will be connected like this and there will be 2 pull downs thin ones. They will be connected to 1 will be connected to this other will be connected to this. Ok so I am not showing the exact layout and this will be connected to this. So with respect to this particular gate array well if you look at it functionally.

As a small rectangular box you will be having 3 pins on top and 3 pins on bottom. This will be the 2 input say A and B and the output F these are also available from top. So if you have the requirement of connecting some pin of here to some other pin of this say the output of this you want to connect to the input say here. May be there is another gate

similar like this so the output of that you want to connect to say the input this. So obviously has a crossing. But if you swap these 2 pins then you can get another solution where there is no swapping so it becomes like this. This output will come to the first pin this output will come to the second pin. So the way the routability is improve the congestion is this. So the idea of this the equipotential and the function equivalent pins and there utilization in case of routing and congestion control is like this ok.

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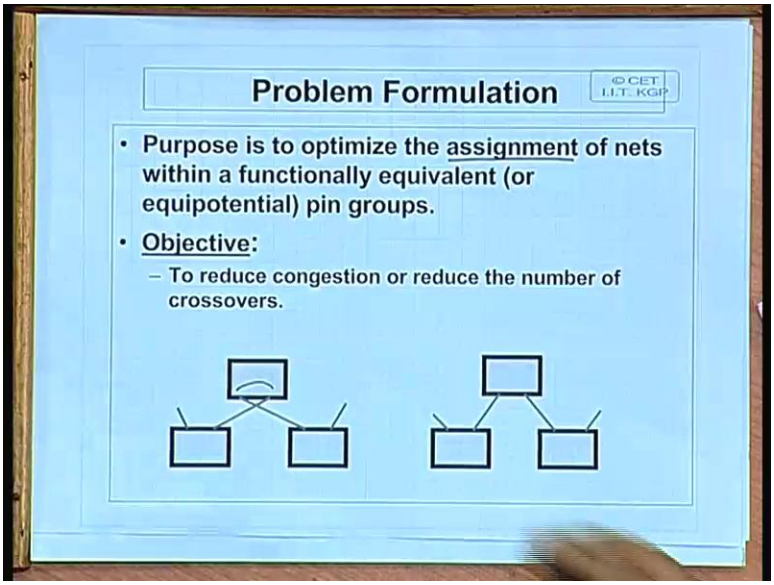

So what we have just said is essentially the optimization of the assignment of nets within a functionally equivalent or equipotential pin groups. So just the example I have cited is something like this similar to this. So there are 2 outputs so these 2 blocks signals are coming like this. But if you re assign them if there are equipotential or functional equivalent then you can swap them so they become like this. So this reduces congestion congestion means your routing will be easier now right. Now let us look at some of the design style specific issues for pin assignment.

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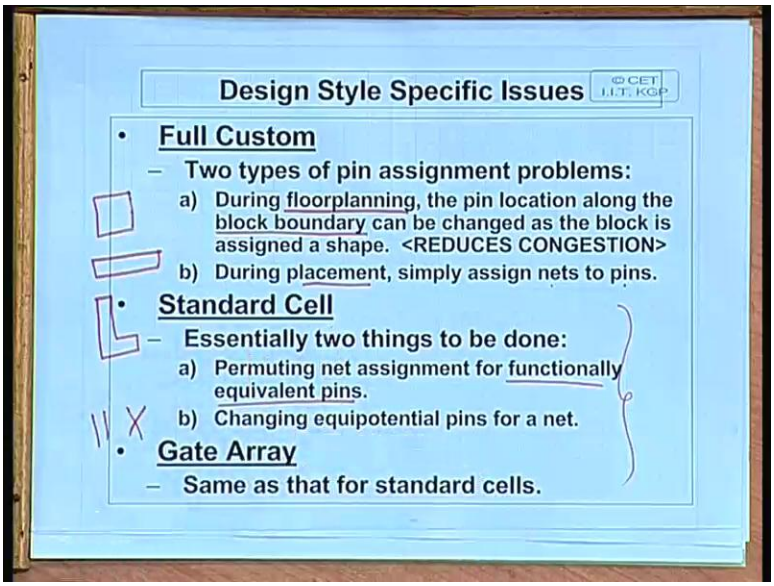

Well for full custom you have entire flexibility there will be many blocks which may be flexible which pre-designed are not already. So you have the flexibility of assigning pins on the periphery. So full custom design style exposes the complete you can say the range of the things you can do during pin assignment. But here normally you do it in 2 different steps. Number 1 is that during floor planning you can change the pin location along the block boundary. Because the blocks may be flexible so the block may finally assume a shape which is a square or it can be like this or in some cases it can also be l shaped in general you can also have blocks like this. So once you finalize the shape of the block the pin location along the boundary of the block will get defined.

They can be changed during this step with an eye towards congestion control like the example I have cited. The interconnection with the other block should be easy. Number of signal processing should be minimized something like that. And secondly during placement you make utilization of the other concept like functional equivalent or means or the equipotential pins in order to assign the nets to the actual pins. So this can be done in 2 distinct steps. Because if you try to just do both these things together you may lead to

a little problem the problem can become little complex and standard cell or gate array here the problem is simpler.

See here basically you will have to you have to identify the functionally equivalent pins and the net assignment you can do some swapping out there. So you have the flexibility of permuting the assignment of the nets for the pins which are functionally equivalent. Just whether you will be connecting like this or will be connecting like this. Changing equipotential pins this is flexibility so for the standard cell you do not have any flexibility of changing the position of the pins just for the equipotential or the function equivalent pins you can play around with it. Similar is the case for gate array right. Ok. So here I am I will not go into details of these algorithms.

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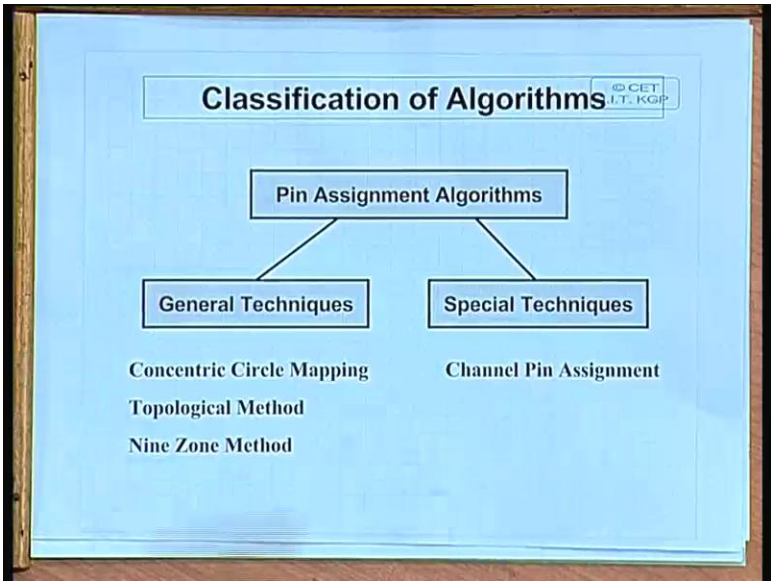

I will give you an idea what this algorithms are all about how do they work roughly. Broadly speaking the generalized pin assignment problem can be solved in several techniques some of this methods are concentric circle mapping topological and 9 zone method. But for very specific sub problem particularly in case of standard cell based design you can have something called channel pin assignment where you have the

concept of routing channel and you are doing pin assignment with respect to a particular routing channel. Ok fine let us try to see these methods.

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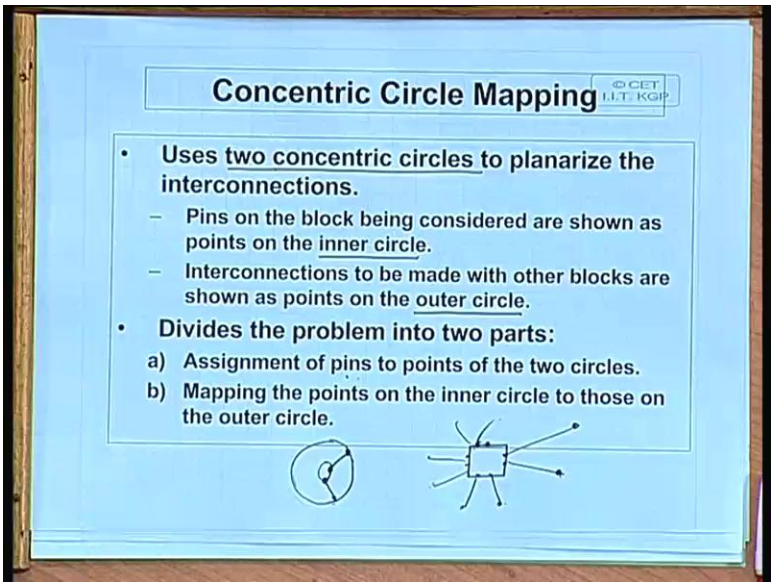

Well the method of concentric circle mapping is simple in concept. This method uses or virtually assumes that there are 2 concentric circles. The objective is to planarize the interconnection means they try to remove the crossings in interconnections if you just imagine it as a graph planarize means they can be laid out on a plane without edges crossing. So it tries to planarize the interconnections as far as possible how. See there is a block with pins on its sides well you are wanting to interconnect this pins to pins of other blocks. So pins on the block being considered this 1 are shown as points of the inner circle I will show with an example. There is a concept of an inner circle. Similarly the points to which you want to make the connections of for the other blocks those are shown as points on another circle that is called the outer circle.

So we will see through that example that the problem is tackled or handled in 2 different paths. First is that with respect to these 2 circles you assign the pins of the inner block as well as to the other pins to which you want to connect to some points on the

circumference of these 2 circles. Number 2 you map a point on this circle to a map to a point on the other circle somehow like this you map them. So these are the 2 steps of the method first you assign the pins to points on the on the circumference of the circles. Then you try to find out the correspondence between the 2 circles ok. So these are whatever I have said is very conceptual let us take an example to understand what I mean. Ok.

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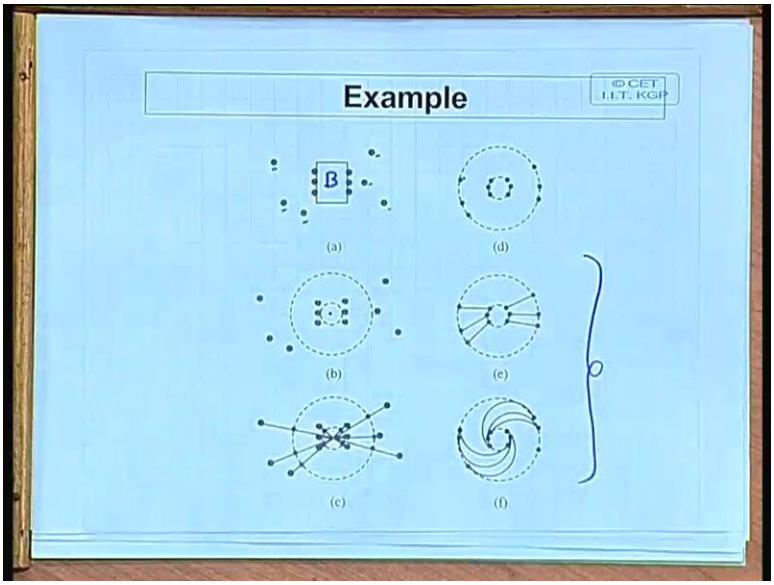

This is an example problem where this is the block B with 6 pins on the boundary. These are the points which may be points of the other blocks are not showing but these pins have to be connected to these 6 points outside. Ok. First thing is that you define 2 imaginary circles the first circle will be just inside the inner pins like this. The second circle will be just inside the outside points this was the nearest point so you define a circle like this. The third step is you take the center of the circle and draw straight lines to all the points of the inner and the outer circles. So these straight lines to the inner points corresponding to the pins of block B will be intersecting the inner circle into these 6 points.

Similarly the lines for the outer points will intersect the outer circle in these 6 points. So now get some points on the inner circle and some points on the outer circle. Now these are 2 possibilities now what they try to do. They try to rotate the inner circle this is the worst case scenario this is the best case scenario. Suppose this is the order in which you want to connect the lines. But if you rotate the inner block then the interconnection will become a little skewed. So you try you just have means this method has an estimate to find out what is the length of the nets if you rotate means what is the orientation of the block that will give you the best interconnection solution.

And in this step also if there is some some concept equipotential or function equivalent pins you can swap them to reduce crossing. So this all this concepts are taken into account in this method. So I am not going details of the implementation algorithm but this is the concept. (()) (38:24) Yes, yes. Possible ok. So this method is conceptually simple and this method tries to make good assignment of the pins so that during the routing did the nets do not cross too much ok. The second modification to this concentric circle mapping is something called topological pin assignment.

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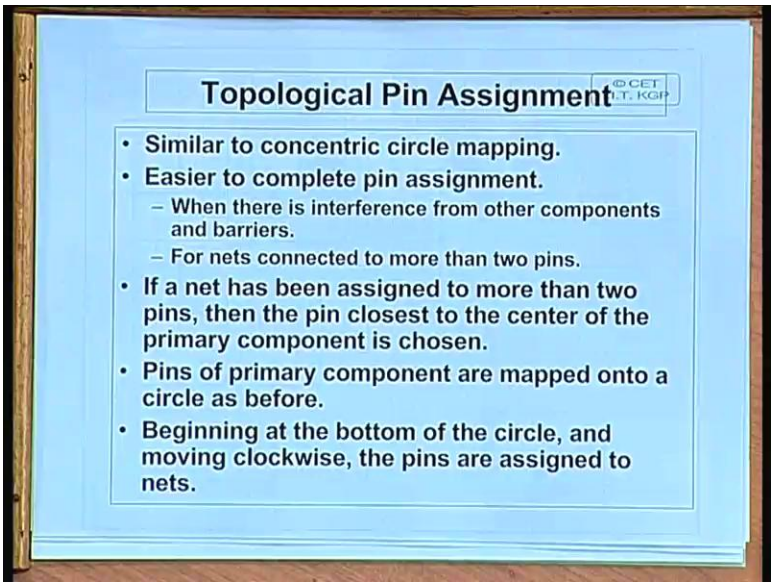

See topological pin assignment is similar. So see in case of concentric circle mapping you are assuming that there are that there are no abstractions in between. When you are trying to interconnect you have finding the shortest distance. But topological pin assignment assumes that there can be some abstractions or interference from other components which can act as barriers. So you will have to go around the barriers for interconnections. So the idea is like this.

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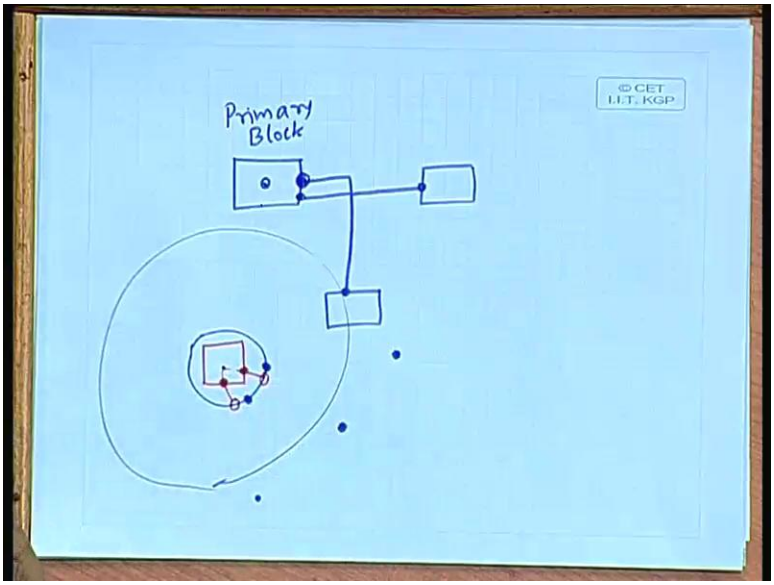

Suppose you have 3 blocks and this method also takes care of nets which can connect more than 1 point. Suppose there is a net like this which must connect 3 points ok. Now the why this method progresses that you identify 1 of 3 these 3 blocks as the primary block. Let us say this 1 you define as the primary block. And this point you assume to be at the center of the primary block. Like you see what he says if a net has been assigned to more than 2 pin then the pin closest to the center of the primary component is chosen ok. This is the primary block and this is the pin closest to it there can be another pin also. For example there can be a pin out here also which also gets connected to the same net. So in that case among this 2 which 1 is the closest you take this this is chosen as the center of this. Now from there a method similar to concentric circle mapping is used.

So again you try to see with respect to this net well this method works with 1 net at a time not with all nets. So you do some kind of a concentric circle mapping you try to do reassignment and find out that how you can configure or if they are flexible to moving the pins. So exactly where should the pin be placed so that the distance with the other pins is minimized? Something like that is I am not go in the detail. So the pins are assigned to the nets in a particular order you say once you have this imaginary circle there can be 1 or 2 pins on the periphery. There will be some other pins outside which you want to connect to it so there will be an outer circle also. So you try to find out an orientation which means that exactly where on this surface, this pin has to loc you can see or you can say that if this pin is moved slightly.

But here and this pin is moved slightly outer here then the total cost gets reduced. There will be a measure of the cost you try to find out the relative position of the pins on this circle which will finally get mapped back into some pin on the boundary ok. So you will say that the pin will be here and the pin will be here. So this topology and mapping and concentric circle mapping are similar but the difference that concentric circle takes all nets at a time. But this takes 1 net at a time and this can handle multi terminal nets. (()) (42:35) Yes. (42:37) Cost is in terms of the total length and the number of net crosses both are taken into account right. Ok in this another approach is proposed.

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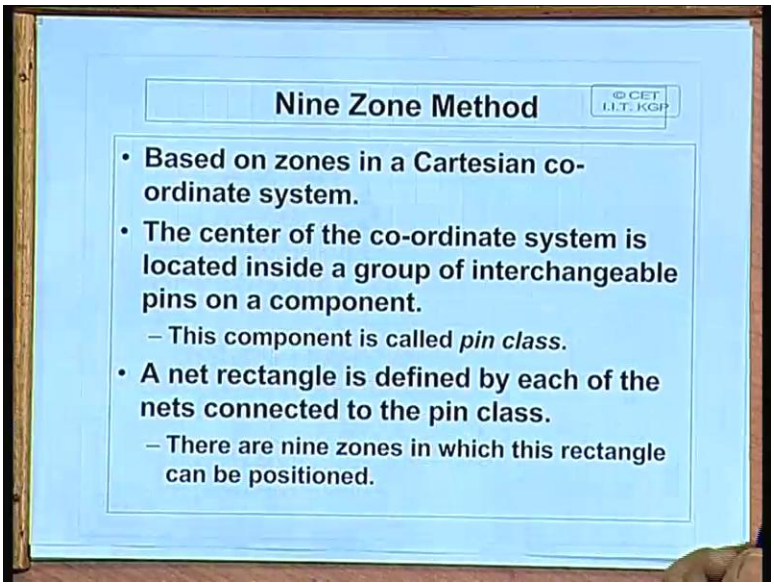

This is based on the concept of zones this is called a 9 zone method it is like this.

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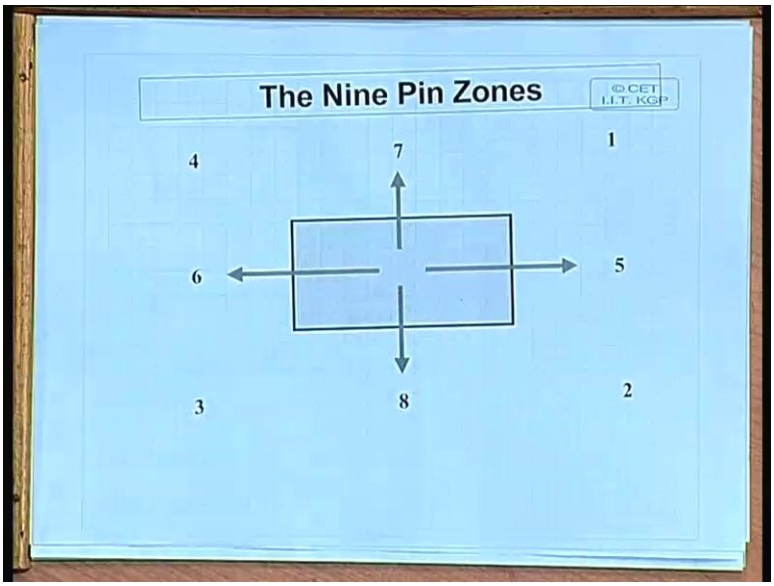

So you have a block this is a block to which some other blocks will have to be connected. You define 9 zone like this 1, 2, 3, 4, 5, 6, 7, 8, 9 is itself. So 8 externally 9 is itself these

are the 9 zones. Now what to do that for each net ok center of the coordinate system is here this is the center of the coordinate system. This component is called the pin class well. The central block which you were choosing this block is called the pin class. Now the concept is like this. Now you take 1 net at a time.

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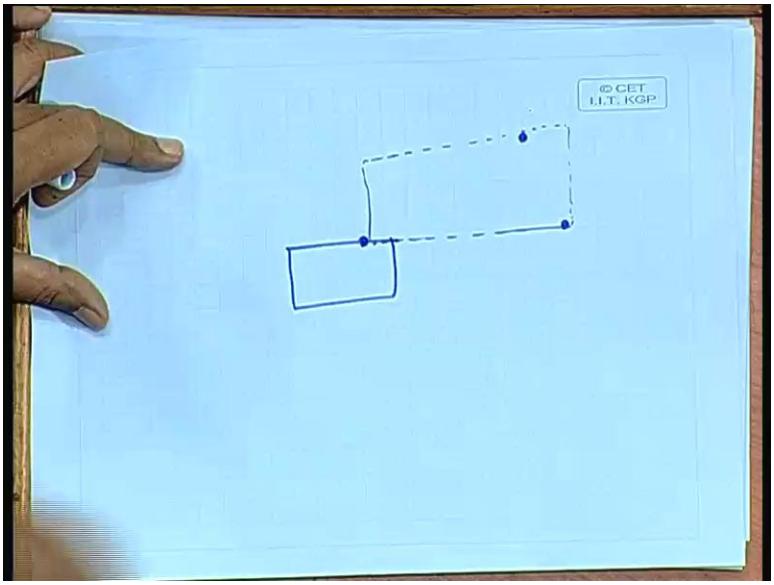

Suppose for this particular block you see that there is 1 net which has to go out from this pin it has to connect this pin and this pin. So you would imagine a rectangular region which will be enclosing this net. Now you try to move around this point so that the area of this rect imaginary rectangle is minimized. And then you try to map it to 1 of these zone which zone this this imaginary rectangle belongs to its essential what you try each net you try to map 1 of these zones and your objective will be to map the different nets to different zones. So that congestion is distributed means uniformly across the zones. So these are indirect method not directly here the individual nets you assume to be in zones you can move around pins to change the areas of the rectangles. Your objective will be to map a rectangle to 1 of the zones.

And you will try and see that more than 1 net, do not fall into the same zone. (()) (45:19) yes (45:23) see I am saying orientation of the block but if the pins are flexible you can as well keep the block fixed and change the pins that means a same. (()) (45:33) yes which is a 1 pin at a time. (()) (45:46) Here this method we are assuming we are going for full custom design the pin definitions are not yet fixed here internally we can make those changes. Because if that ordering is fixed then means you cannot just do much with this playing around. Because the once 1 of the rectangle is fixed the other gates means constraint severely you are right. (()) (46:12) No minimize area is 1 thing that means another thing also you will have to see that the rectangle falls in the 1 of the zones because here everything is mapped into zones (()) (46:27) Conflicting zones absolutely. Somehow you can say some of the rectangle may span 2 zones yes.

Here I am saying suppose we have a pin out here this pin wants to make a connection to an external pin here and external pin here and an external pin here say. So with this points you try to find out an imaginary bounding rectangle say imaginary bounding rectangle will be like this. Now you see that this imaginary boundary rectangle spans zones 1 and 5. Then you see that if I move around this pin can I put this into 1 of the zones or in fa in this example you cannot. So this net has to be mapped or assigned to 2 zones 1 and 5. But if there is flexibility then you can move this around and try to map it into 1 of the zones. Suppose this point was not there and this pin was initially here. Then the rectangle would have been like this big now if you move this point up then it will span only zone one. Like that Fine. So among the specialized method I told you that if you are having a standard cell based design you can have you go you got simpler sub problem which is called channel pin assignment.

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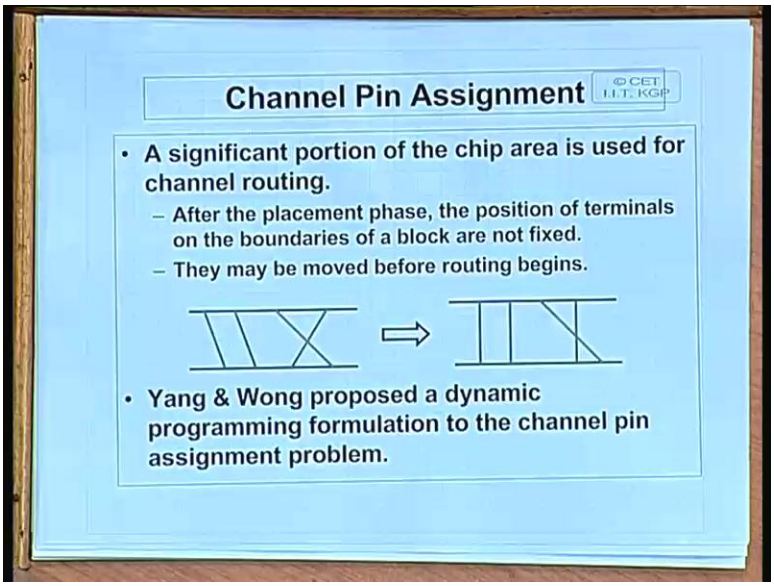

Now a channel is something like this. So we will look into channel in much more detail later when we talk about routing.

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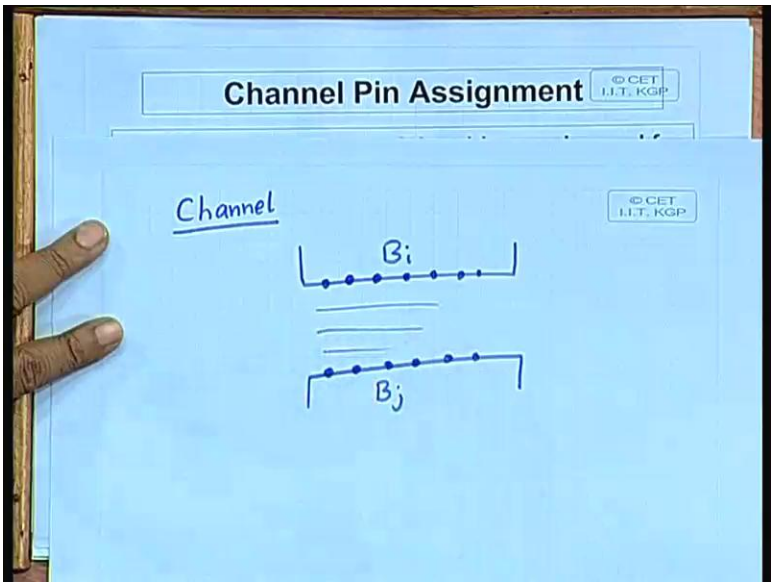

But a channel is something like this there is a block say Bi there is a block Bj there is a rectangular region between the blocks Bi and Bj. And the pins are located above on the surface of Bi on the periphery and below. The objective is to connect some of these pins to some of this pins this is the channel routing problem. So there are pins on the 2 sides of the channel there is a given net list we will have to interconnect them using minimum number of tracks ok fine.

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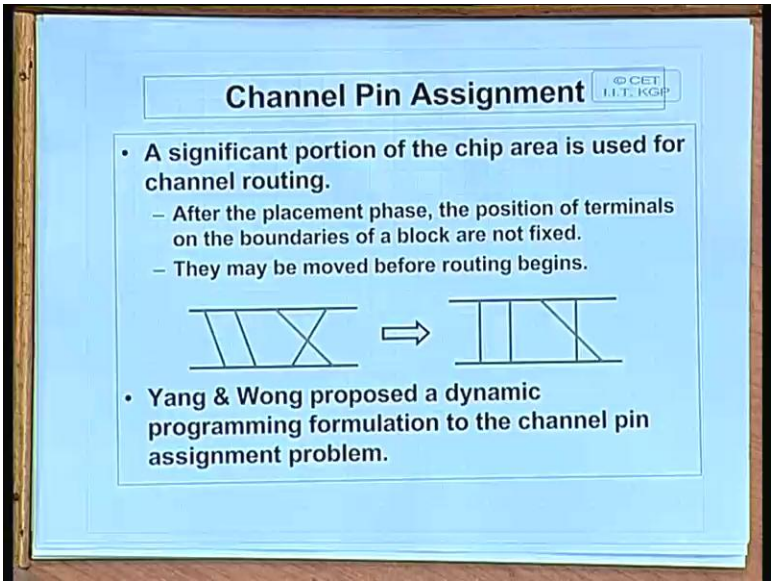

So for channel router pin assignment the problem is that in modern day VLSI design most of the designs are based on standard cell based ones. So we have channels or existences of channels are there in most of the designs. So understanding that channels are a very important part or important you can say important proportion of the routing we have to do. So it will help if you try to do some pin assignment in the channels which will be reducing congestion and the routing areas like in fact there are number of heuristics which are used. Here I am show showing only one.

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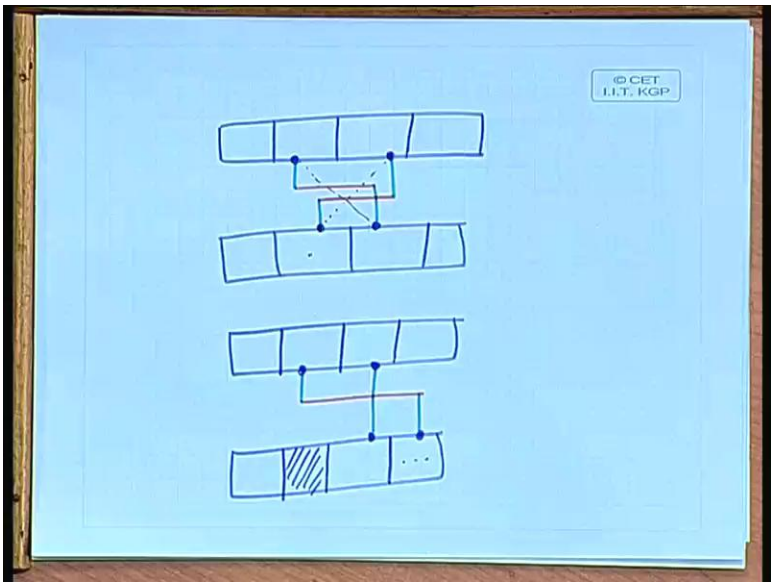

Like for example suppose in a standard cell base design you have 2 rows of cells ok. These are the pre assigned cells on top ad bottom say I am I am having a specific example. Suppose these 2 pins are here and there are there is 1 pin here and 1 pin here. Now your objective will be to connect this with this and this pin with this pin. Now in order to do that you can see that you will be requiring well this interconnections are normally done in 2 different layers. This will be in 1 layer this will be in some other layer this will be in the other layer. Similarly for this interconnection this will be in 1 layer this will be in another layer this.

So for this simple sub problem you see that you are requiring 2 channels or 2 tracks. Since the 2 nets are processing and the span of the 2 nets overlap you cannot do with 1 track. There is a section where both the nets are overlapping you have the 2 defined tracks for them. But suppose I do something like this while in a Steiner design although I have place the blocks 1 after the other I can slightly shift 1 block to the left or right. So I can so means what I can do is that say I will be doing something like this like say I will be aligning any 1 of the nets so that 1 pin is getting just just above the other pin. So may

be I will be shifting which has I am taking the same example say I will be shifting this pins slighter to the right.

So may be I will be having some blank space here or if this blank space come I may be putting some other cell here if I can so I will be shifting this cells slighter to the right ok. So now I will be having a situation where these 2 pins will be coming 1 exactly on top of the other. Say this pin will be here may be just exactly below it I will be having this pin. The other pin will be moving further right. This pin will be here. So now the advantage again is that for this net since there are vertically exactly 1 above the other I can route them in the same layer. And this 1 I can route in only 1 track. Ok.

So I can reduce the number of tracks required for routing if I have scenario like this. So in cases where have flexibility I can use even equipotential or functional equivalent pin to swap and try that if this can be done or even I can shift some blocks around or I can swap some blocks also. So in standard cell based design you have this flexibility. So that this kind of a, you can say some relative pin assignments are done. But 1 thing in this channel pin assignment this is normally done at the time of channel routing itself. It is not that you have first doing pin assignment then you are going for routing it is really difficult to do it separately.

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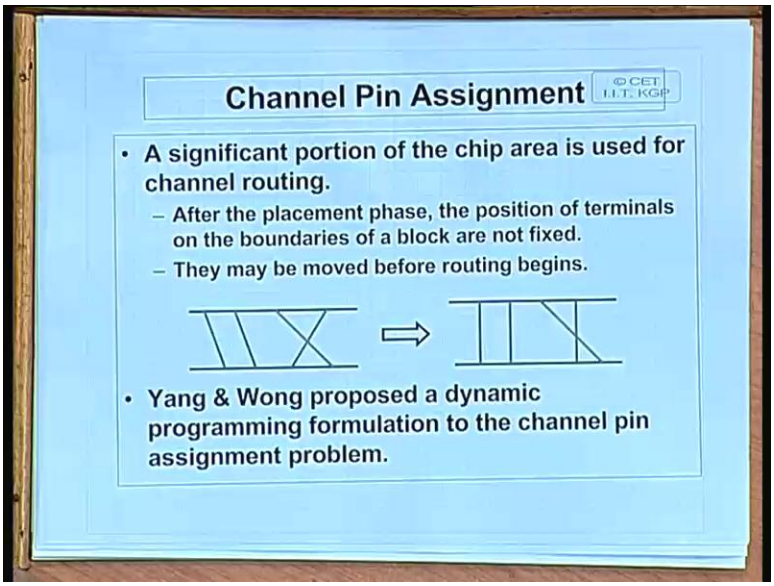

So were although we are saying that this kind of a thing can be done. This will reduce channel congestion everything is fine but this cannot be done in a step which is much before the routing this has to be done along with the routing itself. Ok so we have talked about some algorithms related to floor planning and pin assignments and we will see that subsequently we have some other steps also called first of course is the placement then we will have to go for routing. But we will see that in many situations we may have to go for a integrated approach this again depends on a design cell. For example in the standard cell approach I told you that this pin assignment and routing can go together ok.

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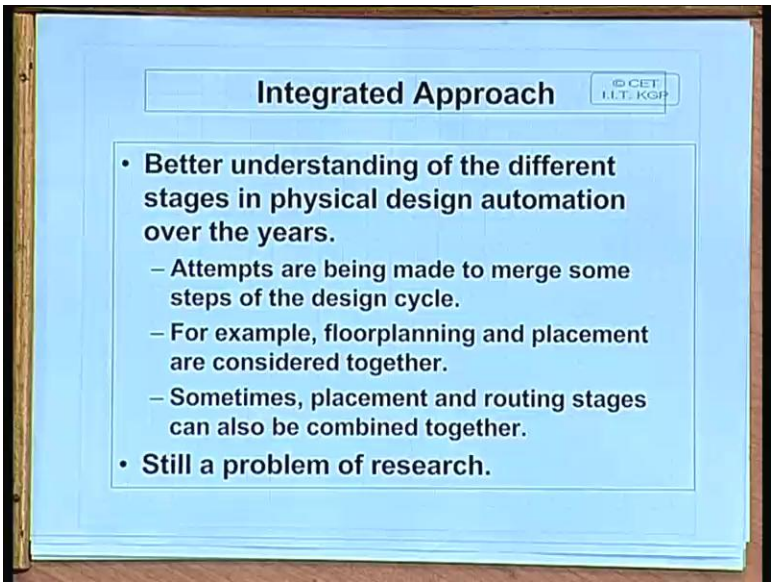

So integrated approach once you understand the different design stages much better you can go for an integrated approach. Like for example floor planning and placement are often merge together nowadays they are not too distinct different steps they go hand in hand. Similarly for some design styles placement and routing can also be combined together it is actually while placing you also do some processing on routing. So that you are interconnection for an interconnection effort later gets reduced of course some estimate is already done during placement. See during placement you have to evaluate something some kind of a cost function so that your routing complexity is less. But since you are already spending some time if you can spend a little more time so that some of the routes also get established then it helps in the later routing steps ok.

So this integrated approach is something which is possibly the best approach but there are a number of unsolved problems still this is a problem of research. So actually such people are stilling working on this these integrated kinds of approaches. (()) (55:42) See even integrated or whatever even in the even in the most modern cad tools available today there often you will have to go back and make some changes you say after laying out you will see that you are power. Some of the parts of the chips will become very hot. That is

consuming power performance that part is consuming lot of power. So we will have to re organize the floor plan again some of the models may be you have to take up to the cooler portion of the chip and they can you will have taken redo a part of it. So this iterative thing will be there. So for a very big design you cannot expect that everything will be done automatically and everything will be fine. So you will have to iterate. Ok so thank you.