Low Power VLSI Circuits and Systems

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Lecture No. # 39

Tutorial – III

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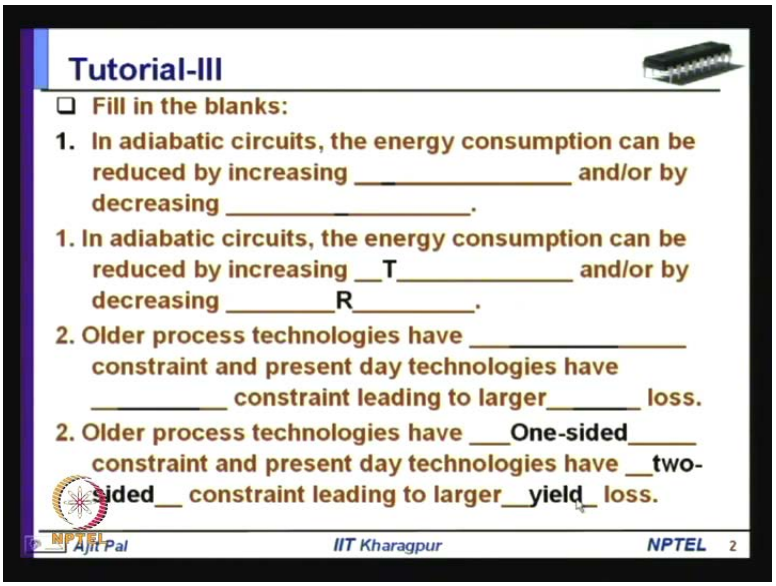

Hello and welcome to today's tutorial. This is the tutorial three, this is based on class test two. Here are some fill in the blanks questions; first question was in adiabatic circuits, the energy consumption can be reduced by increasing dash and or by decreasing dash. So, the answer is in adiabatic circuits, the energy consumption can be reduced by increasing T, that is the time for charging and or by decreasing R that may explain to you, how these two are coming as you know.

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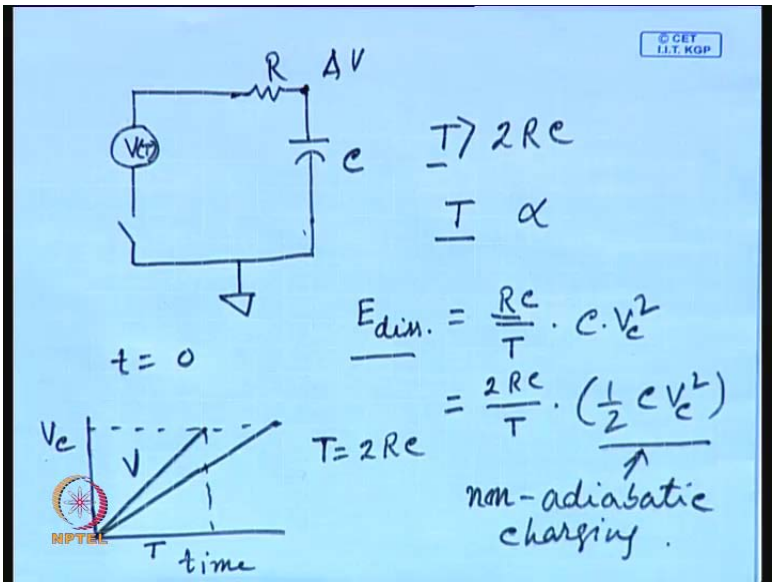

In adiabatic charging you are applying a variable voltage say V T, and through a resistor, and here is a capacitor C and may be you will you will put on switch, and this is counted at time t is equal to 0. We assume that the capacitor in this charge is 0, and after that a voltage I mean time varying voltage is applied and this is the voltage V, and at time t this is a time t, here you have the plot on this in this you have got time. So, in time t it reaches voltage let us assume this is V c, so whenever you charge with the help of this variable voltage what is the energy that is being dissipated in R that can be calculated, and this will be equal to energy dissipated in this capacitor R will be equal to R c by T into CV c square. So that will be the equation that you will get, now this can be rewritten as 2 R c by T into half CV c square, now you note that this is the energy that is being dissipated in non-adiabatic charging. This is adiabatic charging.

Now with respect to this we find that in adiabatic charging whenever you are doing in this way charging with the help of variable which is which varies over time we find that this factor is multiplied by 2 R c by bT, now when t is equal to 2 R c then this this this becomes 1 and obviously the energy that is dissipated for charging the capacitor to to the voltage Vv c c will be equal to half CV square, which is same as non-adiabatic charging. However, when T is greater than 2 R c that means you are you charge over a longer period then what will happen this factor will be smaller that means it should be less than 1.

And obviously the energy that is dissipated will be lesser than the non-adiabatic charging, so I you can you can one way of reducing the power dissipation energy consumption can be reduced by increasing T another possibility is that you can reduce the value of R. So, keeping T reducing the value of R also you can reduce the energy dissipated in the in adiabatic charging, so that is the reason why here is the answer in adiabatic circuits the energy consumption can be reduced by increasing T, and or by decreasing R as I mention by increasing T the power dissipation decreases.

Because the voltage across this resistor reduces whenever you charge it slowly that means the energy dissipated across this resistor is is reduced so if it is it can (( )) increase it can become 0 whenever T is very large, so T is t is infinity than obviously the power dissipation will be small, but however in in real life what you can do you can do you can make T as long as possible, and as a consequence the voltage difference voltage that is applied across the resistor R decreases that means the charge whenever you we keep on charging the voltage here that is being delta V(( )), because of charge accumulation in c will be very close to V c T t. And then as a consequence voltage difference will be delta V and that will be smaller and smaller as you increase T, so that is the reason why by increasing T, you can reduce power dissipation.

Now, second question was older process technologies have dash constraint and present day technologies have dash constraint leading to large dash loss. So, answer is older process technologies have one-sided constraint, and present day technologies have two-sided constraint leading to larger yield loss.

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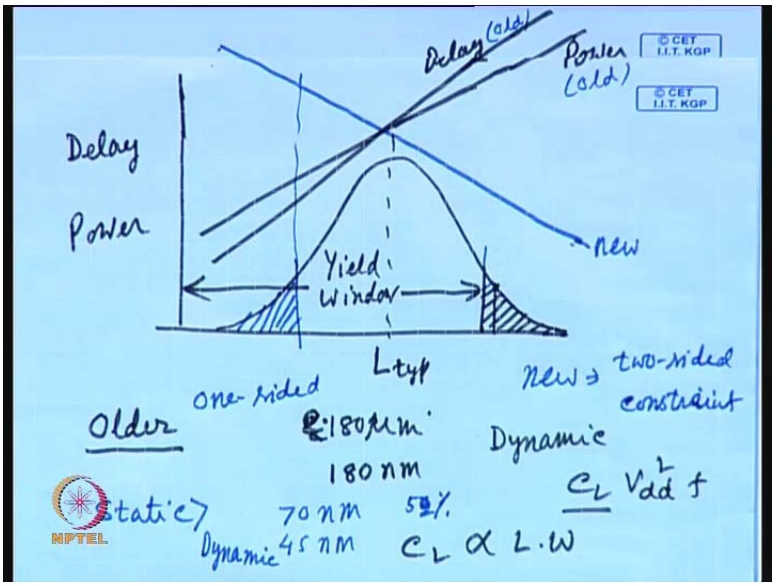

You may recall that because of process parameter variation the channel length varies in this manner, so this is the typical L it say typical and around it it changes, it is it is a random variable and assuming (( )) distribution you can see the the channel length is varying over certain range it is it cannot be considered as a constant. Now as you know in older technologies say less than 180 or you can say greater than sorry greater than 180 micron technology, what was what was happening in whenever sorry 18 micron technology 180 nano-meter technology.

So, whenever the technology was greater than 180 nano-meter then what was the situation, the leakage power was insignificant compared to dynamic power. So, when leakage power is insignificant compared to dynamic power dynamic powers as you know is proportional to C L V d d square f. Now in this whenever you change the channel length when the channel length varies over a range this parameter C L changes, because whenever the channel length is longer obviously the capacitance will be more, because C L is proportional to L into W, so as the length increases the capacitance increases and L as L decreases capacitance decreases. So, the the one sided constant was like this that means the the dynamic power dissipation was increasing like this, this was the dynamic power.

And similarly, delay was also increasing with the channel length, so we can see here the because of this the both channel length I mean both the in on this in this direction, you

will have delay and power so delay increases because of the increasing capacitance so this is your delay, and this was power. Now, if your power (( )) it is exceeded here, and delay was a that means performance is exceeded here than this is the yield window.

This is the yield window that you will get that means the devices which are falling in this range that means for we having channel length have to be discarded, so this is the one sided constraint in older technologies. However, in in the present day technology is say 70 nano-meter or say maybe 45 nano-meter as you know the the static power static power dissipation is greater than dynamic power; that means not only static power is significant, but some it is more than the dynamic power. As you know in 70 nano-meter it is about 52 percent of the total power that means static power dissipation is large. So, in such a case what will happen as the channel length you know decreases.

What happens? The because of V T h role of the threshold voltage decreases that means with the decreasing channel length the threshold voltage decreases, and as the threshold voltage decreases the leakage current increases exponentially. As you know that threshold leakage current is dependent on the threshold voltage, and as a consequence the power is now like this. So, in new technologies, this is the you can say this is old this is also old technologies and this is the new technology. So in this case what is happening because of power budget you can say for delay budget let us assume this is the window. I mean you have to discard, because they are not satisfying the performance, but because of power because of heavy leakage. Let us assume this is the maximum leakage power dissipation or total power dissipation that you can tolerate. So, you find that in this here you have to discard additional devices and or additional devices die, because of the increase power dissipation.

Now, you have got two sided power two sided constraint, so in older technologies it is one sided constraint in new technologies, we find that in the present day technology it is a two sided constraint And because of this constraint two-sided constraint what is happening more dies are to be discarded leading to yield loss, so that is why here old process technologies has one-sided constraint and present day technologies have two-sided constraint leading to large yield loss, so that was the second question.

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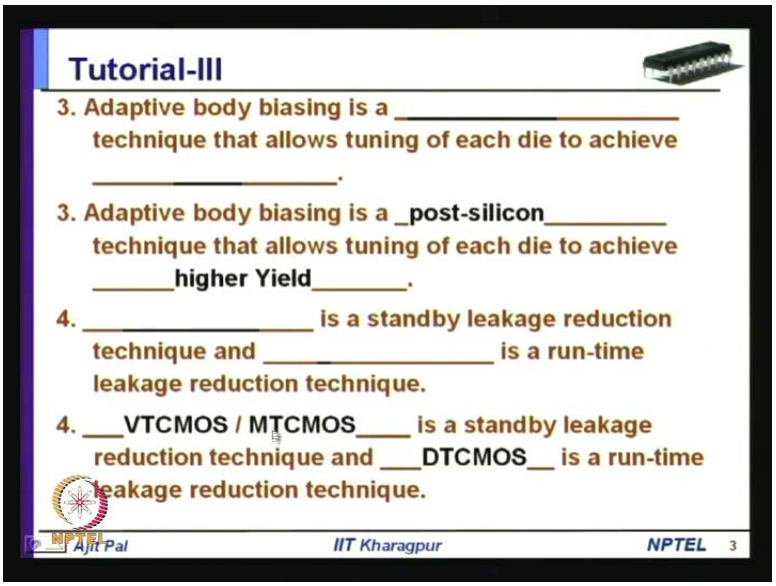

Coming to the third question, adaptive body biasing is a dash technique that allows tuning of each die to achieve dash, so answer is adaptive biasing is a post-silicon technique; that allows tuning of each die to achieve higher yield. So as we know we have discussed several techniques of reducing power dissipation I mean to achieve to achieve higher yield; that means adaptive body biasing is a technique that allows tuning of each each adaptive body biasing is post-silicon technique we have discussed.

We in a lecture on variation tolerant design we discussed some techniques which are post-silicon and some techniques which are pre-silicon, so pre-silicon techniques are essentially designed in using suitable technique, so that the variation is tolerated so you will do do the design in such a way that it will be variation tolerant. On the other hand in post-silicon technique after the fabrication you will do some adjustment that can be done by using by applying different supply voltage or by applying different body bias, so different dies will be applied different body bias.

So the answer is adaptive body biasing is a post-silicon technique and that allows tuning of each die to achieve higher yield, so that was the third question. Forth question was dash is a standby leakage reduction technique, and dash is a run-time leakage reduction technique, so I have discussed many several stand by leakage reduction techniques you you may write any one of them here. So either variable threshold voltage CMOS

VTCMOS, where you can change the threshold voltage by changing the body bias or MTCMOS, where you can do power gating.

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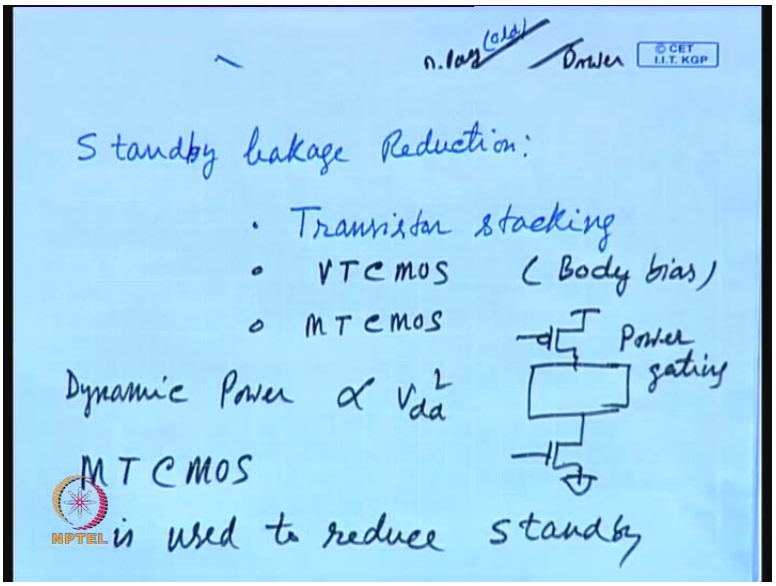

When in the standby condition or you can do transistors striking that means, so for as these standby leakage reduction techniques are concerned, standby leakage reduction technique there are several techniques; one is transistor stacking or which is cell biasing as you know if you apply different input combination to a combination circuit when the transistors are in series, because of cell bias where a particular input voltage there is reduction in leakage power, that is the transistor stacking. So, you can you could have you you can write transistor or VTCMOS variable threshold voltage CMOS in which the threshold voltage is varies by changing the body bias.

And third technique that was discussed is MT CMOS multi threshold voltage CMOS where you can use multiple threshold voltage in series that you may recall, so this is the actual circuit, and you can put transistor either in the as header or footer to reduce leakage current so this is also known as power gating. So you can use any one of the three, any one of the three techniques here VTCMOS or MTCMOS or transistor stacking. And similarly, for run-time leakage reduction leakage technique the most common approach is DTCMOS, where dual threshold voltage CMOS is used that means transistors some transistors are which are on the the gates which are on the critical path.

Those gates are realized with lower threshold voltage and gates which are on non-critical path they are realized by using higher threshold voltage, so VTCMOS is one of the run-time leakage reduction techniques, and so this is this is the answer you can give.

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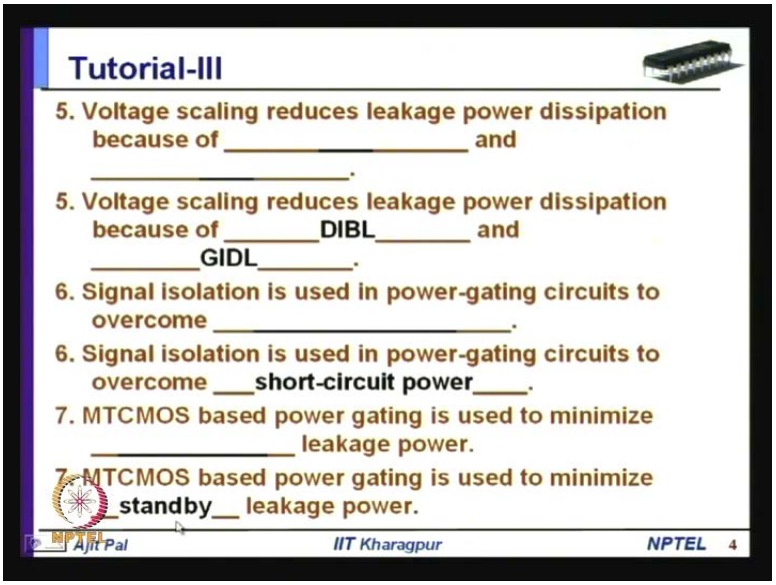

Then question five was voltage scaling reduces leakage power dissipation, because of dash and dash you may you may remember that voltage scaling is commonly used for dynamic power for reducing the dynamic power, because you know that dynamic power is is proportional to V d d square, but you can say there is a side effect side - effect is that. If you reduce V d d by several techniques it can be static voltage scaling or it can be dynamic voltage scaling whatever you do as you reduce the supply voltage the leakage power reduces, because of two factors one is your drain induce barrir lowering, so when the drain voltage is reduced the barrier is lowered barrier lowering occurs, and as a consequence the the the supply voltage is reduced. So the the barrier is higher and as a consequence you know the leakage current is lesser that means threshold voltage is larger; similarly, GIDL effect that is your gate induce drain leakage that also reduce effects the voltage scaling, and for larger voltage the leakage current due to GIDL effect is more and for smaller voltage is this.

So, because of these two effects you know as you do voltage scaling; there is leakage power reduction. Then coming to six question signal isolation is used in power gating

circuit to overcome dash, the answer is signal isolation is used in power gating circuit to overcome shirt circuit power.

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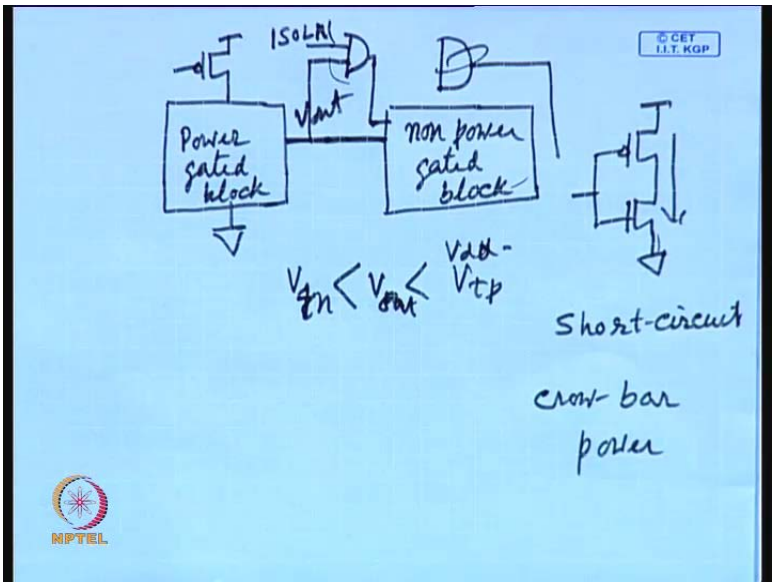

You may recall that so whenever you are using say multiple voltage domain in a circuits, let us assume this is a power gated block, so this is this is a power gated power gated block. So, since this is power gated block the output voltage that is that is generated here, it can be either 0 or V dd but for example, if you use say header switch then the than the voltage will be as you turn it off voltage should come down to 0.

But it may not turn down to 0 because of various reasons, because of the leakage power of this part, because of leakage power of this part even when it is switched off; there is some leakage that will flow through, it as a result there will be a voltage that will be generated here. So, the this output goes to a non-power gated block this is non-power gated block, then what happens if this voltage is greater than V v t n is greater than V t n and less than V t p V d d minus V t p, then what happens? If it is greater than this that means V in that V out you can say here V out is greater than V t n, but less than V d d minus V t p then what will happen in this part of the circuit?

There will be short circuit power as you know for example, in case of an inverter if the voltage is input voltage is greater than V t n this transistor is on, and if the voltage is less than V d d minus V t p this transistor is also on, and as a result both the transistors will be on leading to short-circuit power or crow-bar power. So, this this this this is the

situation, and that is the reason why this this output is isolated with the help of suitable hardware So, you will put an put an AND-gate here this output will be sorry you will put an AND-gate here, this this will go there and this will come here. And isolation signal signal will be applied here, so that whenever this isolated this will be this will be climbed to low level, so that it does not disturb this part of the circuit; that means this is low this will be low. So, this gate of course, has to be it should get always AND-gate should not should not be power-gated.

So, this is how it can be done, so signal isolation is used in power gating circuit to overcome short circuit power, so signal isolation can be done with the help of AND-gate or OR gate or some other hardware as I have already discussed in detail. Coming to question seven MTCMOS based power gating is used to minimize dash leakage power, so as you know MTCMOS based I have already discussed MTCMOS based power gating is used to minimize standby leakage power, MTCMOS based power gating is essentially is essentially you are putting high V d transistors in series.

So, you will be applying sleep-control signal here, and that will and when the circuit is in standby than these transistors are off and as a consequence leakage power will be less. So, you can say this MTCMOS is used to reduce standby leakage power, so MTCMOS based power gating is used to minimize standby leakage power.

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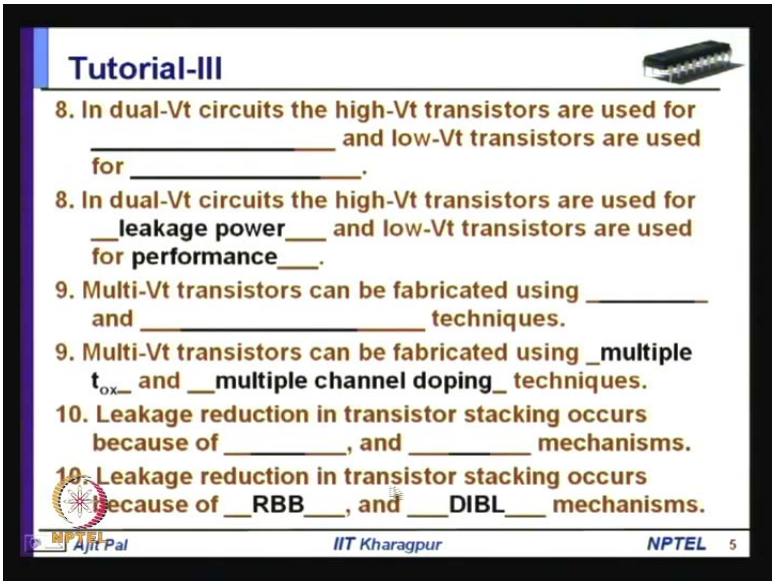

So, coming to question numbers eight in dual Vt circuit the high Vt transistors are use for dash, and low Vt transistors are used for dash, so I have already discussed about VTCMOS as you know in dual Vt circuits, high Vt transistors are used for leakage power. That means in a multilevel multi inputs circuits, you have got many gates and a larger portion them are in are in non-critical path, so the gates which are on the non-critical path you can use you can use high threshold voltage transistor to realize them.

So that will reduce the leakage power, so high Vt transistors are used to leakage power, on the other hand the gates on the critical path that to be realized by using low Vt transistors, so that performance is maintained. So you can say high Vt transistors are used for leakage power for other to reduce leakage power, and low Vd transistors are used for performance higher performance; so lower leakage power and higher performance you can see. Coming to question number nine multi V t transistors can be fabricated using dash and dash techniques. I have discussed several techniques by which you can realize multi V circuits; that means transistors with multiple threshold voltages.

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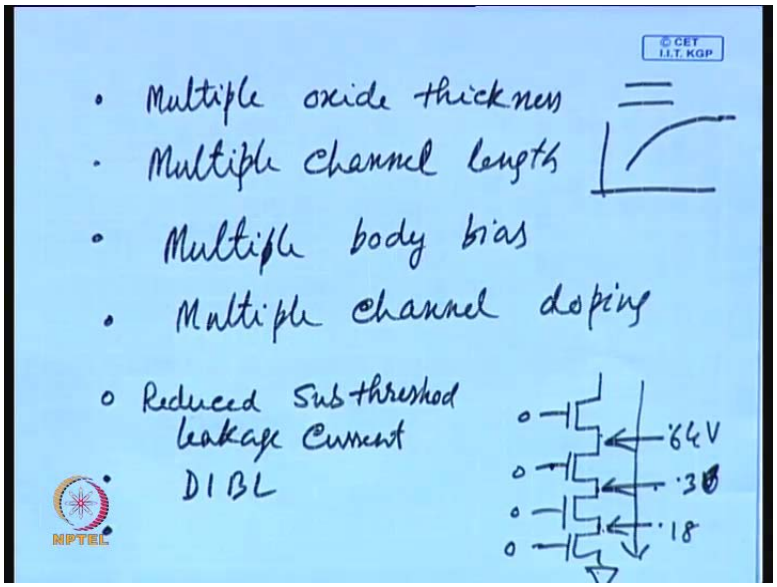

So, the the various techniques are number one is multiple oxide thickness, it can be multiple channel length you can use multiple body bias, so there are these are some of the techniques that I mention. And also you can do multiple channel doping, so I have discussed how these techniques can be used and how the threshold voltage varies as you

realize transistors with different silicon di-oxide thickness; that means the width of the silicon di-oxide layer, and the in realizing transistors similarly, multiple channel length.

I have already mention that smaller the channel length larger is the threshold voltage smaller is the threshold voltage; that means, because of V t h role of… So as the as the channel length reduces threshold voltage decreases, so multiple channel length can be used to realized threshed multiple threshold voltage. Similarly, multiple bias can be used to realize transistors of different threshold voltages; similarly, multiple channel doping.

So you can write any one of the two, any two of the four; so multiple t oxide that means multiple silicon di-oxide thickness or multiple channel length I have channel doping I have written, but you can write any two of the four techniques that I mentioned. Then question number ten is leakage reduction in transistor stacking occurs, because of dash and dash mechanisms.

You may recall that whenever you do transistors stacking like this, say several transistors are in series say and depending on which of these are on and off the leakage current varies. For example, you have applied 0 0 0 0 voltage 0 level voltage, and now some leakage current will flow and as a result some voltages may be say 0.18 here, and may be 0.36 volt here, and some some other voltage here may be 6.64 volt here.

So, as you can see some positive voltages are developed as the source point, and this leads to reduction in leakage current, because of three mechanisms - number one is as you know since the source voltage is positive, and gate voltage is negative you know gate is reverse bias. And as you know whenever you reverse bias gate with respect to source, this reduces threshold leakage current. So, reduced sub threshold leakage current.

Second is the voltage across this transistor is small as a result you know, because of that DIBL effect, because of smaller voltage across the transistors, and smaller smaller drain voltage that DIBL component of leakage current will be smaller whenever you do this transistors stacking. And third reason for reduction is because of reverse body biasing, so reverse body biasing is will will lead to smaller threshold voltages I mean larger threshold voltages, and as a consequence the the leakage current will be smaller, so you can write any one of the three.

I have written reverse body bias and DIBL, so any one of the three techniques; it also reduces threshold leakage current. So, you can write any two any any two from the three mechanisms; that is responsible for leakage current reduction in transistor stacking.

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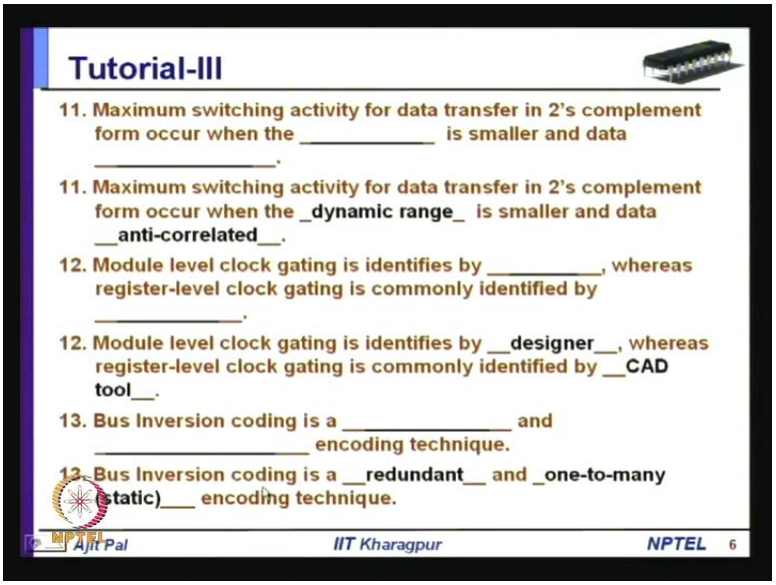

Coming to 11 maximum switching activity for data transfer in 2's complement form occurs when dash is smaller and data dash. You may recall that there are 2 parameters dynamic range, and correlation factor; these 2 parameters are responsible for you know reduction in reduction in dynamic power, so because of reduction in switching activity.

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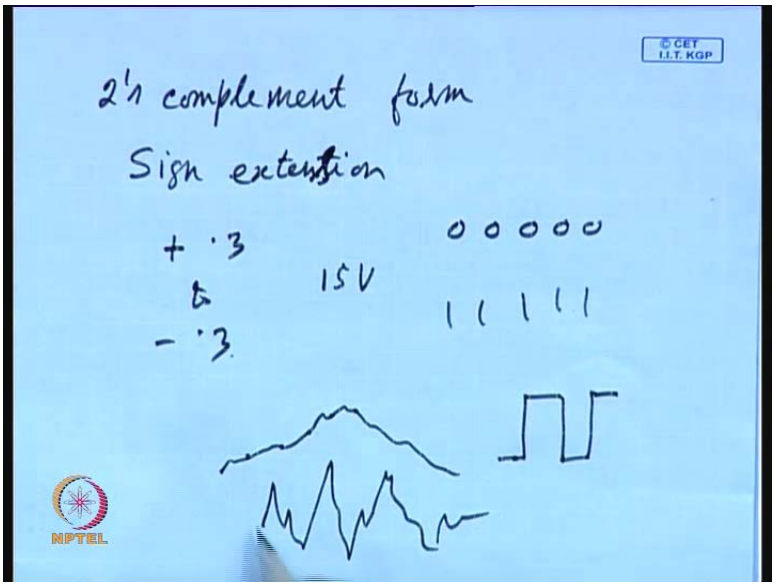

So, when the dynamic range is small as you know, because of a you know in 2's complement form what happens that sign extension occurs, because of sign extension. You know as the suppose it changes from plus 0.3 volt to minus 0.3 volt, and dynamic range is say 15 volt then what will happen? The most of the motion it can beats in this case for positive these are 0, and for negative it is 1.

And as a consequence the there will be lot of switching activity, so when the dynamic range is small and the sign changes in 2's complement form that leads to larger switching activity. Similarly, correlation factor because of correlation factor the switching activity changes; for example, if the input changes slowly increases or decreases than the the consecutive data are anti co-related sorry, co-related as a consequence this switching activity will be less. On the other hand, if the if it changes from negative it goes become positive than it becomes negative, and again it becomes positive. So it is highly anti-correlated, so in in this case again lot of changes will occur or if you can say if it changes very quickly than data is anti-correlated, so in these two situations that means when the dynamic range is small. And data is anti-correlated this switching activity maximum switching activity occurs using 2's complement form, and as I mention these can be reduced by using sign magnitude representation of data when you send it over (( )). Question number 12 was module level clock gating is identified by dash, whereas register-level clock gating is commonly identified by dash.

You may recall that these whenever you are using power gating you can either use some automated CAD tool, but the whenever the module level clock gating is done, I mean here it is clock gating not power gating the clock gating is done in module level say a l u then say transmitter receiver when they will be off; these are usually identified by the user; that means module level clock gating is identified by the user or the designer. On the other hand when the clock gating is automated clock gating tools are used massively clock gating techniques are available nowadays where CAD tool does.

The clock gating automatic insertion of clock gating hardware in the circuit in such a case the CAD tool does sorry, clock gating that is the reason why the answer is module level clock gating is identified by the designer; whereas, register-level clock gating is commonly identified by CAD tool. Coming to question number 13 bus inversion coding is dash and dash encoding technique you may recall that.

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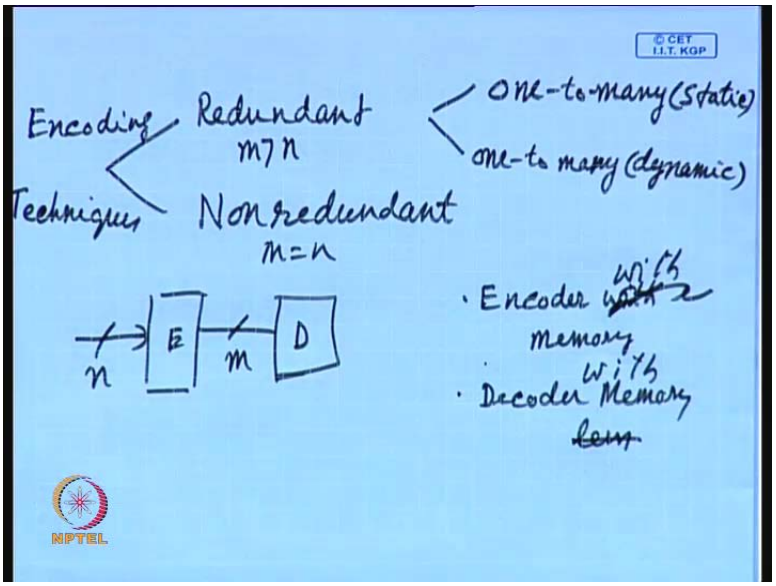

There are several ways by which the coding techniques can be categorized one is your one category is redundant another is non-redundant. Then whenever you are using redundant encoding there are two alternatives one is your one-to-many static or it can be one-to-many dynamic, so these are encoding techniques. Redundant means the whenever you are sending here is you Encoder and here is your Decoder, so to the encoder say n beats are applied, and it generates m beats when m i greater than n than it is redundant and as you know when m is equal to n than it is non-redundant.

So, when known number of additional beats are used it is redundant technique, and there you can have two possibilities: in the first case you know you have got Encoder and Decoder; Encoder with memory, Encoder with memory, and decoder memory less this is a situation one-to-many static. That means in a Encoder you will be using memory, and Decoder will not require any memory, and that is the situation in bus inversion and coding, so it is a redundant and one-to-many static and coding technique.

In the other hand, you may require both I mean Encoder and Decoder may have memory; that means both will be with memory sorry, this is the Encoder with memory and Decoder also with memory. In such a case we call it one-to-many dynamic; that means when Encoder with memory and Decoder with memory it is one-to-many, and as you know I discussed t 0 encoding in to encoding you may recall that memory is required in implementing the encoder as well as the Decoder.

So, it is a one-to-many dynamic technique but so far as this particular technique is concerned bus inversion coding is concerned it is a redundant, and one-to-many static encoding technique.

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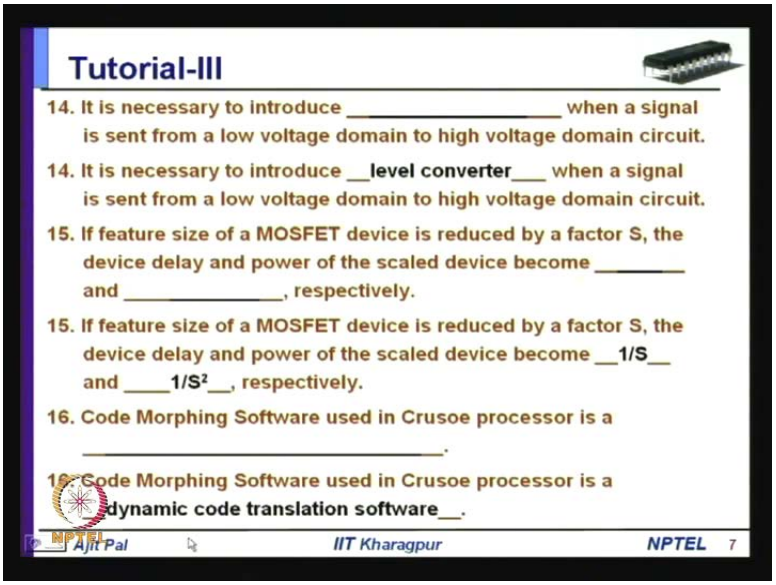

So, coming to question number 4, it is necessary to introduce dash when a signal is sent from a low voltage to high voltage domain circuit, so it is necessary to introduce level converter when a signal is sent from a low voltage domain to high voltage domain circuit.

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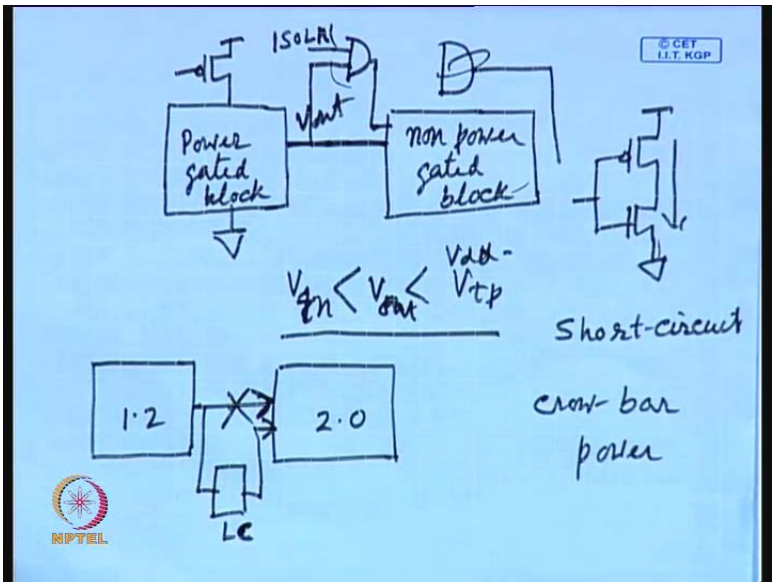

So, reason is same as reason is same as you know whenever signal is passing from I discussed about techniques where you know you have got say 2 voltage domains so this is your low voltage domain say may be say 1.2, and it is going to another voltage domain and here let us assume the voltage is 2.0. So, whenever a signal low voltage domain signal goes from low voltage to high voltage domain. What happens? This voltage will be… There is a possibility that output level voltage will be in this range, it will be less that means V out will be greater than V t n, and less than V d d minus t p, and that will lead to you know short circuit power dissipation in this part of this circuit, so to avoid that you will be introducing level converter l c. And that will be feedback instead of directly applying, so you will be using level converter which will raise the level to high level; there is the low level to high level as the signal goes from low voltage domain to high voltage domain.

So the answer is you have to introduce level converter, when a signal is sent from a low voltage domain and high voltage domain circuit. Question number 15, if feature size of MOSFET device is reduced by a factor s, the device delay and power of the scaled device become dash and dash respectively answer is if feature size of a MOSFET device is reduced by a factor S, the the device delay and power of the scaled device becomes 1 by S, 1 by S you know this. This occurs, because you know you are reducing both three parameters you are reducing one is length, second is width and third is silicon di-oxide thickness.

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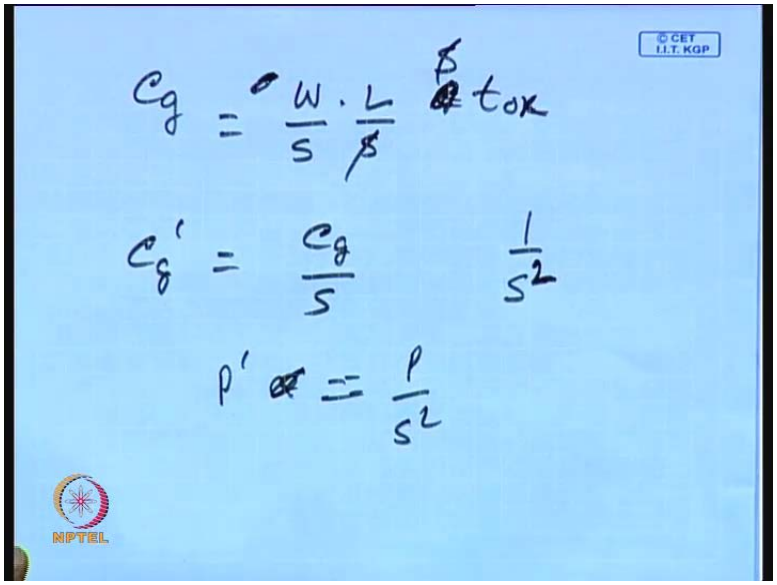

And as you increase the width and that capacitance c g is proportional to as depended on three parameters W L and C g sorry that t o o x, and actually t o o x will influence in different way than W and L, so as you increase W and L I mean reduce W L s. It will be W by S, and it will be l by s on the other hand as you reduce this silicon di-oxide thickness what happens the capacitance increases, so here the parameter will be multiplied by S. So, effectively gate capacitance will be C g dash will be equal to C g by S, and as a consequence the delay will reduced by factor S, and and the so far as power dissipation is concerned it will be proportional to 1 by S square, because you know the the the because of the reduction in voltage the, and that will also reduce it will also reduce the drain current, because of reduction in voltage as well as reduction in drain current the power dissipation P; power dissipation is is equal to P by c square reduces by a factor of S square.

So, I have discussed it in detail. Coming to question number 16, code morphing software used in Crusoe processor is dash essentially, it is a dynamic code translation software as you know that code code morphine software translates from one one instruction. You know one type of instruction of a processor to a another type of instruction set, so from say that you are using; for example, your Pentium processors which are essentially realized by using superscalar technique on the other hand that v l i w technique is used in realizing Crusoe processor; so instruction say instruction.

You know architecture to another instruction architecture it does the translation, and that is why it is called dynamic code translation software essentially translates code from one type of processor to another type of processor, so it is a Dynamic Code Translation software.

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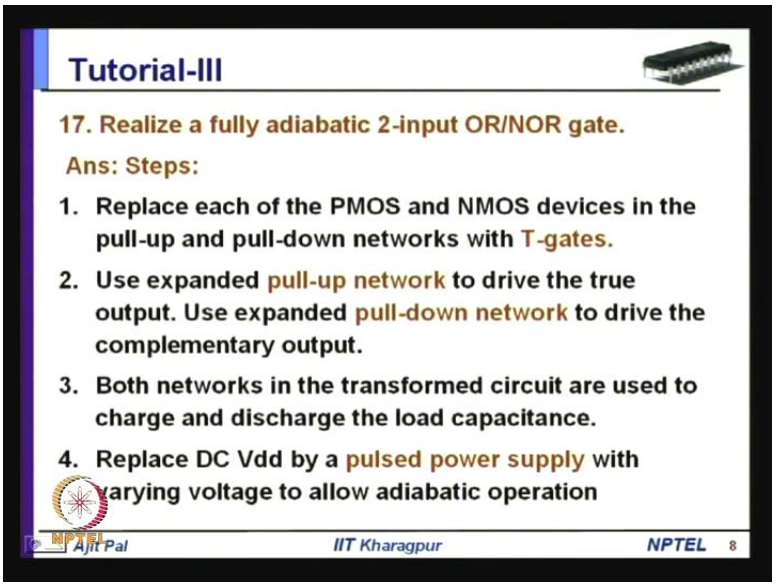

Coming to question number 17 realize a fully adiabatic 2 input and or gate. I discussed about the steps that you have to follow in realizing a in converting a non-adiabatic gate to a adiabatic gate, first thing to be done replace each of the PMOS and NMOS devices in the pull-up, and pull down network with t-gates, second is use expanded pull-up network to drive the true output, and use expanded pull-down network to drive the complementary output. Third is both networks of the transform circuits are used to charge and discharge the load capacitance, and forth is replace d c vdd by a pulsed power supply with varying voltage to allow adiabatic operation.

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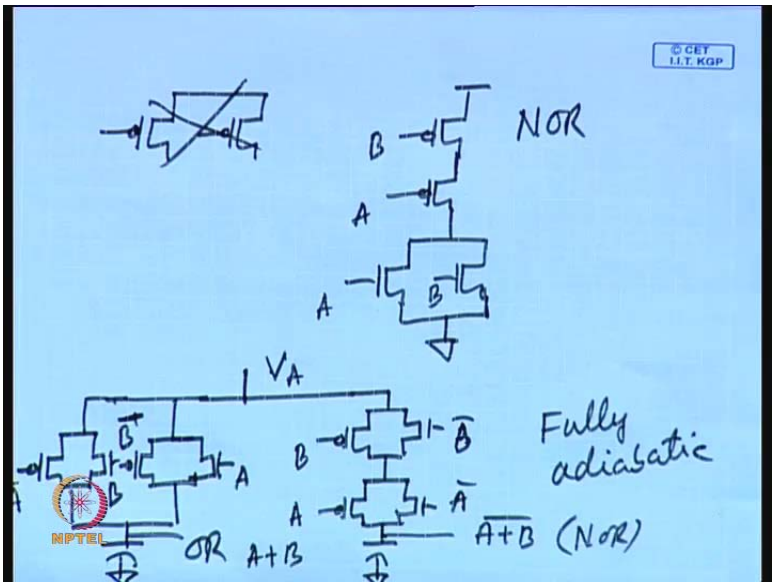

So, let us consider two-input or/nor gate. So non-adiabatic two-input nor gate is realized in this way, so you will require to… So, this is a this is (( )), so this is not (( )), so it will be this is the nor gate two-input nor gate that is realized by using non-adiabatic technique. So, you have to convert it say here you apply A and B, and you can apply A and B, so this is the nor gate that you can realize when on a (( )).

You have to convert it into adiabatic circuit, so you have to replace each of these transistor by a transmission gate, so what you will do say let us consider this part, so here you have got 2 PMOS transistors in series. So you will put two transmission gates in series and this will drive a capacitance and what will be the inputs. So, here you have applied a and b, so will be A and B, and here will be B bar and A bar and here you will get nor output nor that means A or B bar, now then you will realize this part.

You have consider the this part now, you shall consider the pull-down network; so pull-down network two are in parallel, so you will require two transmission gates in parallel two transmission gates in parallel. And that will drive the output capacitance, so here you will get or and what will be the inputs A and B will be here A, and B here will be A bar and B bar. So and finally, here the last step is you will be applying pulse power supply that means you have to apply (( )) supply you are realizing or that means A plus B and this is realizing nor A plus B bar, so this is how you can convert any gate CMOS gate to a fully adiabatic gate. This is fully adiabatic gate, because it it does fully adiabatic charging and discharging with the help of this pulse power supply. You will have dual output NOR and OR or and how it can realized I have explained.

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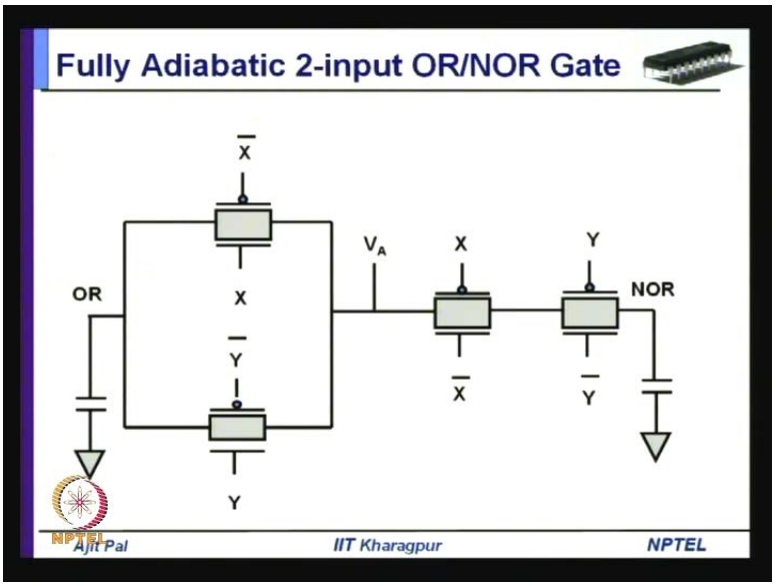

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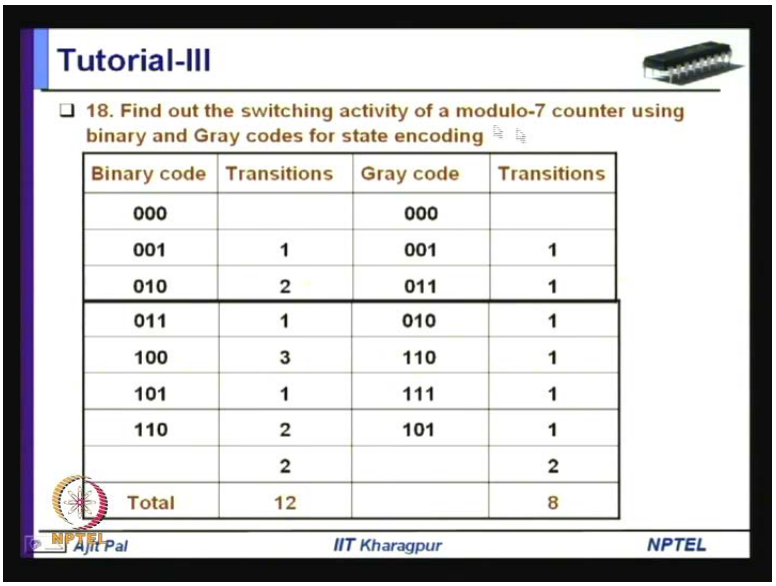

Binary code	Transitions	Gray code	Transitions
000		000	
001	1	001	1
010	2	011	1
011	1	010	1
100	3	110	1
101	1	111	1
110	2	101	1
	2		2
Total	12		8

So this is the realization. Coming to question number 18, find out the switching activity of a module modulo-7 counter using binary, and gray codes for state encoding, so this is the binary code this is the binary code, and this is the gray code so you can see here in a in a counter the transition occurs.

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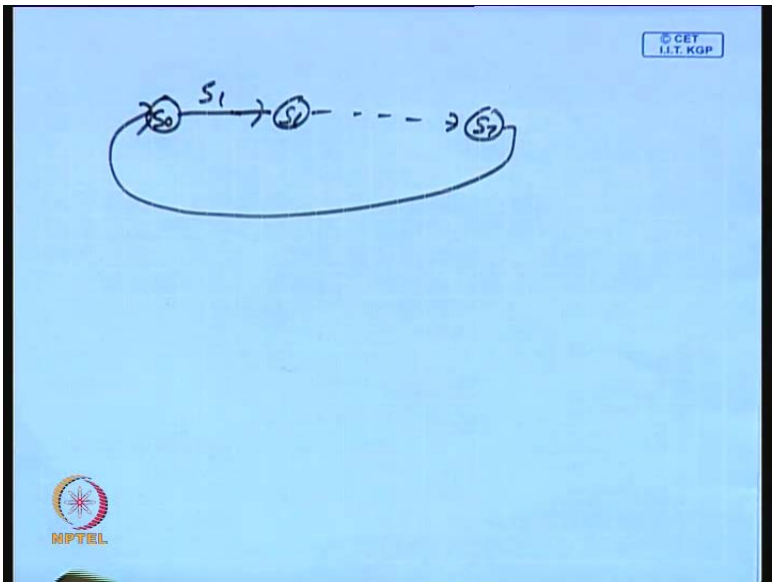

I mean it will go from say S 0 to S 1, then and in this way it will go to S 7, and again it will come back to S 0, so this is how the counter occurs I mean operates, so you can it will the various states are if you use binary coding s 0 is 0 0 0 S 1 is 0 0 1 and 0 1 0 and so on.

So you have it has got seven steps, because of seven codes and whenever it goes from 0 0 0 to 0 0 1 say transition is one whenever it goes from 0 0 1 to 0 1 0 transition is 2 beats, because 2 beats are changing and from 0 1 0 to 0 1 1, 1 beat changing and from 0 1 1 to 1 0 0, 3 beat changing and from 1 0 0 to 1 0 1, 1 beat changing and from 1 0 1 to 1 1 0, 2 beat changing. And whenever it goes from 1 1 1 0 to 0 0 0 2 beat changing, so number of transaction is 12

On the other hand, if you do gray coding the codes are 0 0 1 0 0 0 0 0 0 0 1 0 1 1 then 0 1 0 than 1 1 0 1 1 1 and 1 0 1, and you can see for this 6 from these transitions the only 1 beat will change 0 0 0 to 0 0 1 1 beat 0 0 1 to 0 1 1. Another beat change and from 011 to 0111 beat change, so there will be 6 1 beat changes will occur however whenever it goes form states 7 to state 1, so 1101 to 000 there will be 2 beat changes. So, total number of transitions is 8, so you can see how the switching activity changes in modulo 7 counter for the 2 cases binary code and gray code.

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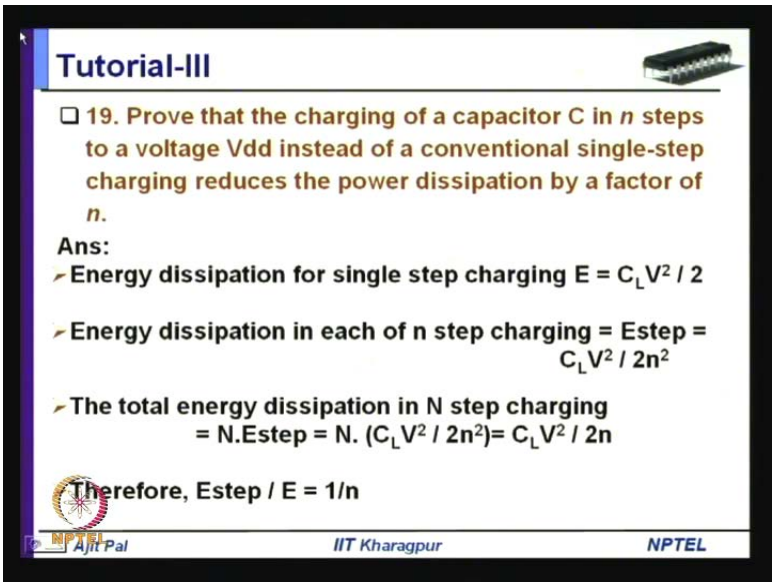

Then the question was question number 19 was prove that the charging of a capacitor C in n steps to a voltage V d d instead of a conventional single-step charging reduces the power dissipation by a factor of n, so whenever the charging is done in 1 step. As you know the power energy that is dissipated is C LV v square by 2 where V is the voltage and as you do n-step charging and obviously, which step the voltage charges from in the first step from 0 to V by n in the second step V by n to I mean stepwise it will keep on doing. So, you can see here energy dissipation in each step of charging will be C L V square by 2 n square because the voltage here is V by n, so C L by 2 into V by n square, so that gives you C L V square by 2 n square, so that gives you C L V square by 2-n square. So, this is for each step of charging now, you will require n steps are charging so the n into E step.

That will be equal to C L V square by 2 n, and if you compare with the first case 1 that means the first situation 1 step charging E step by E is equal to1 by n, now let me consider some other questions. So, there are several questions you have given. So, one of the questions were adiabatic logic circuits operations. I have already discuss that adiabatic logic circuits and another question was the normalized delay sizing how the delay changes with sizing factor, so let me answer the questions which can be discussed in this short time.

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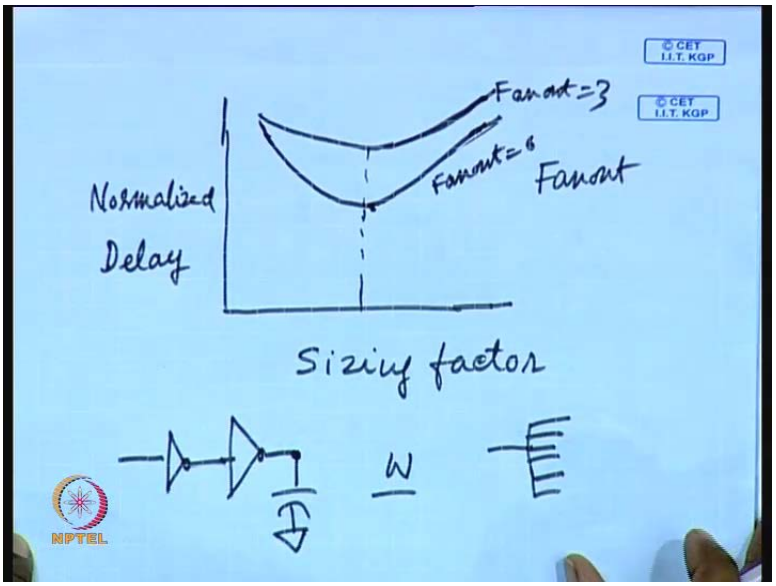

One question was this is the sizing factor, and this is the normalized delay. What do you really mean by sizing? Sizing means you are increasingly, you are increasing the size of the transistors.

How you are increasing the size obviously by increasing W by increasing W you are increasing the size of the transistors, and how the delay changes as you increase the fan out. That means there is a relationship between fan out and sizing factor, so when the fan out is small, so when the fan out is small the delay with sizing factor changes this way; that means, initially as you increase the size the delay reduces, but after sometime delay does not you know as you increase the fan out delay increases.

The reason for that is as you increase this size you know there are two things, you are driving an say inverter of a larger size now if this capacitance is large, if this capacitance is large - the the capacitance delay will reduce, if you increase the size of this transistor but you know that as you increase the size of this transistor the capacitance of this also increases and as the capacitance of this increases there will be large delay for this side.

That means that is the reason, why for a given capacitance if there is an optimal value of size and beyond that it will increase because driving the capacitance is increasing of this that will lead to larger delay here, so there is a optimal size for which it will get minimum delay, and beyond that as you if you increasing in sizing factor then delay will increase. Now, that will be dependent on the fan out fan out means different value of

capacitance, if the capacitance is small than the the effect of sizing is small that means reduction in delay is smaller when the capacitance is small, and reduction in delay will be larger whenever this capacitance is larger. So when this that means here fan out is 6, and here say fan out is equal to there; that means when the fan out is smaller that means this capacitance is smaller fan out means you know that it is driving lesser number of gates when the fan out is equal to 3, and whenever you are driving more number of gates than fan out is more.

So, capacitance is more when the fan out is more and that sizing will have more impact on delay, when the fan out is more and when the fan out is less it has lesser impact. However, again there is an optimal sizing factor beyond which delay will increase in both the cases, so that is what I explain. So, I believe the other questions we can take up in the normal class, and we can discuss in detail. So, with this let us conclude this tutorial 3, and you can take up other questions in our normal class. Thank u