Low Power VLSI Circuits and Systems

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Lecture No. # 38

CAD Tools for Low Power

Hello, and welcome to the last lecture of this lecture series. This lecture is on CAD tools for low power.

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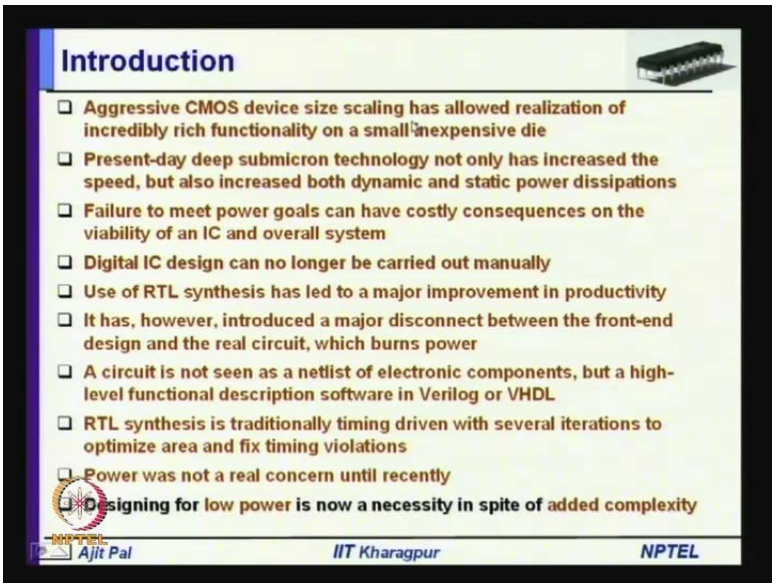

We know that, aggressive CMOS device size scaling has allowed realization of incredibly rich functionality on a small inexpensive die. So, the as the device size has reduced, you have you are able to put more and more transistors on a chip. So, that has increased the packaging density and increased the … And this has, let to you know many challenges as we shall see. And present - day deep submicron technology not only has increased the speed, but also increased both dynamic and static power dissipations. As we have seen, because of the increase of large number of transistors, the dynamic power has increased per unit area of the chip and static power dissipation has also increased so.

And in this scenario, failure to meet power goals can have costly consequences on the viability of an IC and overall system. So, power has become a very important parameter

as I have emphasised on many occasions. Now question naturally arises, can you do low power synthesis design of ICs incorporating low power techniques manually? Because a number of transistors is very large, IC is very complex. You have to incorporate much complex functionality on a chip, can it be done manually? The answer is no.

So, traditionally use of RTL synthesis has led to major improvement in productivity. All of you are may be familiar with RTL coding, writing programs in Verilog or VHDL. So, what, there you write your system level functionality with the help of Verilog or VHDL; however, this has introduced a major disconnect between the front-end design and the real circuit, which burns power. So, who is doing which is writing program in Verilog to him? It is longer a circuit or a net list of electronic components, but high level functional description software in Verilog or VHDL. So, this has introduced a major disconnect between the actual circuit, and the way the design starts. So, RTL synthesis is traditionally timing driven with several iterations, to optimize area and fix timing violations. So, that is the basic approach that is followed in RTL synthesis

So, power was not a real concern until recently, unfortunately what is happened designing for low power is now a necessity rather than a choice. So, as you incorporate low power functionality, low power features, low power tools and low power techniques in your design the complexity increases.

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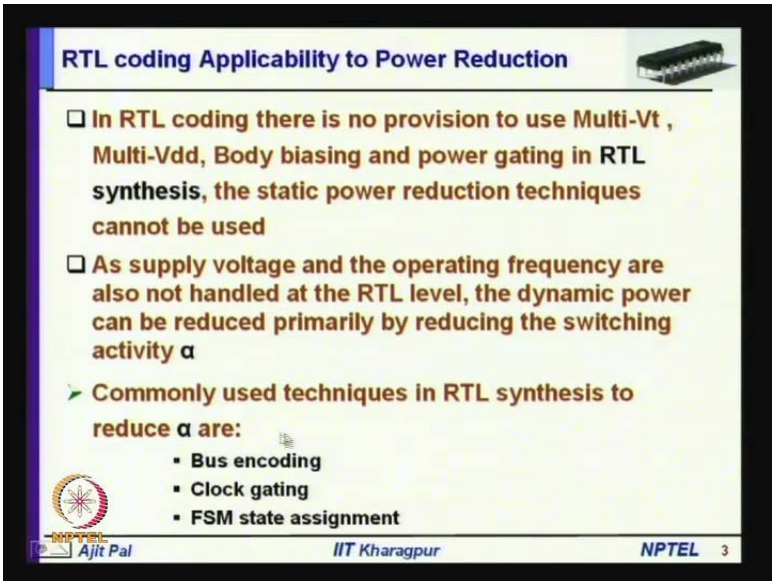

So, in spite of this, you have to incorporate them. So, what is the alternative? Let us first look at the limitations of RTL coding, and it is applicability to power reductions. What really you can do using RTL coding that means using Verilog or VHDL? Unfortunately in RTL coding, there is no provision to use multi- V t, multiple- V d d body biasing and power gating. And obviously, since this cannot be done, you cannot use any technique that will reduce the static power.

So, no static power reduction technique can be implemented with the help of traditional Verilog or VHDL coding, and as the supply voltage and operating frequency are not handled in RTL level. That means you cannot really realize circuit with multiple supply voltages. So, you cannot really incorporated incorporate multiple V- d d design here. There logic level one means, it can be five volt, and it can be one volt even if you use multiple V- d d in your circuit. So, that is a serious limitation.

So, the dynamic power reduction cannot be carried out by supply voltage scaling; however, the dynamic power can be reduced primarily by reducing the switching activity alpha. So, there are some techniques which can be implemented and these techniques will primarily reduce the switching activity and commonly used techniques in RTL synthesis to reduce alpha. Those switching activities are bus encoding, clock gating, and FSM state assignment. I have already discussed in detail about these techniques and using these techniques, you can reduce the transition activity or switching activity to reduce dynamic power. But you cannot go beyond this.

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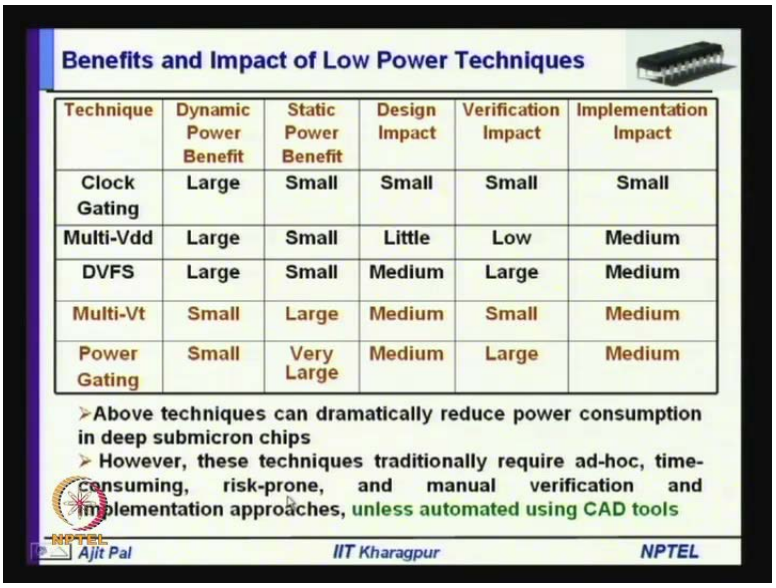

However, we have already discussed in detail various techniques, advanced techniques for low power and these are some of the benefits. And here, some of the important techniques are mentioned; number one is clock gating, clock gating can be used when you know some parts of the circuits are not in use in … You know when the circuit is in action. When the circuit is in operation, it can be in a block level or it can be in a gate level we have discussed in detail. So, you can incorporate clock gating and we have seen clock gating can reduce, I mean gives you large dynamic power benefit. But very small static power benefit, because using clock gating. You are essentially reducing the activity of the circuit, so that does not reduce the static power dissipation

And it has very small impact on the design, because the RTL coding has to be modified little bit to incorporate clock gating and also, it has got small impact on verification and also, very small impact on implementation. So, traditional approach can be followed with small changes. Similarly, you can incorporate multiple V- d d circuits, when different parts of the circuit can operate with different supply voltages. Again this can be done in the module level or gate level. So, in all these cases, there is possibility of reducing the dynamic power.

So, in this case also, there is large benefit on dynamic power reduction in dynamic power take place with small reduction in static power and it has little impact on design, because multi- V d d circuits can be realized. Essentially, only requirement is here that the some

parts of the circuit, you have to take power rail of different supply voltages and it has got low verification impact. And that means, whenever go for verification, it has no impact and implementation impact is medium. However, whenever you go for dynamic voltage and frequency scaling, this can be done in applications where you know the circuit can operate. You know has, different you know the circuit or the system will require different performance level. That means, sometimes you will require ten performance 10 percent performance, sometimes you require 20 percent performance requirement and so on.

In such a case, you can use dynamic voltage and frequency scaling and again this has got small, large impact on dynamic power, small impact on static power and design impact is medium. It is because, you have to modify some parts of the circuit, you have to incorporate those that variable voltage supply, you have to incorporate variable frequency circuit and it has very, I mean strong impact on verification. Because, it is very invasive and medium impact on implementation; that means, the implementation is becomes little complex. Then, the first three techniques are commonly used traditionally used to reduce dynamic power

Then to reduce static power, you can use multiple threshold voltage circuits with small impact on dynamic power. It does not give you much reduction in dynamic power, but it gives you large reduction in static power. And whenever you go for multi V- d d circuits, it has medium impact on design and small impact on verification and medium impact on implementation then power gating which is very important in our present day design. It has again small impact on dynamic power, because it leads to very small reduction in dynamic power, but it leads to very large reduction in static power. And it has medium impact on design, large impact on verification, it is highly invasive that we have seen and it has got medium impact on implementation. And these techniques can dramatically reduce power consumption in deep submicron techniques, deep submicron circuits. However, these techniques traditionally require ad-hoc, time-consuming, risk-prone and manual verification implementation approaches, unless automated using CAD tools. That means, unless you implement these techniques using automated CAD tools, these are not really very beneficial in the sense. Because, it takes long time, it is the risk-prone and manual verification implementation is not a very good situation, whenever you have got large, I mean complexity is very high

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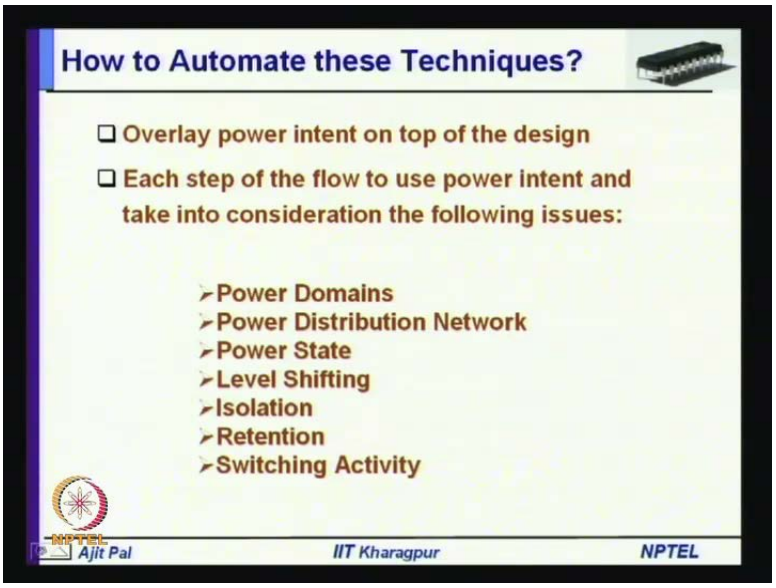

So, what is the …, how can be, how the low power techniques can be automated? One approach is overlay power intent on top of the design. That means what you can do? You can overlay power intent on top of the design. So, on top of the traditional design approach, you have, you will overlay power intent. How it can be done that?

I shall discuss and in each step of the flow to use power intent and take into consideration the following issues as we know. There are various issues related to low power techniques; such as power domains. Whenever you are using multiple V- d d, then power distribution network, clock tree network, and then power state .They will have different voltage, different states, then you have to use level shifters, you have to - isolation circuits, and you have to use retention hardware. And also, you have to take into consideration, the switching activity at different parts of the circuits. So, these are the various issues, you have to take into consideration whenever you go for using low power techniques.

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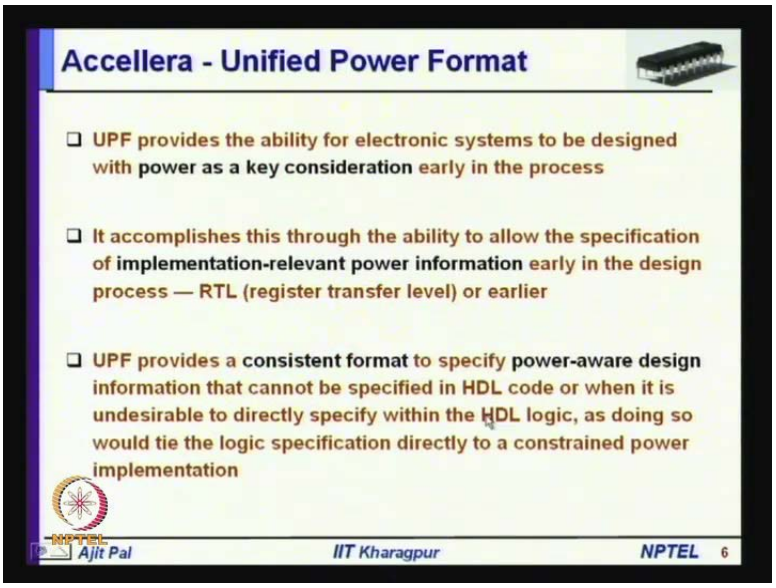

UPF Accellera, accelerate has proposed a unified power format, which has been widely accepted by industry and it provides the ability for electronic systems to be designed with power as a key consideration early in the design process, may be at the RTL level. So, it accomplishes this through the ability to allow specification of implementation-relevant power information early in the design process. That means, whenever you are doing RTL synthesis using Verilog or VHDL along with that, you will also incorporate your low power intent with the help of UPF. So, UPF provides a consistent format to specify power-aware design information, which cannot be specified by HDL code. As I have told, HDL has got serious limitation, and it cannot really incorporated most of the low power features that I have discussed or it can be used, when it is undesirable to directly specify within the HDL logic, as doing so tie the logic specification directly to a constrained power implementation.

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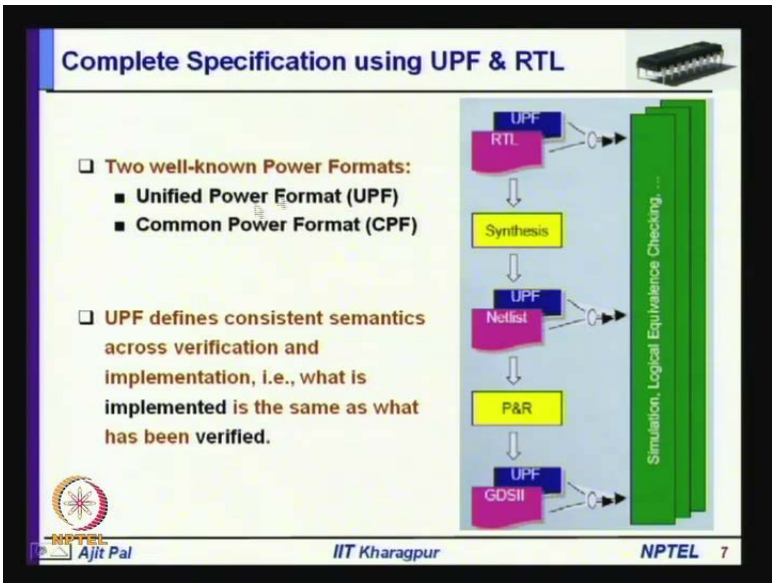

So in both these cases, it is necessary; it will be, I mean these the power intent will be specified with the help of UPF. So, this is actually not only UPF. There are two well known power format: one is UPF that is your Unified Power Format developed by Accellera and it has been accepted by many standards; another is Common Power Format, because unified power format or UPF is most popular. I shall be primarily discussing based on UPF and as you can see, UPF defines consistent semantics across verification and implementation. And that is, that means, what is implemented is a same as that of verified. So, you can see it can be used throughout the …, I mean throughout all the design steps like synthesis, placement and routing and you can, you will be doing simulation, you will do will be doing verification. And also will be performing sign-off as we shall see.

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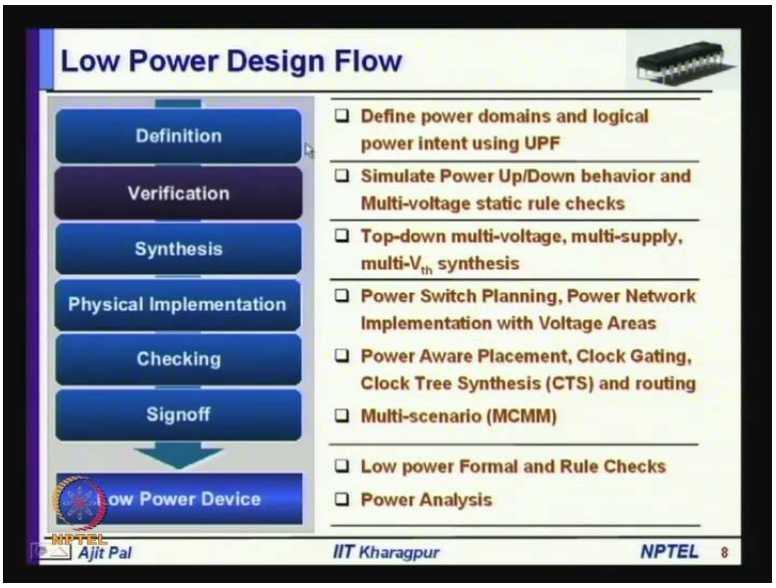

So, UPF along with your VHDL coding or RTL coding can be used throughout the synthesis cycle, starting from system level to the layout level. So, here is the design flow so, what you have to do? Define power domains and logical power intent using UPF. So, that is essentially the definition stage then, you will do simulation various low power. I mean after incorporating those low power techniques, power up or down behaviour and multi-voltage static rule checking. So, we will do simulation and do verification then top - down multi-voltage, multi-supply, multi-V t h synthesis. So that means, you will perform synthesis after verification and in this case, as you can see, the IC can have multiple voltage multi supply. That means, it will be using different switching then, multiple threshold voltages in the synthesis and physical level implementation, where you will implement power switch planning, power network implementation with voltage areas. So, this will do physical implementation then Power Aware Placement, Clock Gating, Clock Tree Synthesis and routing. So, these parts you will do synthesis and then you have to take into consideration multi-scenario so, multi-corner multi-mode scenario. That means, you have to take into consideration all possible alternatives; that means, the low voltage, high voltage, high v t low v t and so on. Then finally, you will be, you will perform sign-off and realized the low power device, where you will do low power formal and rule checking, where you will check, whether your design and actual implementation are same or not, and also will do power analysis.

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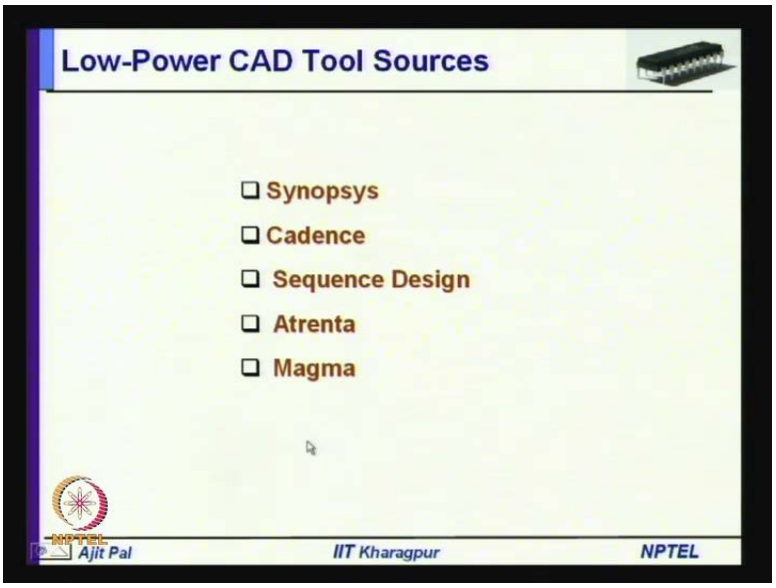

Obviously you will rule, you will require various tools to both through this low power design flow and CAD tools are available for this purposes from various sources: Synopsys, Cadence, Sequence Design, Atrenta and Magma. So, all of them have developed low power CAD tools and they provide of course, their functionality may differ little bit, but they will provide some of the features which I have already mentioned. We shall primarily focus on Synopsys CAD tool, Synopsis tool and low power solution

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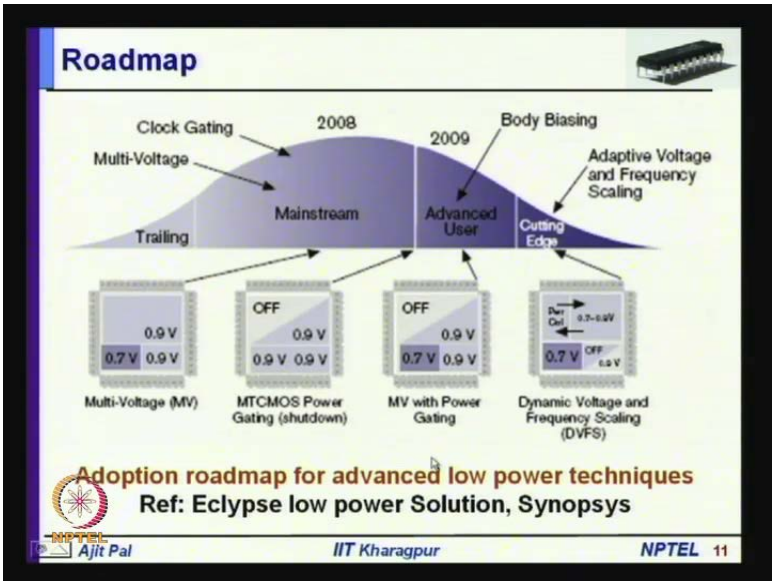

So, this is the road map of Synopsis and the Synopsis predicted that, this is how industry will adopt various techniques of low power techniques. As you can see, those who are trailing, they will be using they will be using simple single supply voltage, single V t circuits. But the industries which will be in a main stream, they will be using multi-voltage and they will be using Clock Gating and those will be using little advanced techniques gradually, as you move from two-thousand-eight to two-thousand-nine. They will be gradually that MTCMOS based power gating will be adopted by most of the industries and then multi-voltage with Power Gating will become common place or has become will become, common place in two-thousand-nine along with body biasing. And then beyond this, you have got industries which will be using cutting edge technologies; they will use adoptive voltage and frequency scaling. And that means, they will be not only using multiple voltages multiple threshold voltages, but dynamic voltage and frequency scaling.

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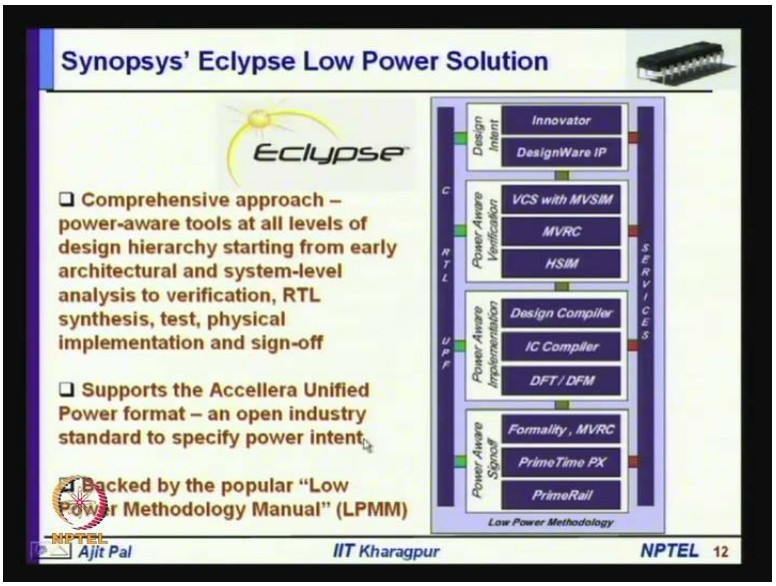

So, this is the road map that was predicted or by Synopsis and various industries is in different stages of this … The CAD tool that has been proposed by Synopsis is known as Eclipse. So it is a comprehensive approach, power-aware tools at all levels of design hierarchy, starting from early architectural and system level analysis to verification. Then RTL synthesis test physical implementation and then finally Synopsis. As you can see, it is not really a single tool, but say suite of tools starting from design intent to sign-off. So, various tools are developed which are part of a Eclipse, which I shall there are various

functionalities, one after another. And this eclipse supports the Accellera unified power format, that is UPF that I mentioned which is an open industry standard, to specify power intent, and this is backed by, Low Power Methodology Manual.

I have mentioned about that low power methodology manual that has been developed jointly by, Synopsys and arm together. And the various approaches, which are proposed in this low power methodology manual, have been adopted in Eclipse

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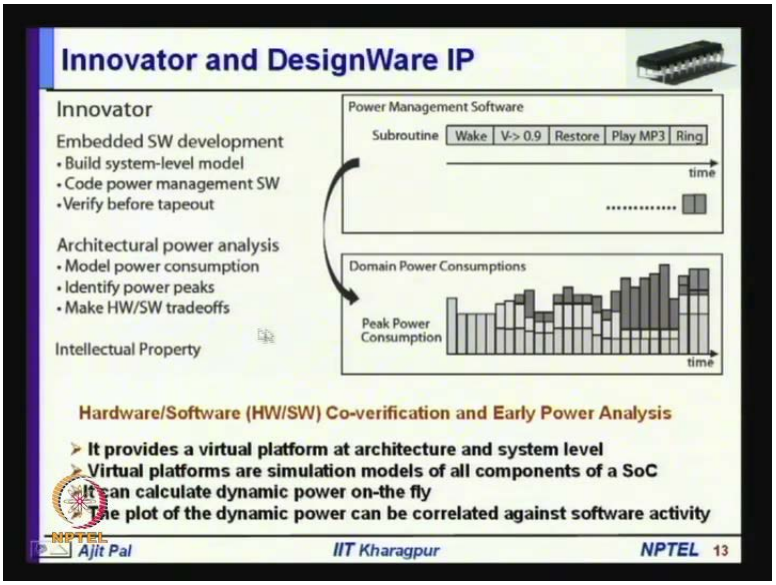

First we shall focus on Innovator, Innovator is a … It provides a virtual platform at architectural and system level, what do we really mean by virtual platform. So, it gives you, simulation models of all components that you require in implementing a system on chip; that means, processors, co-processor, buses and various other components that you require are provided in this. And these virtual platforms are simulation models of all the components of a SoC as I mentioned, and then at the design phase, it can calculate dynamic power on the fly; that means, you have got the simulation models and using that simulation models, you can run some application program and as you run some application program on the fly, it can give you information about the dynamic power consumption and based on that you can.

That means, the plot of dynamic power can be correlated again as software activity. So, these are the key features of this Innovator and that means, it gives you architectural level power analysis; it can model power consumption; it can identify peak powers.

So what it really do, what, how it will help you? At the design step, you will be doing, I have already discussed about hardware software partitioning or hardware software trade-off; that means same functionality, you can implement by hardware or by software or by a judicious combination of hardware and software. So, in this design phase, this software, this Innovator helps you to plan. That means, as you do the simulation, you can identify which part to implement by software or how you can really do the partitioning? Such that your power budget is not violated, so that can be done in the early design step.

So, it is a hardware software co-verification and early power analysis. So, this is a very useful tool at the design step, not only that it. It provides you various Design Ware IP, various IP's which have been developed by many industries those are also available and they can be simulated with the help of this Innovator. And then after, you know early design is done and you have done, you have you have identified necessary hardware and software to be implemented. Normally, VCS is commonly used for the purpose of RTL and Net list simulation.

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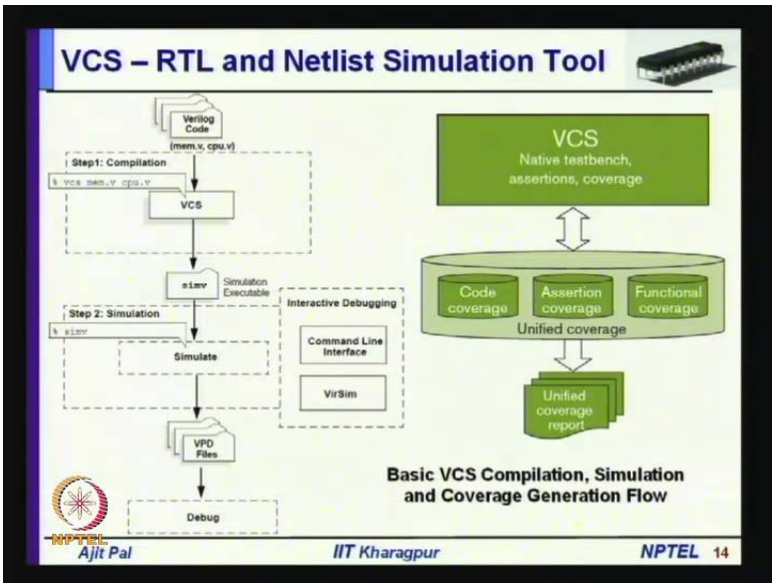

So, this with the help of this RTL and Net list simulation tool, you can do compilation, then you can do simulation and you can find out the functionality of the circuit. But unfortunately, this VCS cannot take the power intent information in the design.

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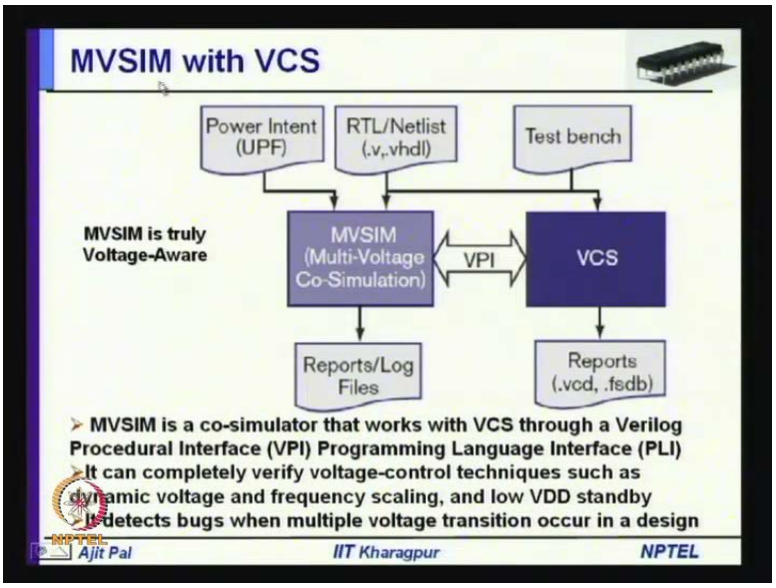

So what can be done? You can incorporate MVSIM with VCS. So, MVSIM with VCS can be done, because MVSIM is a co-simulator that works with VCS through Verilog Procedural Interface, programming language interface. So, Verilog Procedural Interface, Programming Language Interface with that, it can, they can work together. So, it is a co-simulator and as we can see, the just like VCS can accept the RTL or you know that, that logic level Net list, the VCM, MVSIM also can accept the same RTL the logic level net list. It can accept same test bench as the VCS and of course, they interact with VPI as I have already mentioned..

And then, it can that means in the additional thing that, the MVSIM does, it accept the power intempt intent power intent specified by UPF. So, UPF specifies those multiple voltage domains, multiple V- d d circuits and so on. So that means, the low power intent part is the additional thing that MVSIM accepts so, it can completely verify voltage control technique such as dynamic voltage and frequency scaling, low V- d d standby.

It can detect bugs, when the multiple voltage translation occurs in the design as, so far as the VCS are concerned; it does not really differentiate between two voltage levels.

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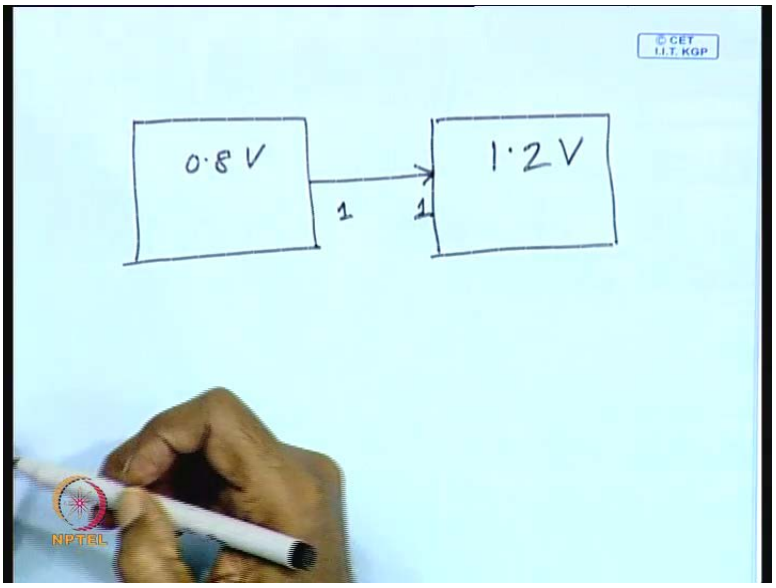

That means, suppose you are using a circuit with say, you have got a circuit which is operating at say zero-point-eight volt and here another circuit, which is operating at may be another part of the circuit or module operating at one-point-two volt. So, if a signal goes from here to, from this voltage domain to this voltage domain VCS, say voltage level is one. So, VCS will take a signal level one; that means, a point-eight voltage is going to another voltage domain and it that is also considered as voltage level one. But as you know, we know the consequences of this. So when a low voltage signal, I mean high voltage signal goes… High level signal goes from a low voltage domain to a high voltage domain, it can lead to you know that, short circuit power dissipation or (()) power dissipation.

But unfortunately, VCS cannot differentiate between the two voltage levels. On the other hand, this MVSIM, whenever you use MVSIM along with VCS then, this voltage differences are identified, can be identified and actually MVSIM is truly voltage-aware. So, various voltages it can take off.

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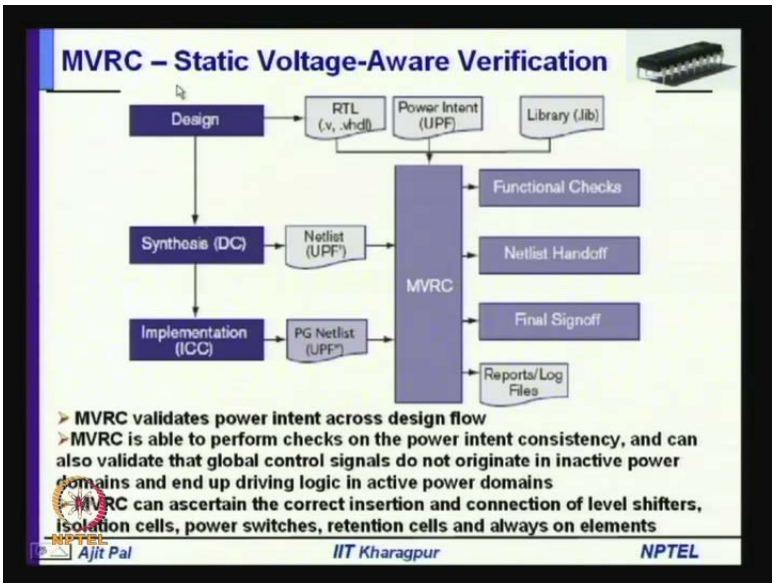

So it detects bugs, when multiple voltage transitions occur in the design. So, this is how we can do the simulation and after the simulation, you will be doing verification. So, MVRC is the tool that is used for static voltage-aware verification. So as you can see with the help of MVRC, it validates power intent across design flow. So, RTL along with UPF are giving your specification and MVRC will accept that. And we can see, it will do not only the design and as you do the synthesis and net list is generated. MVRC will do the net list and it will do the necessary verification and as you do the placement, and routing implementation that also is verified with the help of MVRC.

That means, it will do functional checks, it will do net list handoff, it will do final sign off. So, it is a static voltage-aware verification tool. So, it is MVRC is able to perform checks on power intent consistency and can also validate that global control signals do not originate in inactive power domains and end up driving logic in active power domains. We have seen in a circuit, some parts will be in standby, some parts will be in active state so, and no signals should go from a standby part of the circuit, to the active part of the circuit. So, this detection is done, and verification is done with the help of MVRC

So, not only MVRC does this entire thing, it can ascertain the correct insertion and connection of level shifters. We have seen, you will require level converters whenever you are using, will be using multiple voltage domains. So, it will ascertain the correct

insertion and connection of level shifters, isolation cells, power switches, retention cells and always on elements. That means various components that is required in a context of multiple multi V- d d circuits or whenever you incorporate those Power Gating techniques. Those components, whether they are correctly inserted or not that can be verified with the help of MVRC.

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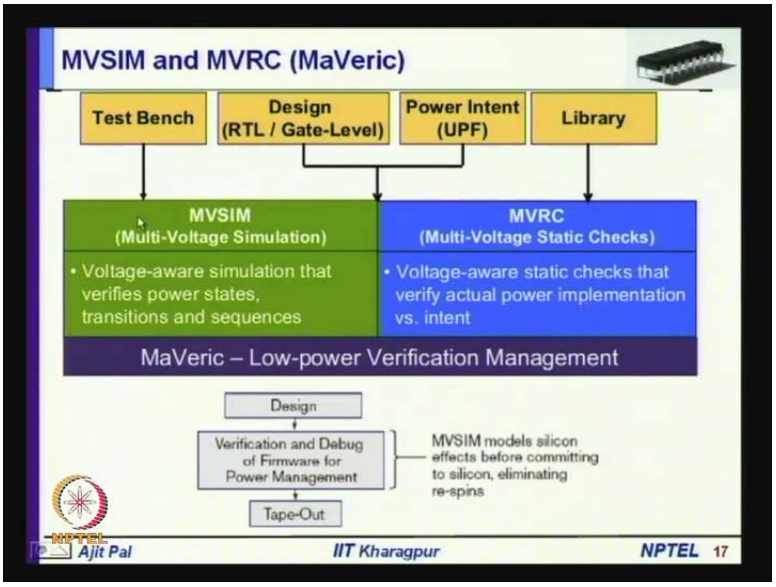

And as we can see, MVSIM and MVRC together is performing so, this MV MVSIM performs Multi-Voltage Simulation, and MVRC, MVSIM perform Multi-Voltage Simulation, and MVRC performs Multi-Voltage static checking static Rule Checking. So that means, MVSIM performs voltage-aware simulation that verifies power states transition and sequences. And MVRC performs voltage-aware static checks that verify actual power implementation versus intent; that means, whatever is the intent and actual implementation by comparing that. It can check whether it has been implemented correctly or not

So, what is the net outcome? You can see, you start a design and this using this MVSIM and MVRC, what is happening verification and debug of firmware for power management is done with, the help of this in a single step. So, before you commit it to silicon and eliminate re-spins; that means, normally what happens you do the implementation, if it does not satisfy the purpose? You have to again go back to the design.

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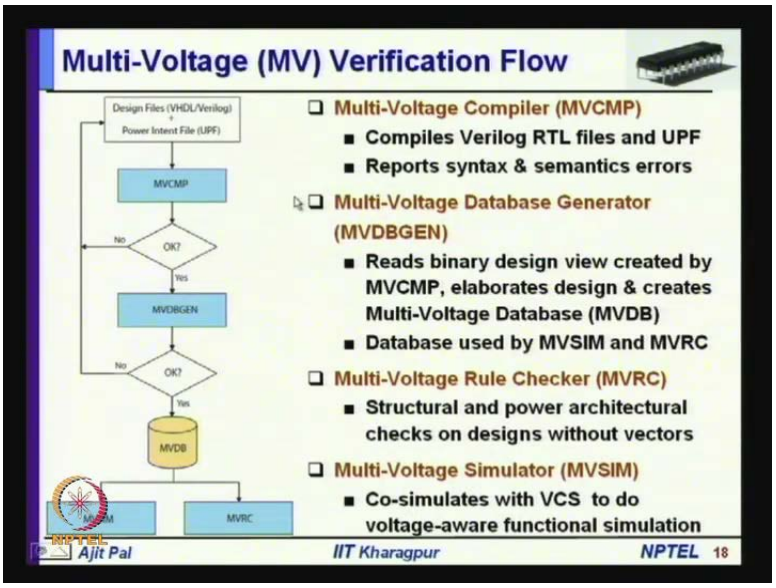

So, that can be avoided and that will reduce the time to market of a particular chip or device, and you can tape-put very quickly. And this is that multi-voltage verification flow that is done with the help of MVRC and MVSIM. First, there is a multi-voltage compiler MVCMP that compiles Verilog RTL files and UPF. So, you can see here always, we are incorporating these two together; VHDL or Verilog code along with UPF power intent power intent file, so it compiles, this multi-voltage compiler will do the compilation and it will report syntax and semantics error. So, this syntax and semantic checking is done with the help of this compiler.

Then, multi voltage database generator will generate some information, it reads binary design view created by MVCMP and elaborates design, and creates multi-voltage database. So, it will generate a database which will be used by MVRC and MVSIM, and this database is used by MVSIM and MVRC. So, you can see that flow here.

So, it goes through MVCMP and it checks the syntax and semantics. Then the database is generated that goes to this MVRC and MVSIM. So MVRC does structural and power architectural checks on designs without vectors, and multi-voltage simulator MVSIM as I have already mentioned; it co-simulates with VCS, to do voltage-aware functional simulation.

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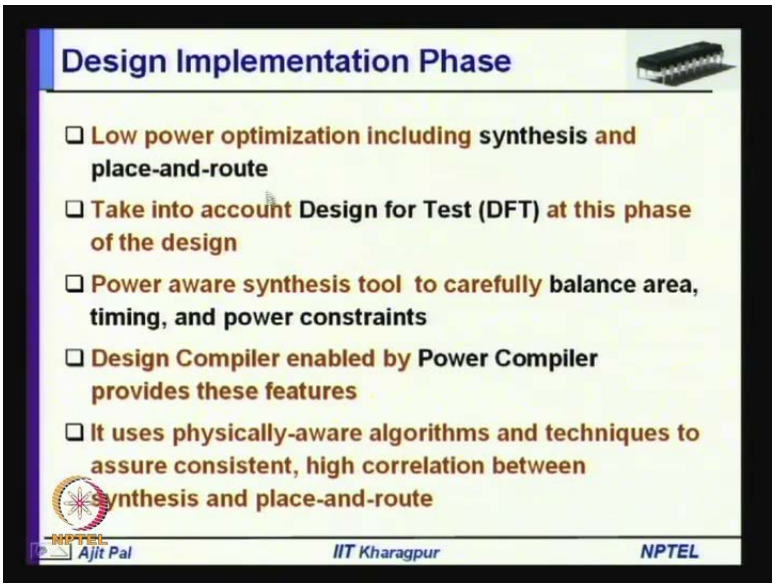

So this is the, this database is used by MVSIM and MVRC, so this is the design flow for simulation and verification now. After the simulation and verification as I mentioned, you have to do the design. So this is the, in the design implementation phase, you have to perform low power optimization, including synthesis and placement and routing. So that means… and the only synthesis that will incorporate, low power techniques and you have to perform placement and routing of various components of that is switches, Clock Gating circuits and other things.

And not only that, you have to take into, account design for test. So, present nowadays design for test incorporation is very important; that means, you will incorporate some hardware as part of the chip, which will help you to do the testing. So, you will do this design, which will be used for the purpose of the testing at later stage. So, you have you have to incorporate that. So, this power aware synthesis tool should care should should carefully balance area, timing and power constraints. So, not only area is important or timing is important, power constraints are also very important. All these three are to be properly balanced, with the help of this design implementation tools.

What is done in this in this in the synopsis tool? They have used design compiler enabled by power compiler. So, the power compiler is the addition which will take care of those power intent implementation things; that is whatever you those low power techniques, that we implement, that will be taken care of with the help of this Power

Compiler. So, design compiler enabled by Power Compiler, is the solution and this it uses physically-aware algorithms and techniques to assure consistent high correlation between synthesis and place-and-route. So, we shall how this high correlation is obtained between synthesis and place-and-route.

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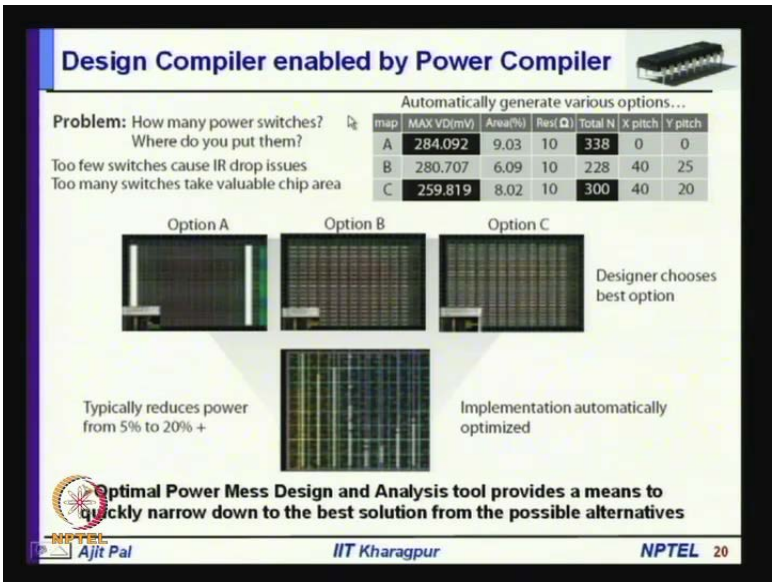

So, as I mentioned design compiler enabled by Power Compiler, is done here. Question arises, how many power switches are to be used? We are interested in reducing the number of switches, because if you add more number of switches, which will increase the area. On the other hand, if you increase lesser number of switches, that may lead to voltage drop, as you draw larger current. So, here is a trade-off between performance and area. So, the not only how many switches? How do you put them? Where do you place them? That means, too many too few switches cause, IR drop issues, voltage drop takes place and too many switches take, valuable chip area as I mentioned.

So, what this design compiler enabled power compiler? Does it generate several design options? So, option a, option b, option c with various features; that means, they can have different area, you can see different area. And also different delay, different resistance and delay, and designer can choose has the choice of selecting one of the few such good designs. That means, this can this is how depending on the application requirement, one can choose the best out of the best solutions.

So, Optimal Power Mess Design and analysis tool provides a means to quickly narrow down to the best solution from the possible alternatives, as I have mentioned. So, it typically reduces power from 5 percent to 20 percent plus and implementation is automatically optimized.

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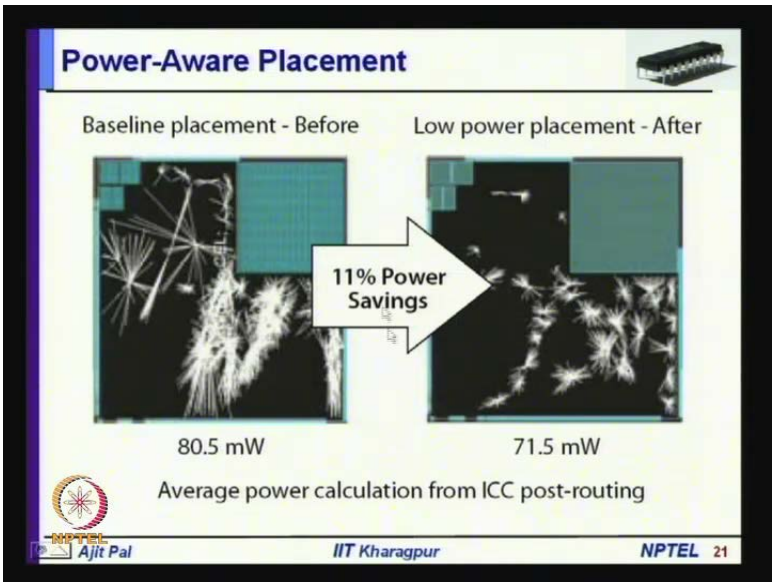

So, various optimizations are done; I shall discuss some of the optimization techniques those are being done for example, it does power-aware placement. So, if you, if the placement is not done properly, it may lead to lot of, I mean lot of power dissipation and simply by placing them properly, the power dissipation can be reduced. So this is how, it is being done and you can see, this is the low power placement after, and this is baseline placement before.

So using this tool, you can achieve this power-aware placement. As I mentioned this IC, this design compiler along with power compiler helps you, to do that.

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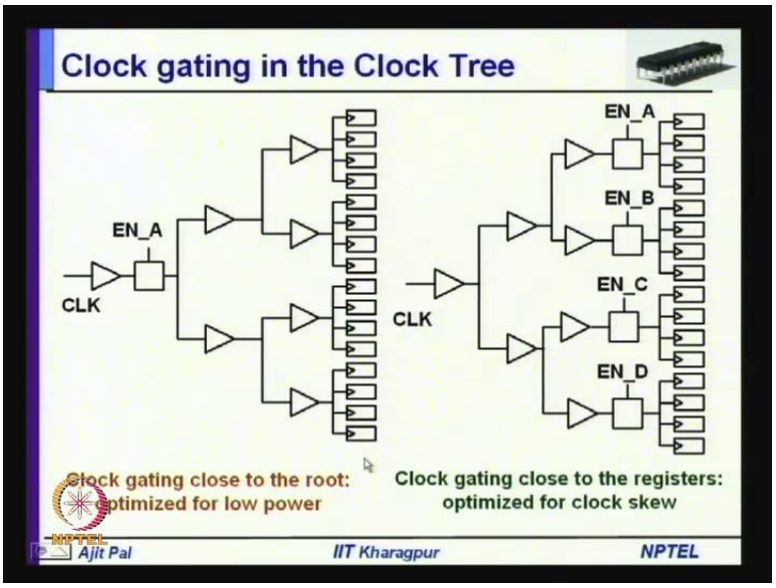

Then coming to Clock Gating, we have seen Clock Gating is to be inserted and if you can insert them automatically, there is nothing like it. And you can see traditionally, you can use Clock Gating for two purposes: In the first case, you can see, you can use it to reduce power dissipation; that means, if you use it early in the closure to the source of the clock. So, this Clock Gating has been done closure to the source of the Clock Tree and it is driving the subsequent parts of the Clock Tree. If you can insert a Clock Gating here, it will lead to larger saving in power dissipation. On the other hand, on the other hand this will introduce, I mean whenever you can this will introduce lot of, I mean clock skew through different parts of the circuit.

On the other hand, you can introduce this Clock Gating close to the registers. So here you can see, this is the clock tree and these Clock Gating circuits have been incorporated, which are very close to the registers. So, Clock Gating close to the registers; this optimizes the clock skew.

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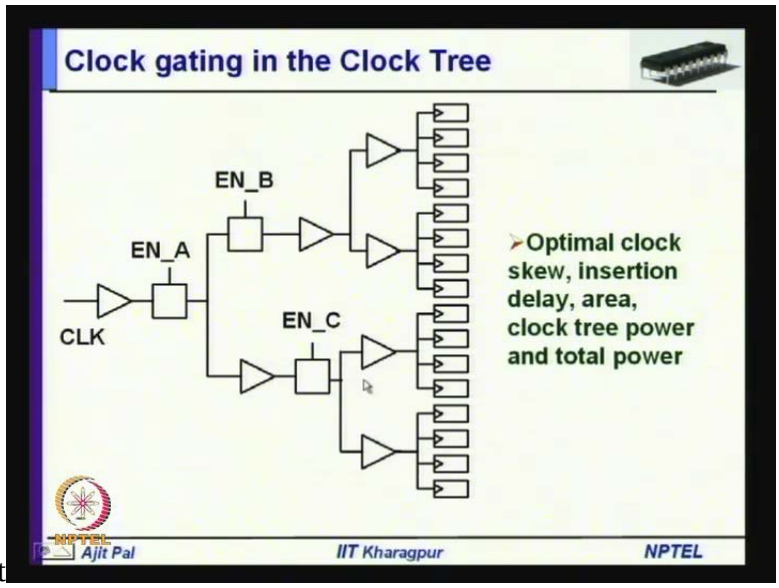
hat 

So, delay of different paths that are your difference in delay of different paths; that are your clock skew. That clock skew can be optimized with the help of this technique. Now using the automated CAD tool, what what is being done? The Clock, the Clock Gating is introduced, judiciously in different paths. As we can see, it has incorporated Clock Gating circuits; one is close to the source, another is close to the registers, another is in between. So by doing that you can, what it does? It optimizes clock skew, insertion delay, area, clock tree power and total power; that means, it is optimizing multiple parameter simultaneously, not only area, not only clock skew, not only delay and various parameters. It is trying to I mean, optimize simultaneously and that is being done with the help of this automated CAD tool.

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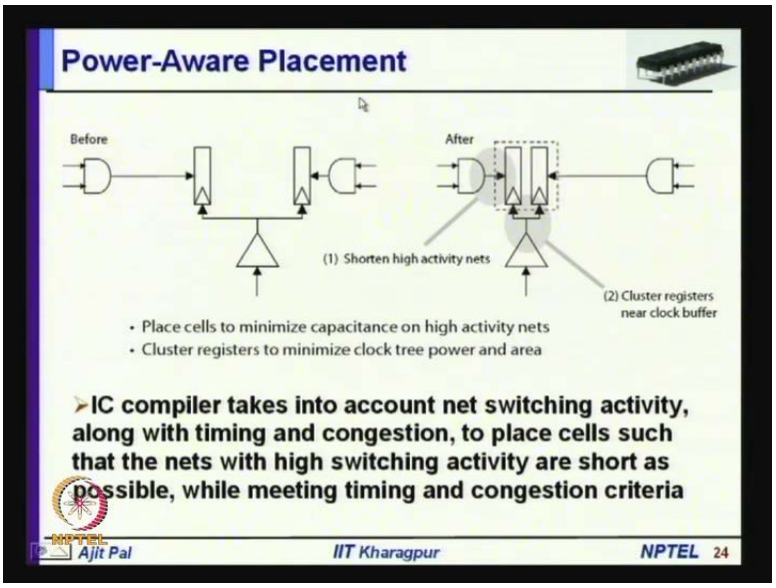

So, this is your Clock Tree generation and what the power-aware placement does? This IC compiler takes into account net switching activity, along with timing and congestion, to place cells such that the nets with high switching activity are short, and are as short as possible, while meeting timing and congestion criteria. So, you can see this is before; that means, here the neither the switching activity, nor the congestion has been taken into consideration. But here this for example, this particular net has high switching activity, so the length of this particular net has been reduced. So, it has shortened the high activity nets. So, this tool has reduce the length of this high activity net and also it has this part the for example.

This particular clock tree, I mean is driving this register as well as this register and these are wide apart. So, the in this tool, they have been clustered together, to minimize Clock Tree power and area. So, Clock Tree power and area as minimized by, clustering this part of the circuit so, clustering the registers. So, this power-aware placement will definitely reduce various parameters that I have already told particularly. It will reduce the power dissipation due to switching activity and also, it will reduce area because, it reduces the net length.

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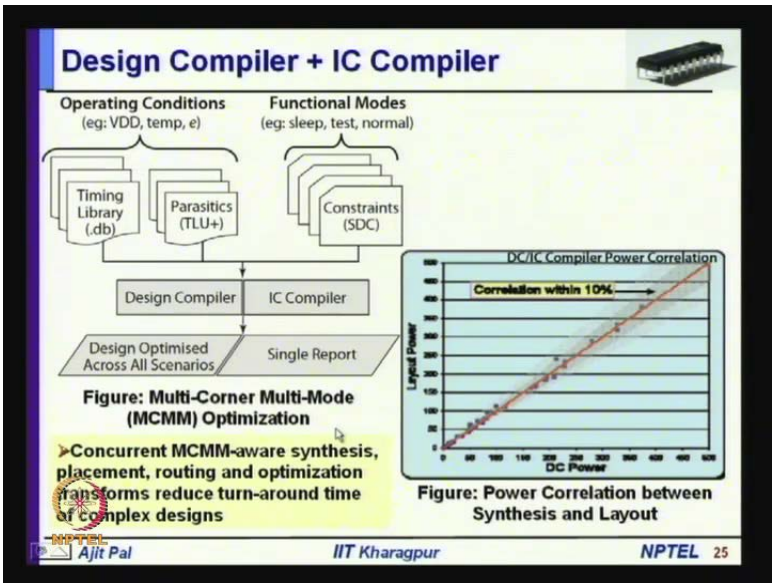

So this shows, how the design compiler and IC compiler works together? I have mentioned that along with design compiler, you will be using IC compiler to do various optimization placement, routing and all these optimizations. Essentially, it is a multi-corner, multi-mode optimization.

So, concurrent MCMM - aware synthesis, placement, routing and optimization transforms reduce, transforms reduce turn-around time of complex design. So, this multi-corner multi-mode optimization will help you, to get optimization and also it will reduce the turn-around time of very complex design. On the right side here, there is a plot and it shows the correlation between the synthesis and layout, you can see here. There are, this plot shows here, the layout power and here the d c power. So, you can see at the design time, what was the power? And here is a low out power. So we find that, that d c by IC compilation power correlation is very high so, correlation is within 10 percent. So, this shows the efficacy of the tool; that means, the design and layout are very close, and only ten percent, correlation is within 10 percent.

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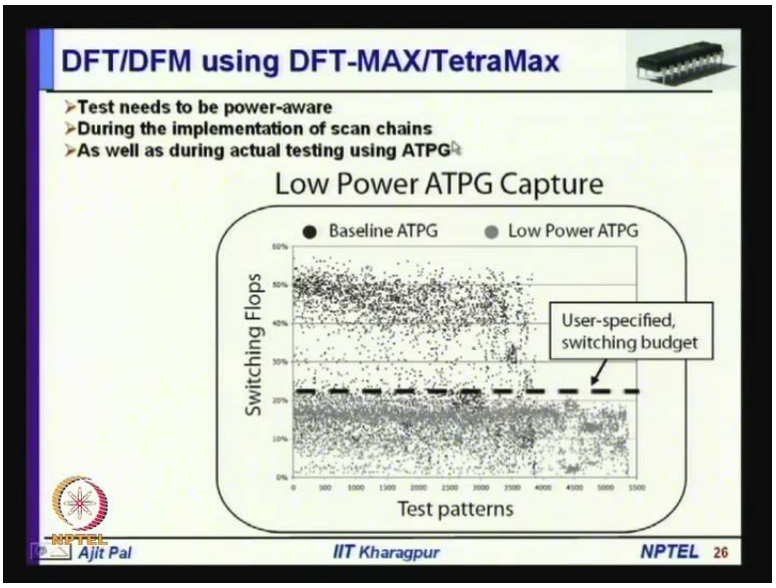

So this shows the, I mean how good is the tool? And how it helps to? I mean, accurately does the placement and routing and various design techniques it performs, as I was as I was mentioning about the testing.

So, you have to incorporate design for testability; that means, you have to incorporate scan chains. I am not going into the details about the testing; there is a full course on testing and verification, where, how to incorporate scan chains are discussed in detail. So, you have to incorporate scan chains which can be used for testing and these are these are incorporated in a design not only, you have to use them. I mean at the time of design, but at the time of actual testing with the help of ATPG. Those are Automatic Test Program Generation hardware; that generates the test sequence and at the time of testing, it has been found that. At the time of testing, lot of switching activity take place and actually, the switching activity may be higher than, when they are actually used.

The reason for that is, whenever you are testing with the help of ATPG, you may be simultaneously activity; I mean activating different parts of the circuit and lot of lot of dynamic power dissipation will take place. But in practice, whenever they are they are being used, they may not be used in parallel. So, what can happen? The power dissipation may be more, at the time of testing and this may lead to artificial failure of the chip. So, it may not fail, when it is actually used, but it may fail at the time of testing. So, it is a kind of artificial failure.

So this, that means, this actual, this testing at the testing time, you have to you have to develop techniques such that, the artificial failures can be avoided. So, that is being, what is done with the help of this, these with the help of this tool. So, during actual testing with the help of ATPG, you can say this line is a user specified switching budget; that means, at the time of testing or use, it should not exceed this line. So, if you do not use the automated CAD, the cad tool that I have mentioned that is your DFTDFM using DFT MAX/ Tetra MAX. So, this tool actually identifies, I mean how you should really apply the test sequence, such that the switching budget is not exceeded.

So, this is the base line ATPG and you can see, here it is exceeding the base, the power budget, the user specified switching budget and this may lead to artificial failures.

On the other hand, other hand this part the lower part of the circuit, you can see the power dissipation has reduced to around ten-twenty percent compared to 60 percent with the help of this low power ATPG, which is which is provided by this tool.

So, you can see at the time of actual testing, the power dissipation can be significantly reduced with the help of this tool.

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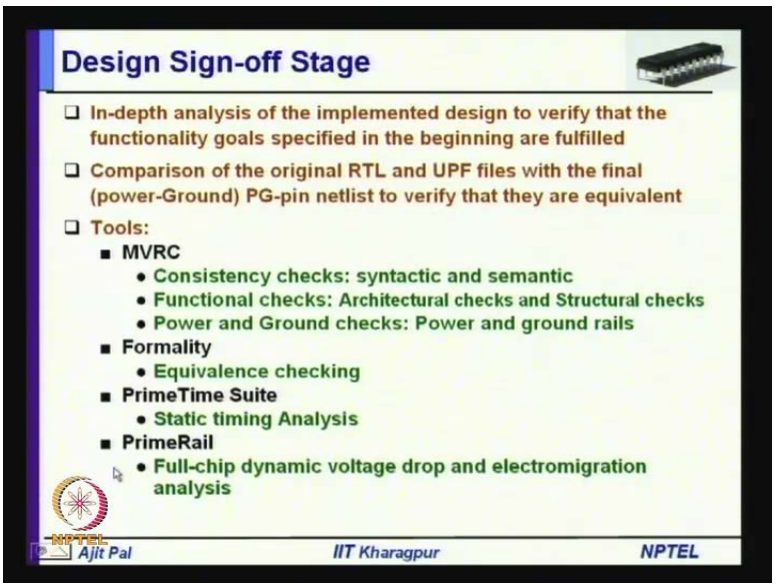

Coming to the last stage, that is your design sign-off stage. So, whenever you are signing off, that means you are realising the chip for commercial implementation at the stage, you have to do certain things which are mentioned here. You have to perform in-depth

analysis of the implemented design to verify that the functionality goes specified in the beginning with the help of UPF and VHDL or Verilog code are fulfilled or not. Then you have to compare the original RTL and UPF files with the final. This power this is known as PG- pin or power ground PG- pin net list to verify that they are equivalent.

That means, you have to you have to perform verification with the intent, with the actual implementation that verification has to be done, and it can be done with the help of several tool know as formality. So, MVRC does the consistency checks, I have already discussed. It will do syntactic and semantic checks and functionality checks: architectural check and structural checks should be done by MVRC, I have already mentioned about that. And then power and ground checks where it checks, whether different parts of the circuits are getting the power supply or ground lines or not; This is also done with the help of MVRC. Then you have got formality, which does the equivalence checking, and prime time suit which does static timing analysis, and prime rail which does full-chip dynamic voltage drop and electro migration analysis.

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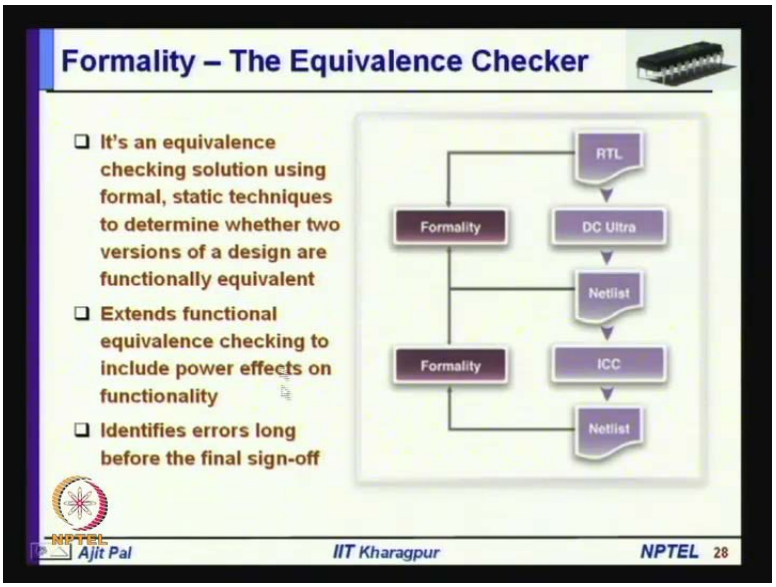

So with the help of this, the design sign-off stages perform. You can see, this is the formality equivalence checker, so it checks the RTL as input and also the net list, and it compares them. So, it is an equivalence checking solution using formal and static techniques to determine whether two versions of a design are functionally equivalent or not. So, it is extends functional equivalence checking to include power effects on

functionality. So, it is not only taking into consideration the functional behaviour, but also the those power effects, as you incorporate those low power techniques and it identifies errors long before the final sign-off .

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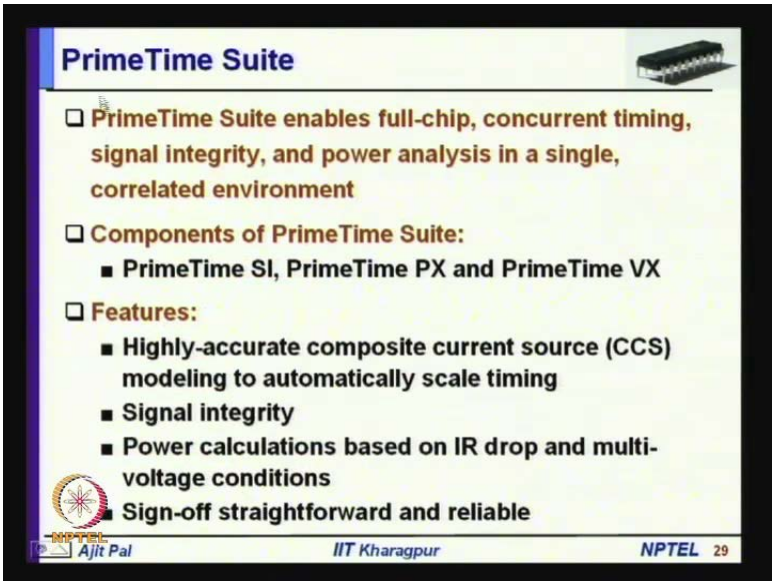

Then prime time suit enables full-chip, concurrent timing, signal integrity and power analysis in single, correlated environment and these are the various components of prime time suite: Prime Time SI, Prime Time P X and Prime Time V X.

And the key features of these - prime time suite is highly- accurate composite concurrent current source modelling of automatically scale timing; it does signal integrity and power calculation based on IR drop and multi-voltage condition and sign-off straightforward, sign-off straightforward and reliable with the help of this tool. So this is how, the prime rail does the rail analysis in detail.

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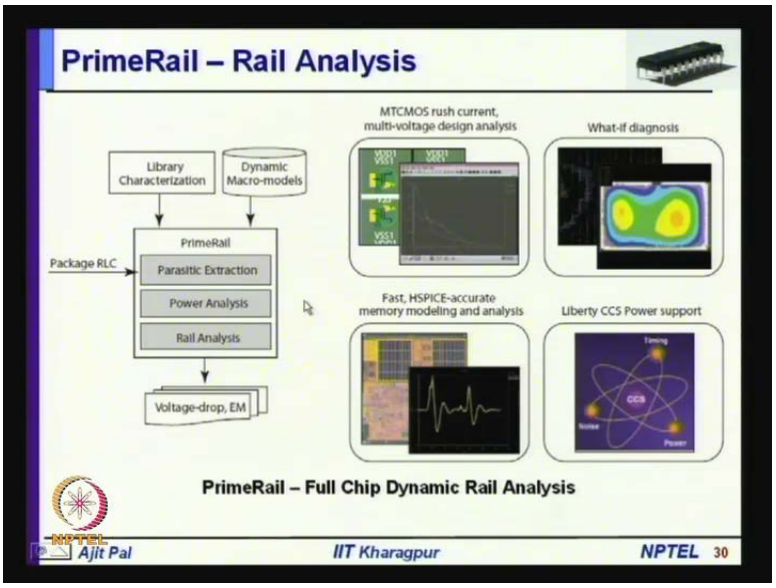

So, it can do that MTCMOS rush current, whenever you are using MTCMOS based gating, it checks whether it there is any heavy current is flowing or not. And it does what if diagnosis; that means it can checks, I mean what has failed and which parts, where there is you know that large power dissipation. So, these are the various stages: Parasitic Extraction, power analysis and rail analysis. And it can perform, it can do, it can identify voltage drop and electro migration. So, it is a full chip dynamic rail analysis tool that helps you to sign-off

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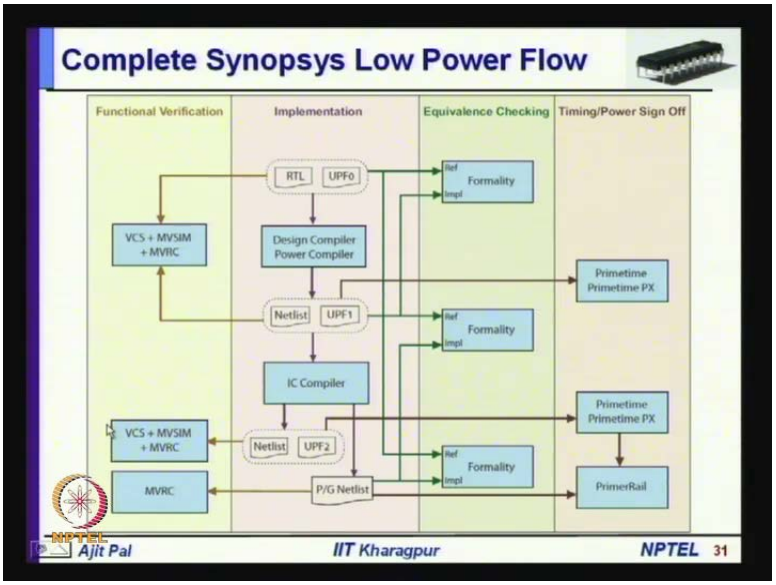

And this is the last slide that gives you, the complete synopsis low power design flow. So, you can see starting with functional verification which can be done with MVSIM with MVRC. Then the implementation, which can be done with the help of Design Compiler and Power Compiler and IC compiler complete design, can be done along with low power intent. Then you can do Equivalence Checking with the help of formality at various levels of design hierarchy. Then finally timing and power off, you can do with the help of prime time prime time P X, prime time P X and power rail.

So, that is also done at different levels of design hierarchy. So, this slide gives you, a complete picture of the design flow and different tools which are being, which you can use in the for the low power synthesis of digital circuits. So, with this, we have come to the end of not only today-s lecture, but also end of this lecture series. Thank You