Low Power VLSI Circuits and Systems

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Lecture No. # 36

Adiabatic Logic Circuits

Hello and welcome to today's lecture on Adiabatic Logic Circuits. This is a new class of circuits; obviously, much different from static CMOS circuits and we shall see how you can reduce the power dissipation in adiabatic circuits. So, obviously the circuits would be CMOS in nature.

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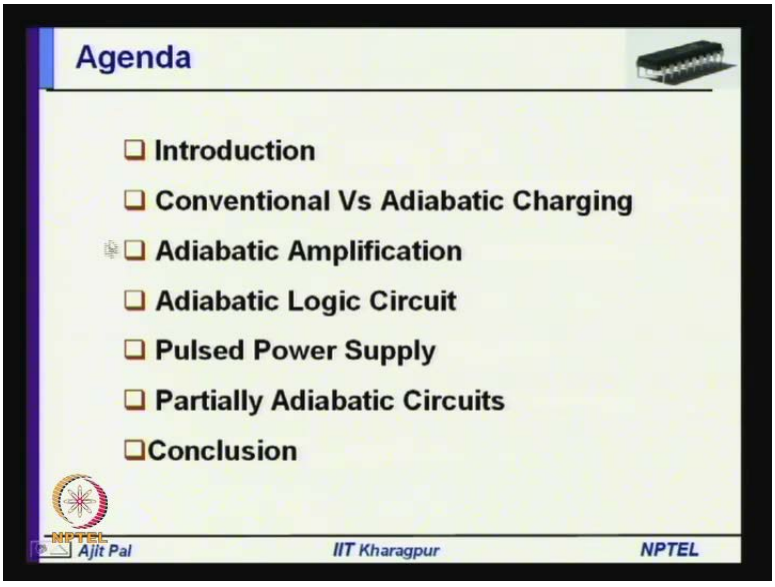

But adiabatic CMOS and here is the agenda of today's lecture, after giving a brief introduction, I shall discuss the basic differences between conventional and adiabatic charging. Then, we shall see how we can do adiabatic amplification and then, we shall discuss about realization of adiabatic logic circuits and after that, we shall have brief discussion on pulsed power supply, which will be required in implementing adiabatic logic circuits. Then, we shall discuss partially adiabatic circuits to reduce the cost of implementation, fully adiabatic circuit. Then, we shall conclude the lecture with some comments.

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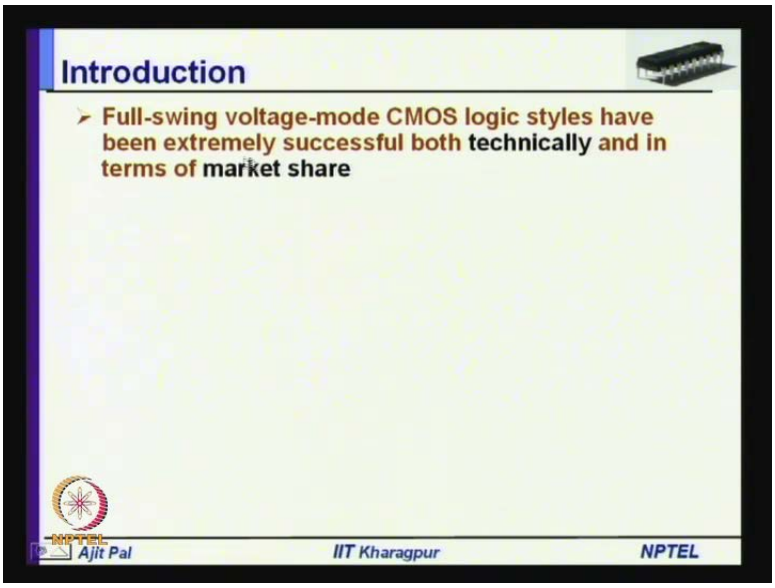

So far, we have seen that full-swing voltage-mode CMOS logic styles have been extremely successful both technically and in terms of market share. That means, whatever we have discussed, so far.

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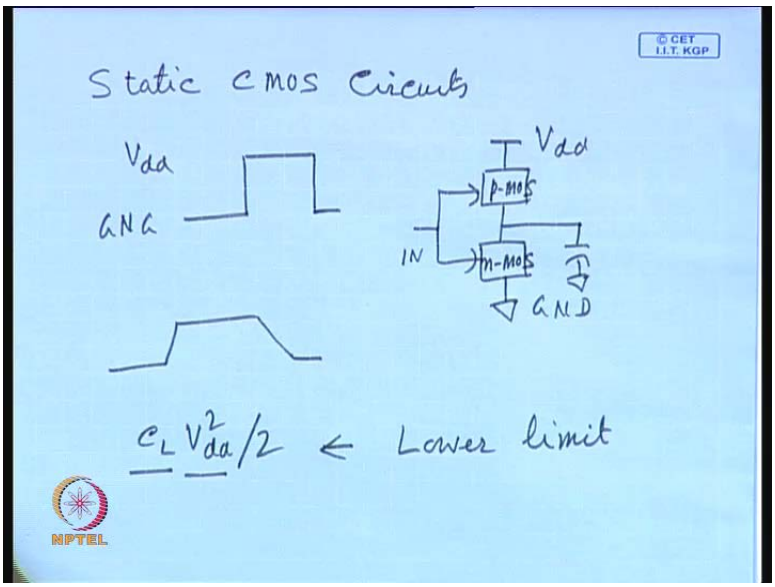

They are known as, as you know static CMOS circuits, static CMOS circuits and in static CMOS circuits we have seen that, there is a voltage swing between V d d and ground. So, there is a rail to rail voltage swing and as we know the basic implementation, which

is being done with the help of 1 p mos and 1 n mos logics block. So, we have got this is the p mos and this is the n mos and output is taken from here, input is given here.

So, here the output swings between may V d d and ground and we have seen that, this is very a successful technology, with lot of cad tools available and most of the v l s i circuits are nowadays realized by using this technology. But switching power dissipation of CMOS circuit with capacitive load has a lower limit of C L V d square by 2. We have seen, that whenever there is a switching, I mean may be from 0 to 1 or from 0 to 2, there is a transfer of energy, I mean there is a dissipation of power dissipation of C L V d d square by 2. This power dissipation always take place in each in switching and total energy transfer from the battery or power source may be C L V d d square, but half of that energy is dissipated. When it charges; when the capacitor charges and remaining half is dissipated. When the output goes from high to low? That, we have already discussed that.

That means and that is the reason, why in conventional circuit to reduce power dissipation. We tried to reduce the supply voltage, known as supply voltage scaling or we tried to reduce the capacitive switch capacitive as long as the c L is fixed, V d d is fixed; this is the lower limit of energy loss part switching. This cannot be changed. So, you can say this is the lower limit.

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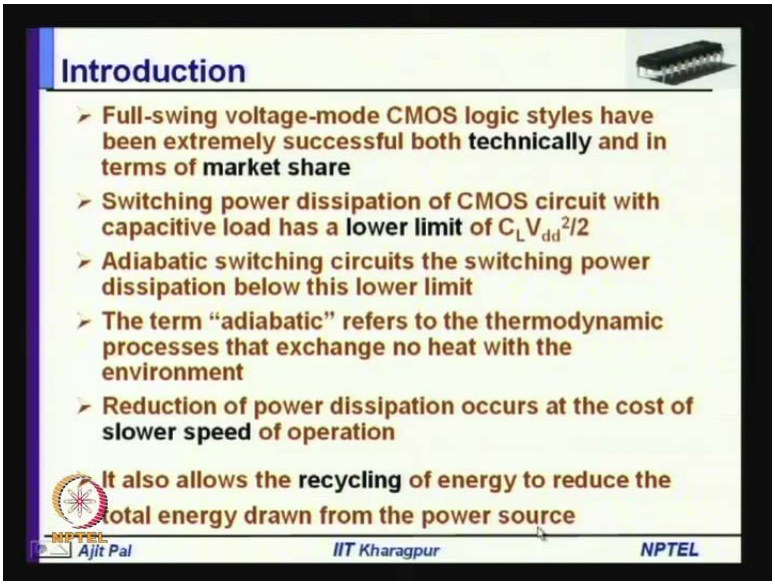

The the power dissipation switching power, that may dissipation cannot be lowered than, this one by using this conventional static CMOS circuits. Now, is there any way we can do it. The other alternative is adiabatic switching circuits, where the switching power dissipation is below this lower limit; that means, we shall be doing the switching in such a way, that the energy dissipation; that means, energy loss per transition will be lower than this.

That means and that can be done by using a technique known as adiabatic technique. This term adiabatic, has been taken from thermodynamic processes, as you know adiabatic systems do not release energy to the environment or do not take energy from the environment. These are the typical characteristic of adiabatic systems; that means, no energy is transferred from the system to the environment. So here also, that is the basic objective, but how far that goal is successful that, we shall see but this term has been taken adiabatic term, has been taken from this thermodynamic process that exchange no heat with the environment.

So, in this in at thermodynamic systems, essentially heat is the energy and in fact, in our logic circuits also ultimately, the energy is transferred to the environment in the form of heat. Now, reduction of power dissipation occurs, at the cost of slower speed of operation later on, we shall see in adiabatic systems, the reduction in power dissipation, will be taking place at the cost of speed; that means, we shall be trading, I mean at the cost of slower speed in other words adiabatic circuits, will be slower and why that we shall understand very soon.

Moreover it also allows, the recycling of energy to reduce the total energy, drawn from the power source and another approach, which is being followed in adiabatic circuit is to recycle the energy; that means, whatever energy has been transferred from the power source to the circuit, will be transferred back after some computation is done back to the power source. So, that is that is the reason why these are also known as reversible logic circuits; that means, you are transferring energy from the power source to the circuit and again, you are recovering, that energy by transferring back from the circuit to the power source. How can it be done that we shall discuss little later on.

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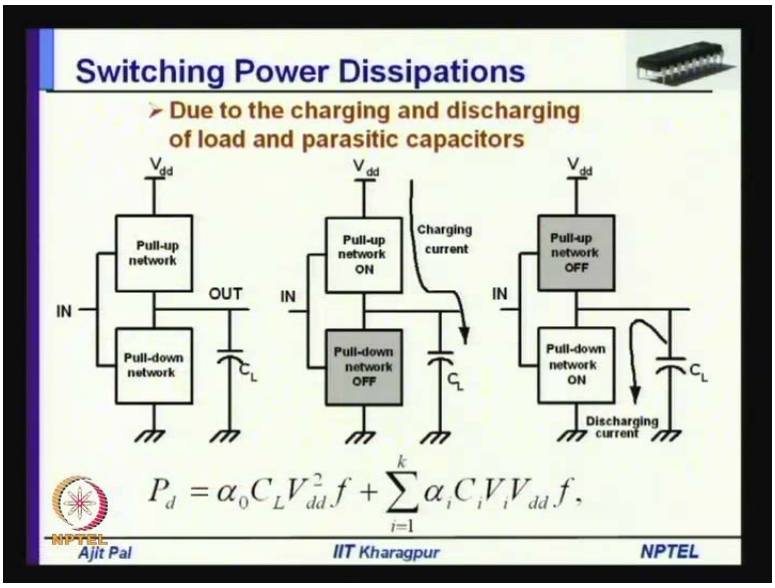

And you you are familiar with the switching power dissipation in static CMOS circuit, we know that charging and discharging take place, leading to this switching power dissipation.

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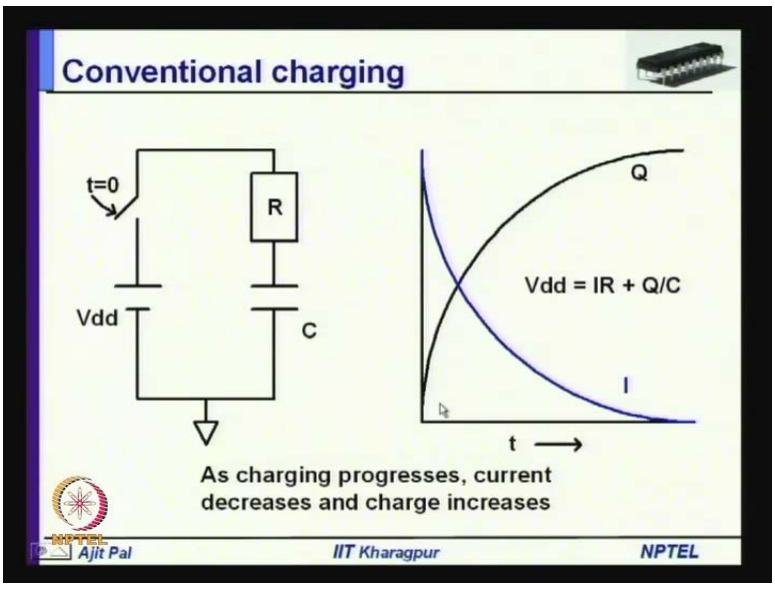

Now, let us focus on the charging process of a capacitor.

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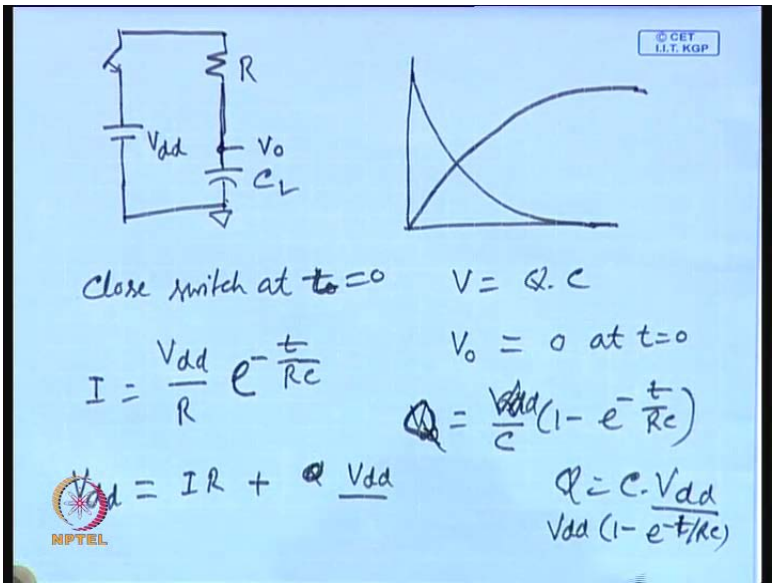

We have a capacitor. This capacitor is typically the load capacitance or it can be any capacitance, this capacitance has to be charged simplest circuit by which you can do it is that, suppose this is your a power source V d d and you can put a a switch and then you can put a resistor and as you close the switch close switch, at t is t is equal to 0, t is equal to 0 then what will happen? this capacitor if, there is no charge initially initially at t is equal to 0, the charge in this capacitor is zero then, it will start charging and as we know in in case of whenever you are charging through a resistor, this is your R and this is your c or c l. Whatever it may be, we know that the initially the current will be current, will be maximum because the voltage across the capacitor is zero. So, the entire voltage will be developed developed across this resistor. So, if this is the voltage V d d then, a current of V d d by R will flow initially.

Then of course, this current will keep on decreasing with time and it will become eventually zero, asymptotically it will approach zero and the corresponding equation of current is I is equal to as you know is equal to e to the power minus t by R c; that means, it depends on the time constant and the rate at, which it will discharge. So, this is the typical current, drop I mean current current that flows in the circuit. Now, if we consider the voltage that is developed across the capacitor. The voltage rises in the opposite way; that means, initially this voltage across this capacitor is say v o let us; assume the voltage here is v o initially it is 0 at t is equal to 0 and then, v o will be equal to Q by C into 1 minus e to the power minus t by R c; that means, the voltage will gradually rise and

eventually it will become equal to equal to you know that V d d it will become equal to V d d.

So, we find that, what is happening in this case V d d? This is the voltage across it will be equal to I R; that means, this has to be multiplied with R. So, it will be equal to I R plus Q by C it will be v zero is equal to v zero into it will be V d d by I believe V d d by c v zero will be equal to V d d by charge is equal to charge actually, I have written it wrongly charge Q by C; that means, v is equal to Q into C; that means, v is equal to Q into C. So, it will be actually expression for Q charge that, is built up is equal to V d d by C into one minus p by R c. So, it will be this this this plus V d d by Q by C something wrong, Q is equal to V d d by Q is equal to I have q is equal to c into V d d.

So, in this particular case this will be changing. So, it will be equal to, it will be a changing and that will be equal to V d d by into one minus one minus e to the power minus t by R c so; that means, this V d d is is not a constant in this case you can say it is t v t. So, it will be V d d into one minus t by R c. So, this this will become equal to I into R plus Q by C; that means, V d d will be equal to I R into Q by C.

So, we find that with as the time progresses, this I R is this voltage will gradually come down, because current will gradually reduce on the other hand, this will go up; that means, Q by C will go up and as a constant as a consequence V d d will remain constant; that means, we find that the initially voltage drop across the resistor is maximum, whether voltage across is zero then, as the time passes voltage drop across the resistance will become zero and voltage drop across the capacitor will become equal to V d d. So, this is how the charging occurs, but irrespective of this mechanism, we know that the energy transfer is equal to C L V d d square part, I mean whenever it switches from zero to one, that we have seen and energy of C L V d d square by two will be lost, in this resistor even if it is instead of a resistor, if we put a constant current, I mean if, it is a instead of voltage, if we instead of voltage, if we put a constant current source even then, that will take place.

That will that, this will be linear and this will be also linear; however, that energy, so far as the energy dissipation is concern that, will remain same, so irrespective of the nature of voltage that is being applied or if it is charged for a constant kind. So, this will happen.

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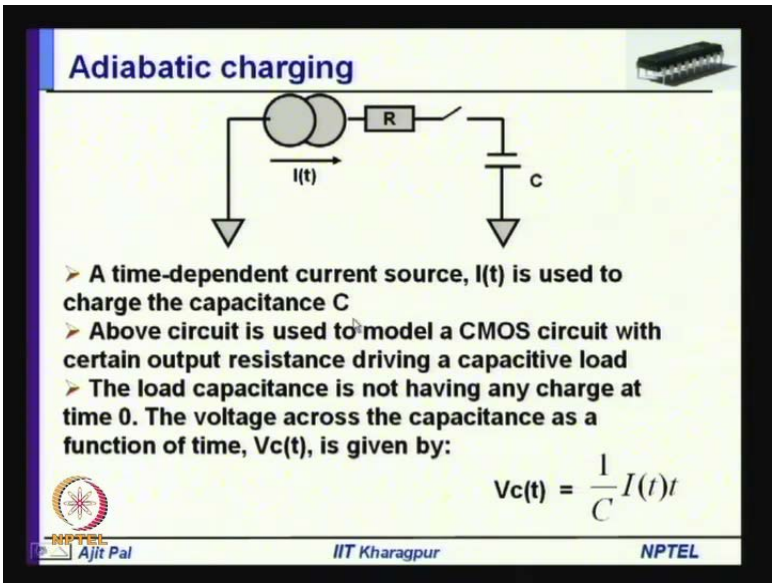

So, this is the typical conventional charging. Now, let us consider a situation.

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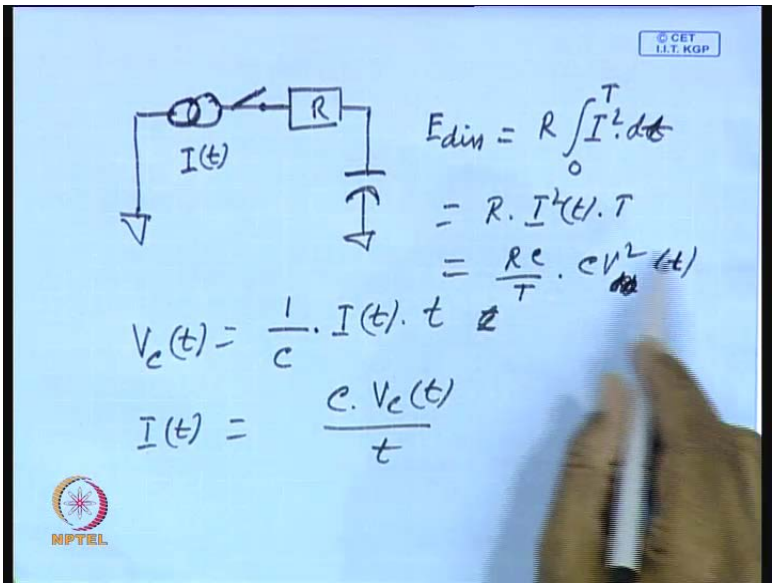

Where, we shall use a current time varying current I t. I t which is being applied across a resistor R and you have got a capacitor c of course, we can put a switch in between here we can put a switch. So, at time t is equal to 0 the charge across this capacitance and so on.

So in such a case, what we were trying to do this current is no longer constant and in such a case let us sees, what will be the equation for current. So, a time-dependent

current source I t, is used to charge the capacitance C and this circuit is used to model a CMOS circuit with certain output resistance. Driving a capacitive load so; that means, we are trying to model a CMOS circuit later on, we shall see how it can be modeled.

So, the load capacitance is not having any charge at time zero, as I have told and the voltage across the capacitance, as a function of time V c t is given by V c t is equal to 1 by C into I t into t. So, this is the 1 by c into current into t, that is how the charge will take place and what is I t and I t, that is time varying current will be equal to c into V c t by t let us assume this time varying current is arising, because of this variable voltage which is a time varying voltage that is being applied across it.

So, if we substitute this, here in this particular expression. We get V c t we substitute not in this equation, but we shall try to find out the energy dissipation is equal to R into I square into d t as you know, I square as the is the dissipation and over a time period t. So, let us assume zero time taken to charge to a to a particular voltage level is time t. So, if we substitute these value here then, we get R into I square t into t is equal to R c by t into c say c v let me let us assume v d square let let it not be since, here time varying time varying voltage let it be v square t.

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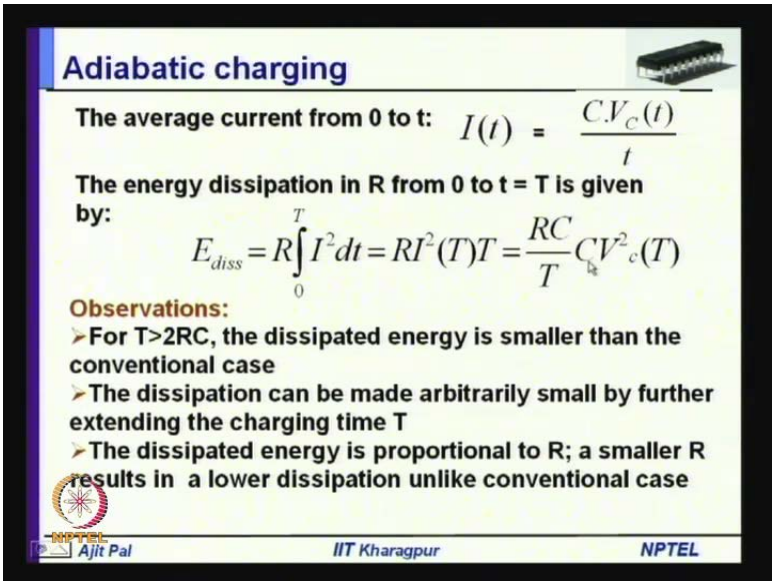

So, we find that in this particular expression, we are observing that it is R c by t into c v d square into t. Now, in what way it is different from our previous expression let us consider the case.

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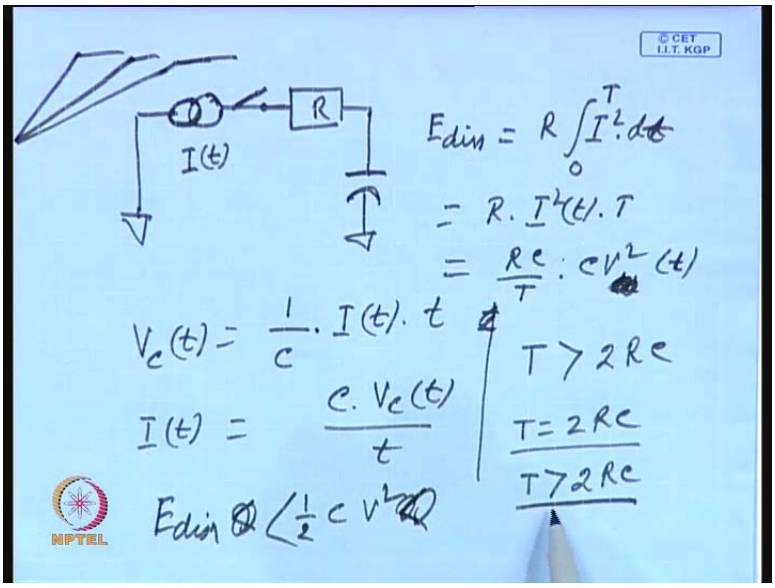

When, T is greater than 2 R c. So, if you can substitute 2 R c here. So, if we substitute 2 R c greater than 2 R c here then, what will happen when t is equal to 2 R c then, this value will be will become equal to half c V d d square. So, that means, the V c t square v t square. So, that will be the voltage whenever, that is that will be the energy dissipation when t is equal to R c. Now, if we can make t greater than 2 R c then, what will happen then; obviously, this will be lesser than half c V d d square t; that means, this expression will become less than half c v square because t is greater than two R c.

So, since it is less than sorry it will be less than half c v square. So, this power dissipation energy dissipation is less, let me write here e dissipation will be less than half v v c v v squared, whenever t is greater than 2 R c. Now, question naturally arises how we can really make t larger than 2 R c? That is quiet easy to do because we are applying a voltage which is time varying.

So, we can instead of applying the voltage to rise quickly, we can apply another voltage, which rises more slowly more slowly and like that. So, we can apply a voltage of this type; that means, which rises very slowly and as a consequence the time, that t can be made, I mean we can make larger than 2 R c; that means, this time can be made much larger than 2 R c. So, whenever we make T greater than 2 R c then, what is happening we are able to reduce the energy loss power switching less than half c V d d squared.

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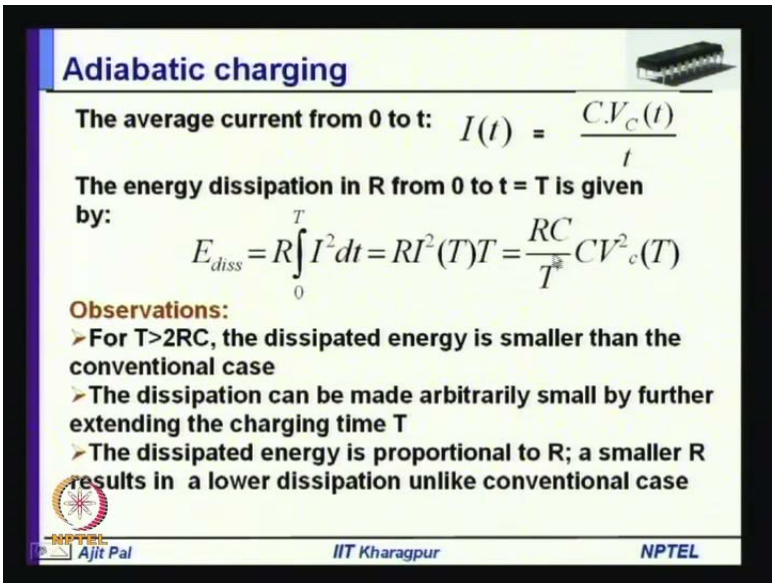

Is there any other way to reduce it, another alternative is you know that, first is time, and second is there is another very important parameter. Earlier, we have seen this resistance was not part of this expression, because the dissipated energy is proportional to R. This R was not present in our earlier expression. So, in this R was not present in our earlier expression. So, by making t larger than 2 R C, that is one one possibility of making it smaller than half c V d d squared v c square another alternative is to reduce the value of R to make it smaller than half c V d d squared.

That means, the dissipated energy is proportional to R a smaller. R results in lower dissipation unlike, conventional case because in conventional case as we have seen R does not figure out in this expression. Because in this expression, whether you are charging with a constant voltage or a constant current irrespective of that R is not present in this expression, but in this case that in case of adiabatic charging. We call it adiabatic charging, when the voltage is slowly applied time, varying voltage is applied which gradually rises from zero to V c or V d d then; obviously, an expression in the expression R is appearing. So, this is how we can reduce the energy dissipation this is the basic idea behind adiabatic charging.

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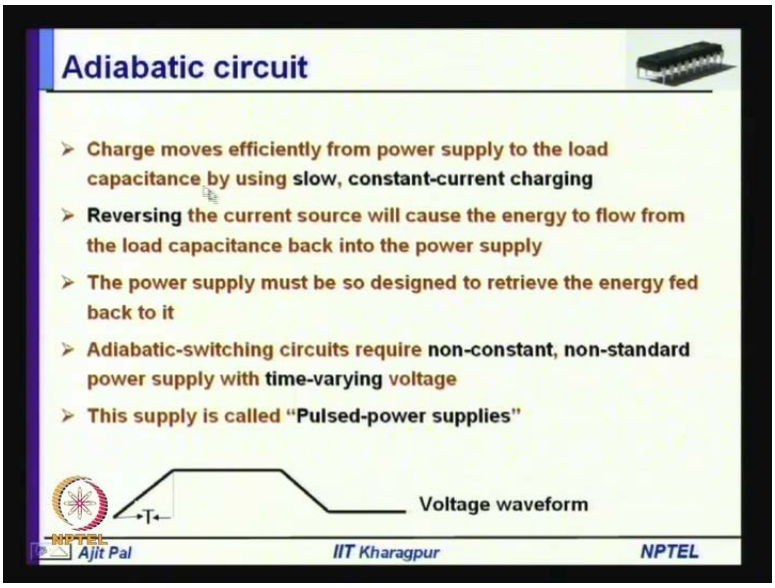

So, charge moves efficiently from power supply to the load capacitance by using slow, constant, current charging.

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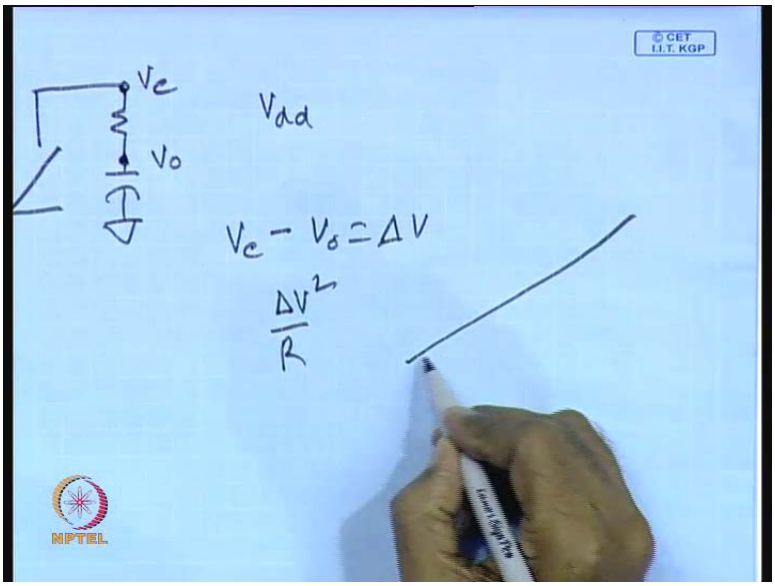

So, you may be asking, what is the basic physical phenomenon involve in it, basic idea is very simple, you see we you have got a R and a c and if, we if we apply a constant voltage here then, what happens initially as we have seen there is a voltage of V d d. Which is present across this R? So, maximum current flows and subsequently of course, it decreases as the voltage builds up here.

Now if we apply, a voltage which is somewhat like this and in that case, what happens if we can make this voltage here say this is your V c and voltage here v o this difference is very small; that means, V c minus V o is equal to delta V, that is very small then power dissipation across this will be you know delta V d squared by R; that means, by if we can make this difference voltage small then very small power dissipation will take place that is the basic idea.

In fact, by making it you know by extending the time t, that is precisely we are doing that voltage difference between this output of this capacitor and that is applied to the resistor that is becoming smaller and smaller and that is leading to smaller power dissipation in this resistance. So, that is the basic idea behind adiabatic charging.

Now, reversing the current source will cause the energy to flow from the load capacitance back into the power supply. So, the power supply must be designed to retrieve the energy feedback to it, that is the that is to I mean realize the reversible circuit. So, adiabatic switching circuits require non-constant, non-standard power supply with time varying voltage like this. So, it will charge from zero to a voltage let it be V d d in time t and the supply is called pulsed power supplies and we shall see, how we can transfer back the energy to the power supply from the circuit.

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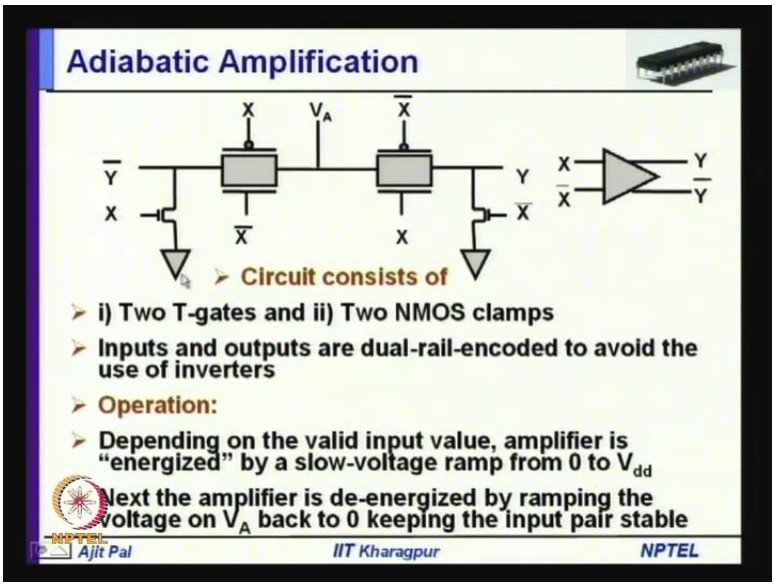

So, this is the a adiabatic amplification circuit circuit consists of two transmission gates as you can see, you have got one transmission gate here another transmission gate here

and inputs and outputs are dual-rail-encoded to avoid use of inverters, you know if we do not use dual rail then, you have to use static CMOS inverters and if we use static CMOS inverters, that will lead to you know that non adiabatic charging and discharging. So, to avoid that in adiabatic logic circuits, you will always use dual-rail-encoded circuits; that means, you will be realizing both Y and Y bar.

So, you may consider it is an inverter or buffer. So, you see here you are applying a time varying voltage V A here. So, initially what is happening depending on the input x, you know depending on this input that, we applied here x that is also applied across the switches one of the path will become one of the output will become high and one of the output will become zero. So, the output which becomes high, I mean the capacitor at that point will charge through, this through this through this transmission gate on the other hand, when the output is zero, that discharge will take place not only through this. I mean, will primarily take place through this transistors; that means, when this is high, this output will be zero and when x is bar is zero then then this will be high.

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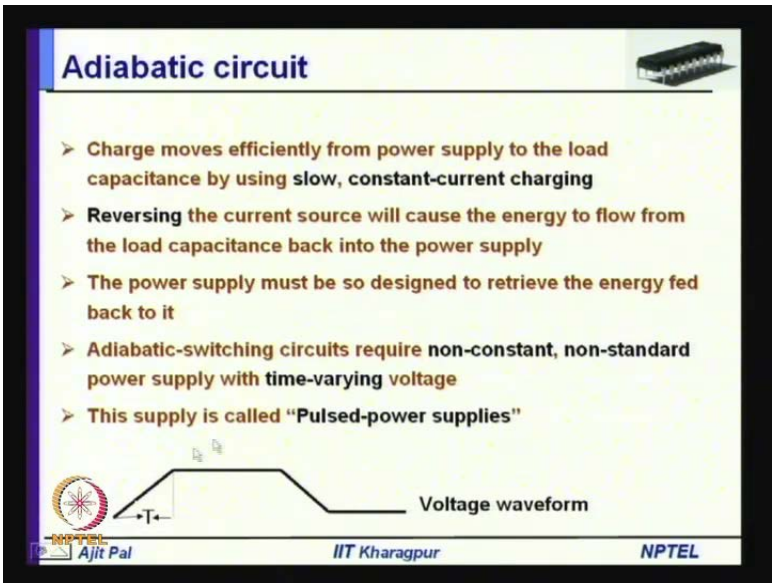

So, this is how this two transmission gates can be used to realize adiabatic amplification. So, what we are doing here depending on the valid input value amplifier is energized by a slow-voltage ramp; that means, we are applying this voltage and gradually charging it and the corresponding point, one of the output will become high and one of the output will become low then, these output values are used during this period sorry during this

period it will be used this, will remain stable during this period; that means, it will fed the succeeding stage. During the stable period then, after this stable period is over, what will happen this voltage will gradually ramp down and in that case, what will in that case the charge those are the which stored in this node will be transferred to the power source. Back to the power source; that means, what is happening the you are transferring energy during this phase to the circuit and during this phase, you are transferring back the energy to the from the circuit to the power supply. So, that is how reversible operation is taking place and you will require, this kind of supply voltage.

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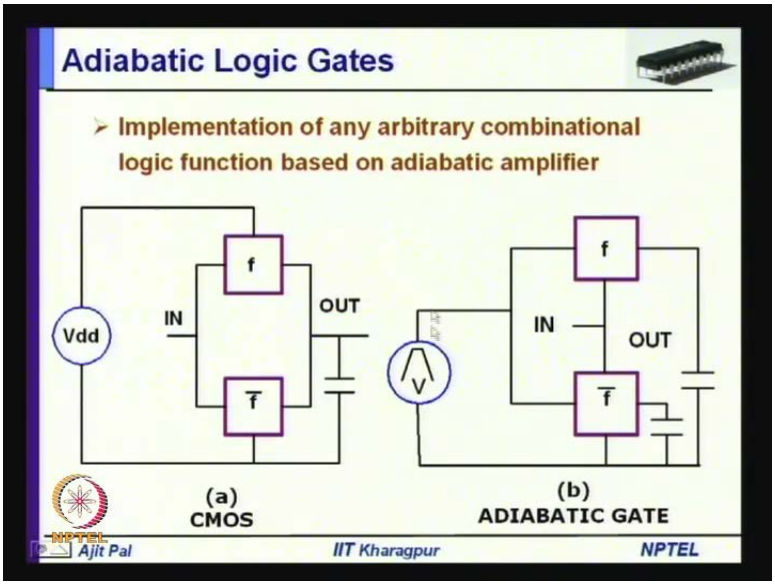

Now, how do you really realize adiabatic logic gates by using this type of circuits? So, we have a supply voltage V d d and this is the traditional you know that, traditional CMOS circuits you may recall that, we realize f bar that corresponds to the n mos network and here is the p mos network that, essentially is that this path is open when f is one.

So, this is the traditional CMOS circuit, where you apply constant voltage V d d and there is a load capacitance c l s. So, this is being modified to realize a adiabatic circuits. So, in this case we are applying the input here and we have two outputs f and f bar. This is f bar and this is f and instead of using a fixed voltage here, we are applying a time varying voltage, that pulsed power supply that I mentioned earlier, you know that this pulsed power supply that is being applied to this input.

So, to this input you are applying that; that means, the circuit which is realizing f as well as the circuit, which is realizing f bar to both the circuits. We are applying this pulse power supply and we are applying the input to both of them. Then, we are getting 2 outputs; obviously, one will be out and another will be out bar for f for f bar.

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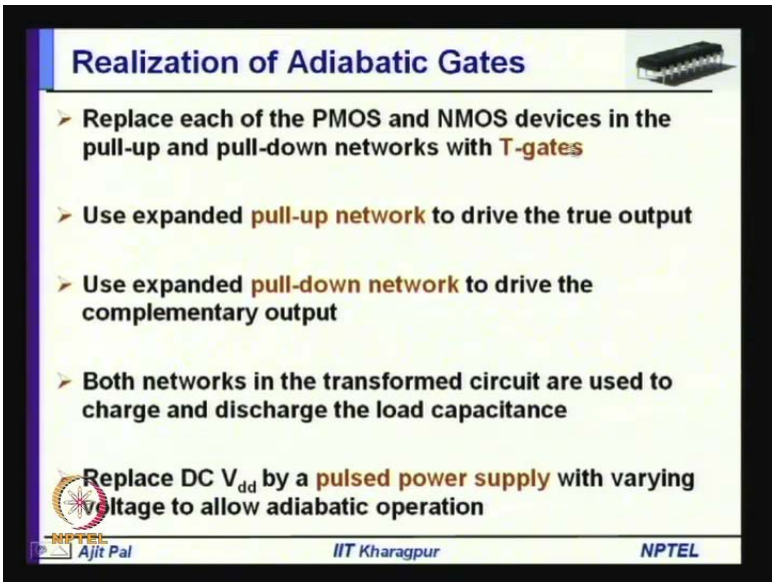

So, let me illustrate this with the help of let before that, let me explain how exactly you can realize a any gate by using this basic steps are like this replace each of the PMOS and NMOS devices in the pull-up and pull-down networks by T gates Transmission gates. So, whenever you are using realizing this circuits; obviously, you will not be you will not be using NMOS network, which is used here or PMOS network that is being used here you will be replacing them by transmission gate then, use expanded pull-up network to drive the true output and expanded pull-down network to drive the complementary output; that means, we are driving these two networks with the help of transmission gate circuit and both networks in the transformed circuit are used to charge and discharge the load capacitance and replace V d d d c V d d by a pulsed power supply with varying voltage to allow adiabatic operations.

So, these are the steps that, you have to follow in converting a standard static CMOS gate to a corresponding adiabatic gate and here for example, the realization of a and n and is shown.

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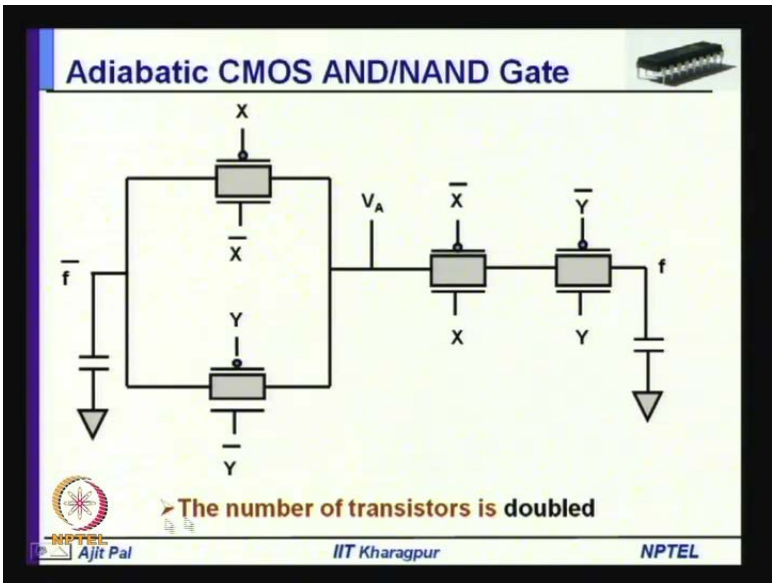

So, you can see here this V A, which is that pulse power supply that is being applied and this part this is a two transmission gate. Which is driving a capacitor and which is realizing f; that means, whenever they this is a and NAND gate; that means, when both of them are one you see both of them are 1; that means, this path will be close only then, this will become this output will become 1 and when both of them are 0 or any of them is 0 then, when any of them is 0 then, in case of NAND gate. So, this will be the output of and this will be the output of NAND; that means, it will realize NAND opposite of AND. So, NAND means if any of the input is 0 then, there is a path through this because zero means this transistor will be on or this transistor will be on. So, there will be a path. So, this will realize and NAND function and you will apply a pulse power supply here.

So, we can see by following the step that, I mention we have realized this and NAND network, we have converted this circuit, I mean the static CMOS and gate NAND gate into a corresponding adiabatic CMOS and NAND gate, because it will realize both AND and NAND, that because it is dual railed logic , but one point you must notice here the number of transistor is doubled.

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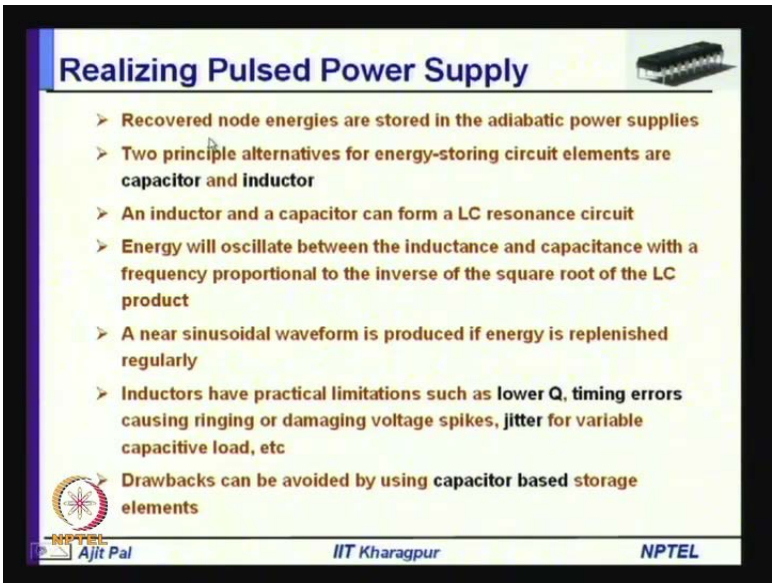

So, here as you can see earlier if you realize a two input NAND gate, you will realize two and that means, 2 plus 2 4 transistors, but here the number of transistor is 1 2 3 4 5 6 7 8. So, number of transistor is doubled, whenever you go for adiabatic CMOS logic circuit realization, moreover you have to put lot of effort in realizing this pulse power supply and particularly realizing pulsed power supply is a little difficult task and it has to be design in such a way that, recovered node energies are stored in the adiabatic power supply and two principle alternatives for energy-storing. Circuit elements are capacitor and inductor as you know, you have to use some energy storing device in the pulse supply and typically in electronic circuits or electrical circuits, you can use either capacitor to hold charge or you can use inductor. So, either inductor or capacitor can be used to for for for storing energy and another alternative to use both.

So, inductor and capacitor can form a L C resonant circuit; that means, energy actually switches back and forth between l and c and then, that way you can realize the pulse power supply. So, it will act like a resonant circuit. So, energy will oscillate between the inductance and capacitance with a frequency proportional to the inverse of the square root of the L C product; that means, the f will be equal to 1 by root L C. So, that is the frequency of oscillation.

So, you can generate a (()) sinusoidal form if, energy is replenished regularly. So, induct, but unfortunately whenever you are going for v l s i realization of an inductor is very

difficult, particularly the inductor realized by using v l s i circuit on a chip. We will have very low q. The q value is very low and have there are many limitations like lower q timing errors causing ringing or damaging voltage spikes (()) for variable capacitive loads and that is the reason, why instead of using inductor particularly capacitive capacitor based storage elements are normally used in realizing pulse power supply. We are not going to the details of realization of pulse power supply, that is a you know area of research, how we can realize pulse power supply very efficiently? The efficiency has to be very high. Otherwise, you know if the power supply if not efficient, whatever gain you achieve in adiabatic circuit will be lost in the power dissipation of the power supply. So, that is also a very important area of research realizing pulse power supply in adiabatic circuits.

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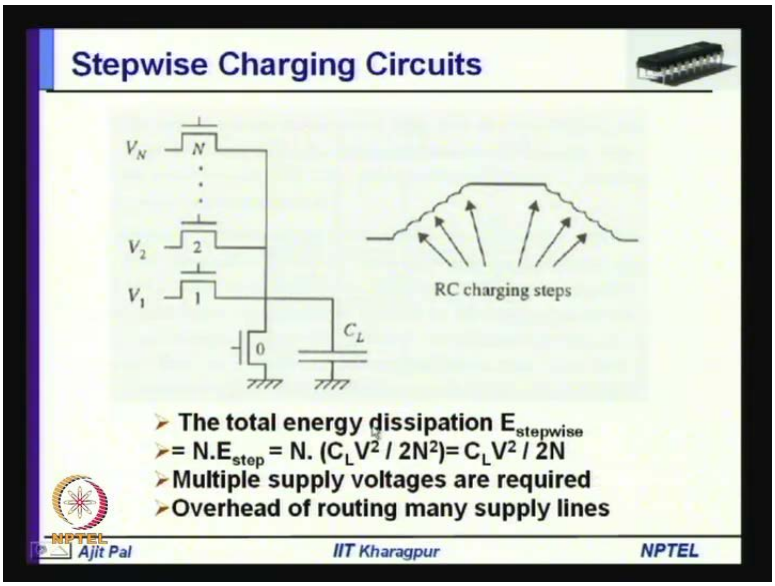

Anyway, let us consider another alternative by which a capacitor can be charged adiabatically. So, here what is being done a stepwise charging circuit used, what you really mean by stepwise charging.

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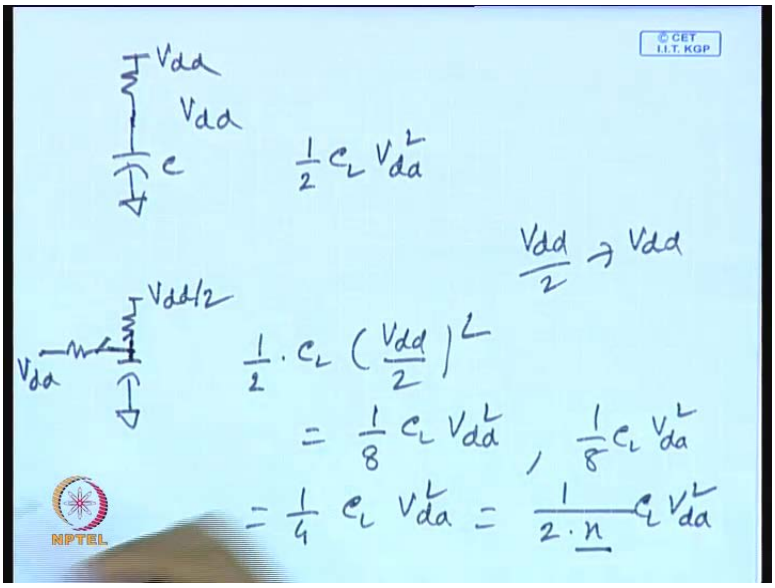

So, instead of charging a capacitor say, you have got a capacitor instead of charging it directly to a voltage V d d through; obviously, it will be through some resistance. So, instead of applying a voltage V d d then, it will charge to charge to V d d. This capacitor and you that power loss of C L V d d squared, will take place instead of doing that, what you can do let us assume first, we charge the capacitor to say V d d by 2 then, how much energy will be lost in charging half c l into V d d by 2 squared, that is your that is your 1 by 8 1 by 8 C L V d d squared.

Now, now let us assume another supply, you apply where when you after this charging is over now you charge it to V d d after it has been charged to V d d by 2 now, you apply this switch is closed after, you know this charging has taken place and this this this is now turned off. So, you have two switches here, first this switch is closed to charge it to V d d by 2 then, this switch is closed to charge it from V d d by 2. V d d and again in that case what will happen there will be another. In that case, what will be the power loss again there will be a since, it is charging from V d d by 2 2 V d d. So, a a loss of c l one by 8 C L V d d square take place; that means, it will be if you put them together, it will be 1 by 4 C L V d d squared.

So we find that, this can be represented as one by half into n C L V d d square if we generalize it that, we shall be charging by using n steps. So, where n is equal to 2 in 2 steps then, it is 1 by 4 and suppose you use n steps and that is what is being shown in this

diagram. We are using n steps in charging this capacitor. So, initially this capacitor is discharged with the by turning this transistor on. So, the voltage is 0.

Now, first you this switch number 1 is closed, it will charge to a voltage v 1 then, the switch will be turned off. Switch v 2 will be closed it, will charge from v 1 to v 2. In this way it will go up to voltage V N in n steps; that means, whenever you do the charging in n steps then, the total energy dissipation by using a stepwise charging is equal to n into e step, that is equal to n into C L V d d squared by 2 n squared as, we have already seen. So, this will be equal to C L V d d squared by 2 n.

So what is happening here? Whenever, you do the charging in n steps, there is a the power energy loss for charging from 0 to V d d or in this case, v let us assume which is 1 by n times smaller compared to if, you do it in 1 step. So, if we n if we make say suppose n is 8; that means, the power dissipation will be 8 times smaller than the traditional energy dissipation that, take place in one step charging.

So, this will require multiple supply voltages. So, we have seen here, the switches can be easily realized, but you have to you have to realize multiple supply voltages. So, from a single supply voltage you can generate n supply voltages and then, n supply voltages are to be present here; obviously, this will increase the cost of implementation, not only that, you have to do the routing that, power real routing for all these n supplies to the circuit and as I mentioned the you can do the charging the way you can do the charging, you can do the discharging at well so; that means, you can also transfer transfer the energy back to the source by reverse operation, that is discharging the capacitor in the reverse order.

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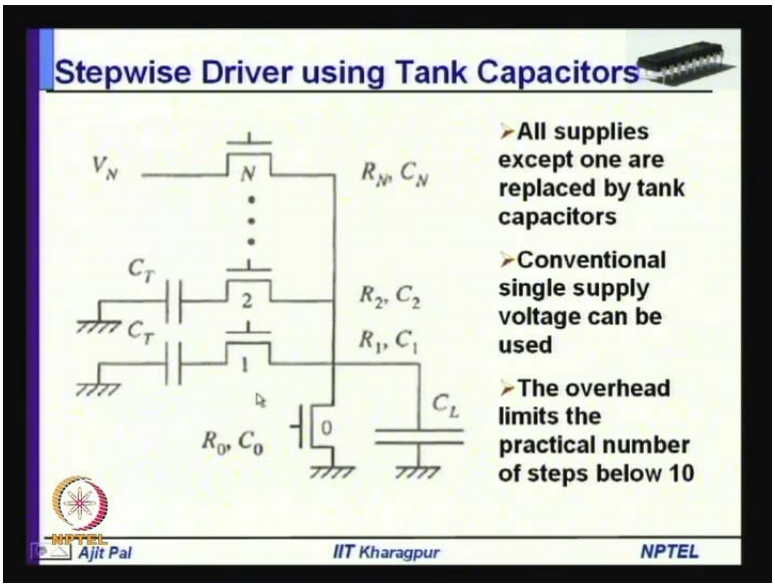

So, whatever way you, do you will require n power supplies and n power supplies have to be connected to the capacitor while using this circuit. So, the stepwise charging can be done, but number of power supply requirement is high another approach is to reduce the cost of implementation is to use capacitor tanks, you know what is being done little larger capacitors are used to hold, the value of different voltages; that means, what you will be doing say suppose, this is the voltage V N now, what you will do you will selectively turn on these transistors to charge these tank capacitors to some voltages to different voltages like, earlier we have seen voltage V 1. So, you will charge this capacitor to voltage v 1 then, you will charge this capacitor to V 2 and so on.

So, you will require n minus 1 tank capacitors, which will be tank capacitors are essentially capacitors of little large value this is because that they can supply energy for the operation of the circuit, during its normal mode of operation. So, all supplies except one are replaced by tank capacitor and conventional single supply voltage can be used. So, this is your conventional single supply voltage and overhead limits the practical number of steps below 10; obviously, this will also will have overhead like the previous case and whenever, we use this approach for generating the you know those switched power supply then, the number of steps that, can be used in practical circuits is limited to 10. It cannot be because of large overhead. We cannot really have large number of steps, but larger the number of steps the reduction in energy is more; however, because of practical limitations this is not being done.

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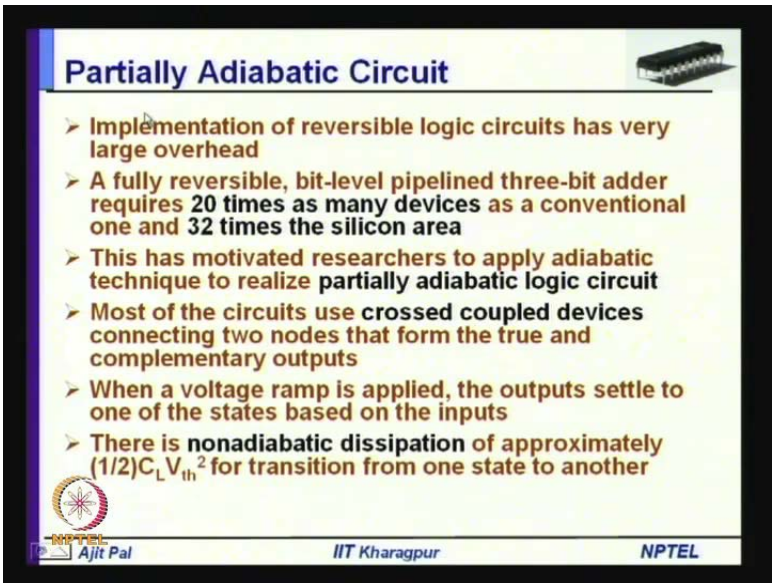

Now, as I have told this implementation of fully adiabatic circuits are very expensive. You will require large number of transistors, it has been found that, a fully reversible bit-level pipelined three-bit adder requires, 20 as many devices as a conventional one and 32 times the silicon area. So, we can see it has got very large overhead. So, this has motivated researchers to apply adiabatic technique to realize partially adiabatic logic circuits. So, instead of using fully adiabatic logic circuits partially, adiabatic logic circuits can be used to reduce the I mean a in with some compromise, but still significant reduction in power dissipation.

How can it be done? So, you will see that most of the partially adiabatic circuits use crossed coupled devices; that means, a flip-flop like crossed coupled devices, connecting two nodes that form the true and complementary outputs, when a voltage romp is ramp is applied the outputs settled to one of the states based on the outputs; that means, in this case we do not really use transmission gates rather than, we use traditional NMOS and PMOS transistors; however, there is a non-adiabatic dissipation of approximately half C L V t square for transition from one state to another. I shall explain that, as I discuss a particular type of circuit.

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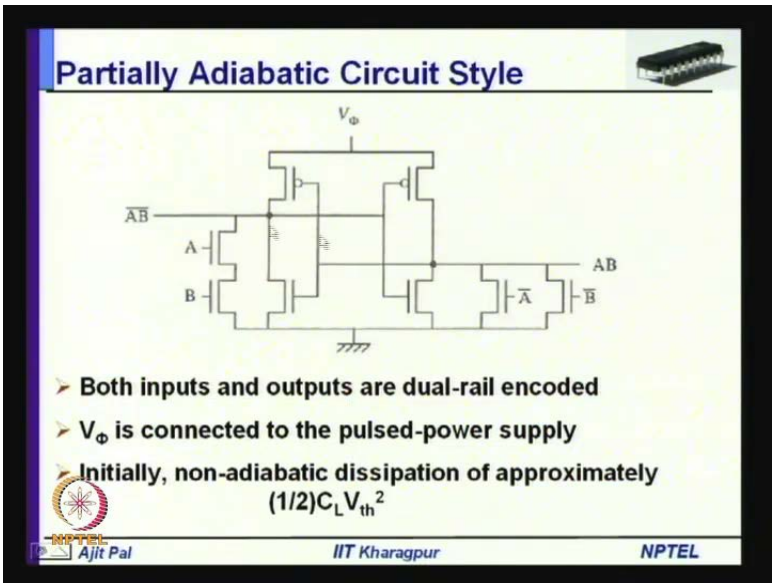

Let us, consider this is a partially adiabatic circuit style one of the partially adiabatic logic style see here, as you can see we have got we have got pulsed power supply applied here then, two inverters which are connected back to back and then, you know those this is these two inverters are connect to connected back to back then, we have these NAND these PMOS NMOS transistors A B and here A bar B bar NMOS transistor connected in parallel.

Obviously, they are realizing the complementary functions. Which are connected in parallel with these n mos transistors of those inverters? So, both inputs and outputs are dual-rail encoded and v phi is connected to the pulsed power supply. This one and initially there is non-adiabatic dissipation of approximately half C L V t squared. What is the reason for that, you will see that, depending on the inputs A and B, you know one of the output will be 0, when this input is 0 then, this out this 1 voltage will be 0 0 means this transistor will be on provided the voltage here is greater than this by a voltage of v t h. Otherwise, this transistor will not turn on. So, this will be minus v t this is voltage has to be minus v t h with respect to this. So, as you know this pulse power supply is charging from zero.

That means, initially this v phi is 0 at time t is equal to 0 and up to this time say some sometime t 1, this voltage is not reaching v t h p; that means, the v t h with the threshold voltage of the PMOS transistor then, what will happen; that means, this transistor is not

turned on; that means, no adiabatic charging is taking place of this node for, this part of the circuit so; that means, this particular part of charging is taking place non adiabatically and as a consequence, there is a energy dissipation of half C L V t square subsequent part of course, will be adiabatic charging; that means, the output voltage will follow the these voltage.

So, but initial part will not follow, it will be as if suddenly after sometime a voltage of v t h is applied here, then it will charge to 0 to v t h the initial part. So, these kind of this this this happens this this non-adiabatic dissipation take place in this particular circuit.

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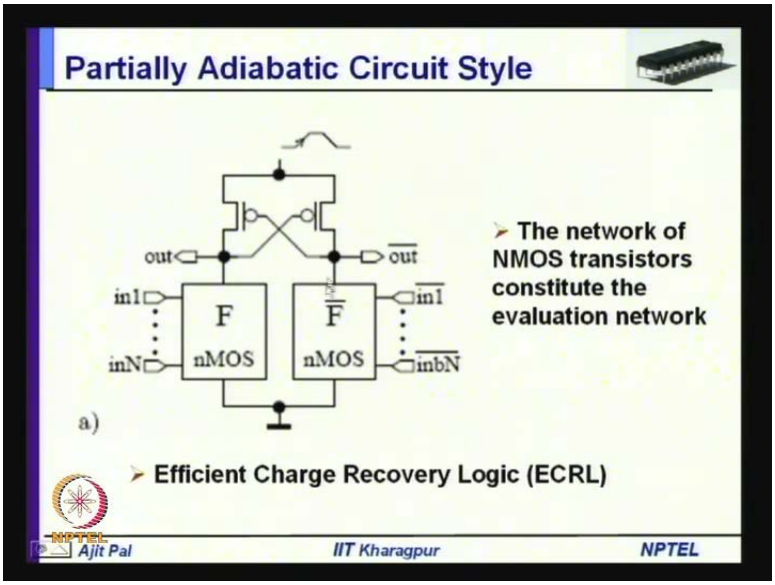

Now, there are several you now that, adiabatic logic circuit families. I shall briefly mention about them, one is partially adiabatic circuit style p, that is your that is actually this is a this is one of the partially adiabatic circuits style known as e c e ECRL energy charge recovery logic here. You can see two p mos transistors are connected back to back in most of the partially in all of the partially adiabatic circuits actually, this type of cross coupling is used.

Now here, you have got two networks of n mos transistors. One is realizing F, another is realizing F bar. So, the network of n mos transistors constitute devaluation network. So, this is how you are realizing this this the the energy charge recovery logic and here also depending on the inputs; obviously, one of this this node will be, I mean that be discharge path through one of these nodes n mos transistors will turn on and one of them

will not be having any discharge path; that means, this if this output is I mean there is a discharge path this will be 0, this will turn on this transistor and that will charge this output to 1.

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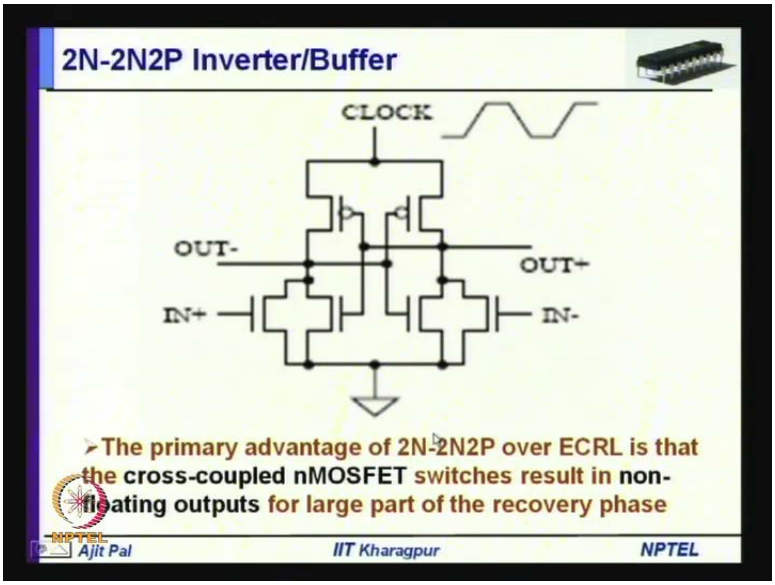

So, this is how one of them will be charged to 1 and 1 of them will be will become 0 depending on the input combination, that you applied here and the circuit, that is being realized and there is another logic family logic circuit. Which is part of that partially adiabatic logic circuit family, which is known as 2 n 2 n 2 p 2 n 2 n 2 p logic style here, as you can see we have inverters then, we are having these n mos transistors connected in parallel with this n mos transistors of this inverters.

So, this is same as what I have explained earlier it is and how the NAND gate is realized by using this this is essentially this 2 n 2 n 2 p implementation of circuit. So, this is the inverter, that is being realized the primary advantage of this, 2 n 2 n 2 p over ECRL is that the cross-coupled n mos fed switches result in non-floating outputs for large part of the recovery phase; that means, when the you know recovery is taking place, these outputs remain floating for certain duration in this particular case and as a consequence you know the adiabatic transfer does not take place for that part and as a non-adiabatic loss takes place. So, that does not happen in this 2 n 2 n 2 p circuits and that is advantage of this logic style, over ECRL logic circuits.

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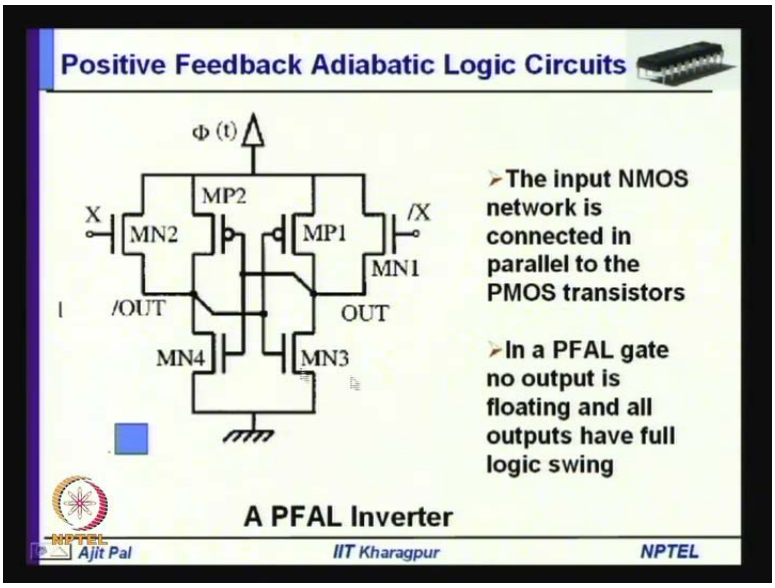

Coming to the third type, which is one of the most popular that is actually known as positive feedback adiabatic logic circuits PFAL. Here actually, instead of connecting the n mos transistor network in parallel, with these n mos transistors they are connected in parallel with the p mos transistor. So, you can see here, the p mos transistors are I mean these p mos n mos networks are connected in parallel to p mos network. So, the e input n mos network is connected in parallel to the p mos transistors.

So, in a PFAL gate no output is floating and all outputs have full logic-swing. So, that means, here also just like that, this 2 n 2 n 2 p circuit here also we get full-swing at these outputs and there is the outputs do not remain in floating condition. So, for major part of the circuit and as a consequence this is also advantageous and lot of simulation works have been carried out, I shall discuss about them.

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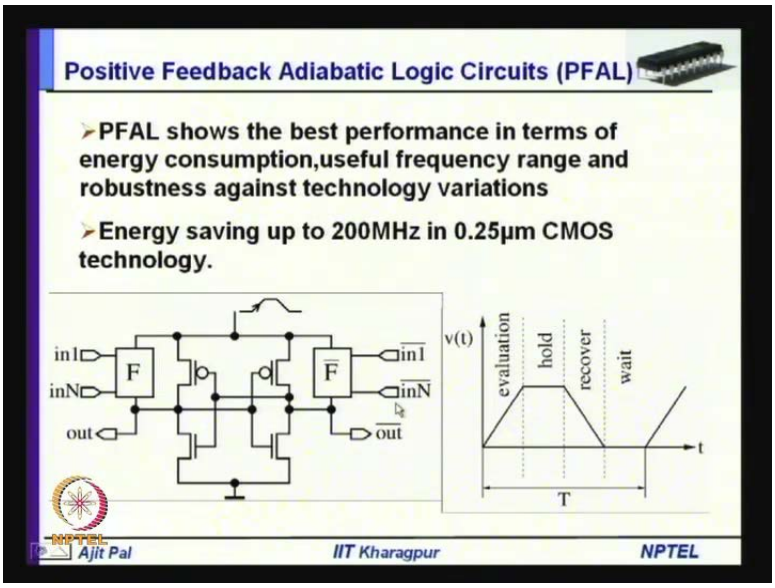

I shall give their results. So, PFAL shows the best performance in terms of energy consumption, useful frequency range and robustness against technology variations. So, this has been established by simulation that out of the three three members of the non adiabatic I mean partially adiabatic logic circuits that I have discussed this PFAL has been found to, I mean found to work better and actually the circuit operates in 4 phases as you can see.

During this phase, during this part evaluation take place evaluation take place means and in this part inputs are stable inputs are stable and output is charging from zero to some level say V d d and during this evaluation is taking place and accordingly these nodes these output nodes will charge to some certain values because depending on these input combination one of them will be will be output will be 0 and 1 of them will will be one.

So, this is the evaluation and after this evaluation phase, these outputs will have some output values depending on the input combinations and during this hold phase. This output will be applied to the succeeding stage and after that is being used by the next stage during, the hold phase that energy is recovered in the third phase recovery phase recover phase and the energy that, were stored in these node capacitors. Now, are transferred back to the pulsed power supply during this recover phase and then of course, this is the wet phase before another evaluation starts.

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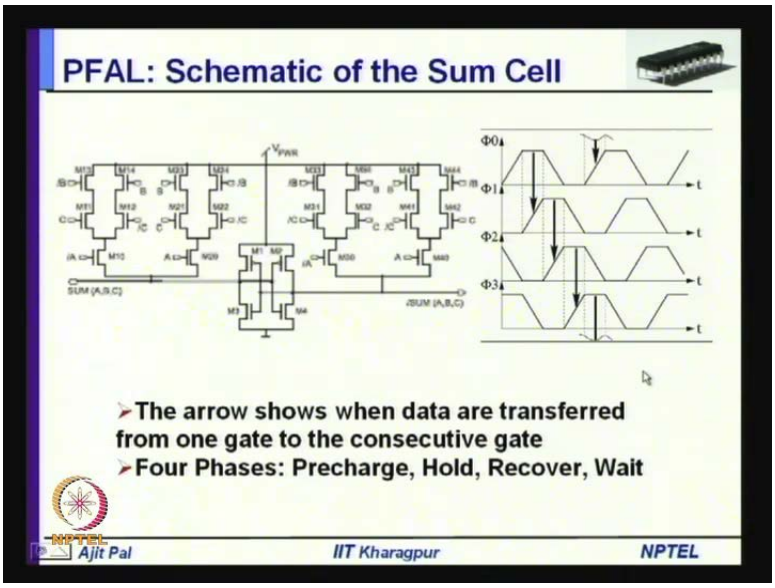

So, this is how the PFAL circuit works in a in 4 phases and you can implement pipelined PFAL circuits, using this approach for example, here how the 4 phases work and that is being shown here, this is realizing a sum cell. So, you can see this is this is this is the sum cells n mos transistor network one is your sum sum a b c; that means, it is essentially realizing 3 inputs, sum a b c and it is sum bar complement of sum a b c, that is being realized here.

So, the arrow shows when, the data is transferred from one gate to the consecutive gates, as I mentioned during this part it is getting transferred to the next next stage and similarly in this part, it is getting transferred to the next stage. So, by using this kind of 4 phase circuit, you can realize pipelined implementation of PFAL logic circuits. So, 4 phase 4 phases will be driving the 4 pipeline stages.

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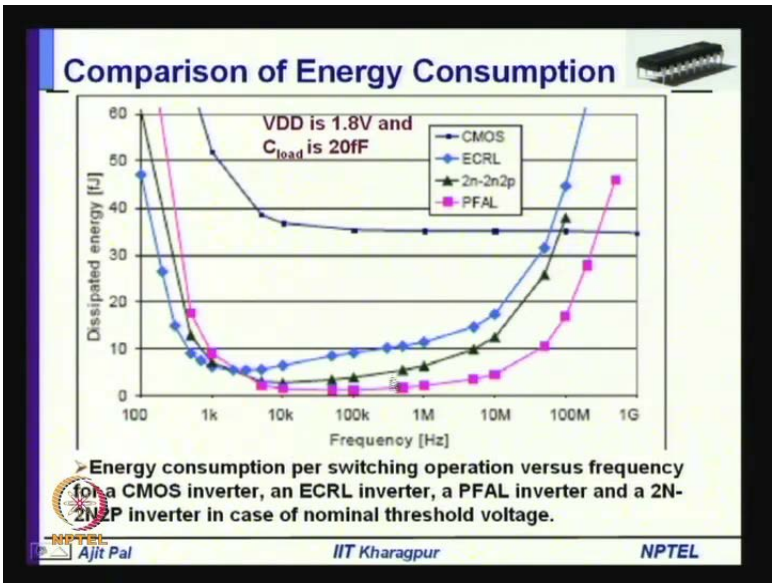

Coming to the comparison of energy, we can see here the top, one top line corresponds to the static CMOS and compared to that we it is being compared with ECRL 2 n 2 n t p and PFAL l; obviously, PFAL l is giving the maximum reduction in or dissipation of energy. So, energy consumption per switching operation versus frequency of CMOS circuits; that means, as I know as I have mention the energy consumption will be more when the clock frequency is smaller.

However, there is this part of the energy consumption is occurring, because of you know leakage power leakage power you know, when the frequency operation is low then leakage power is more because in you know that, in this part during this part lot of leakage power will take place and that is the reason, why this part leakage power dissipation take place then of course, their energy power dissipation will remain more or less constant and then, it will keep on increasing as the frequency is increasing.

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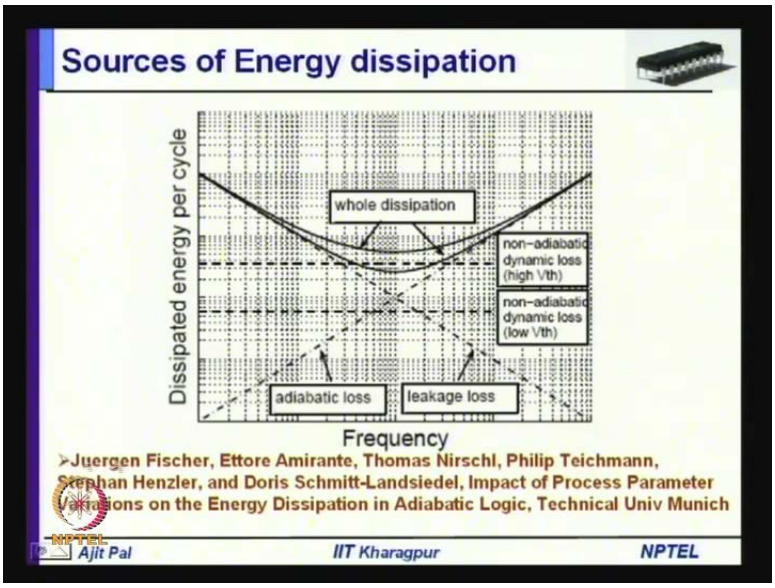

So, here actually this diagram shows, how exactly this occurs for example, adiabatic loss as we know increases as the frequency of operation increases because it is proportional to frequency smaller the operation larger is larger is the saving and leakage loss as we can see smaller the frequency of operation leakage loss is larger.

So, you can see this is the total power dissipation if, you take into account the dynamic and static power. So, there is a group working in this area, from the technical university of munch.

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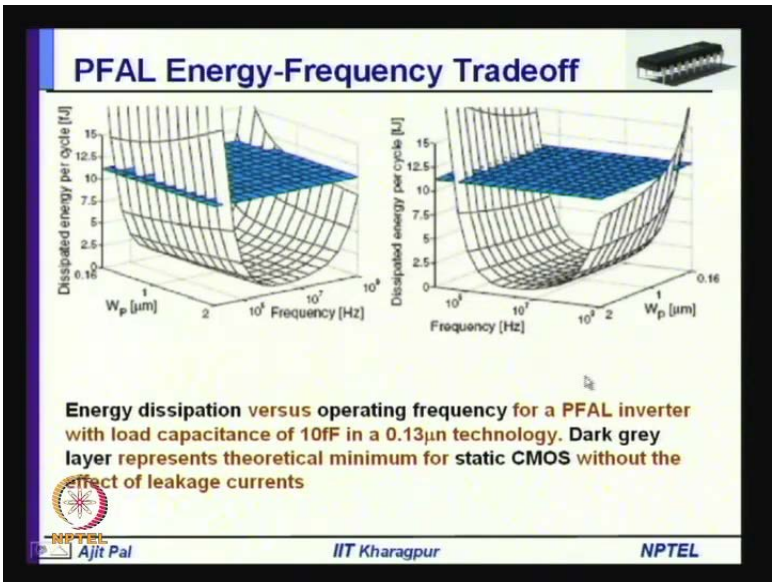

So, they are carrying out lot of research work on adiabatic logic circuits. The impact of that impact of process parameter variation on energy dissipation in adiabatic circuits. So, they have done they are doing always works and here is another simulation result. It shows that, how the tough layer corresponds to the static CMOS and how the how the 4 adiabatic PFAL l circuits, it is a PFAL l inverter with load capacitance of ten piko farad and realized using point 1 3 micron technology. You can see how the energy dissipation occurs and how it varies with frequency and also with the width of the p mos transistor. So, the variation of the width of the p mos transistor and also along for the variation of frequency how it occurs that is being shown in this result.

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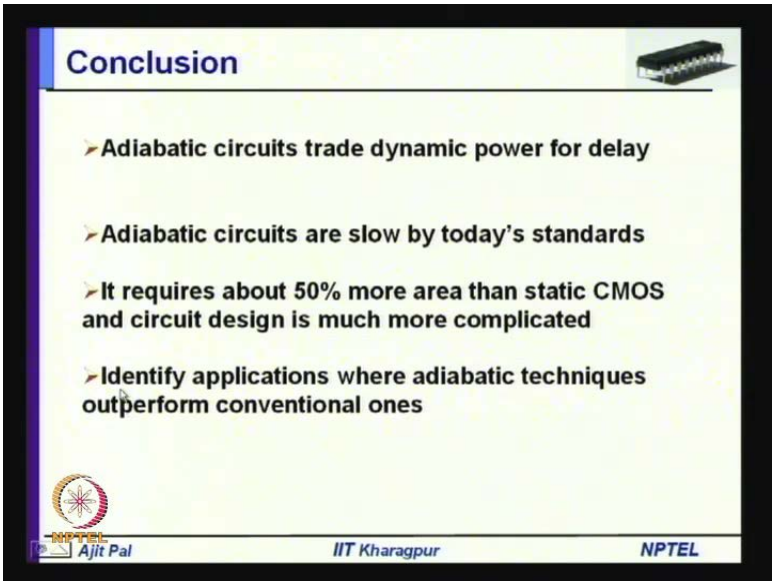

So, we can conclude our lecture with few statements. So, adiabatic circuits trade dynamic power for delay as we have seen and adiabatic circuits are slow by today's standards. As you have seen, they can operate only in the megahertz range not in the gigahertz range. They are much slower into their standards, but there are many applications where, we can use these adiabatic circuits for example, pacemaker which need not really operate at a very high frequency no speed of operation need not be very high, but saving of energy is extremely important, because you cannot replace the battery everyday and battery placement is hazardous.

So, in such cases; obviously, it can be used then it requires 50 percent more area than static CMOS. As we have seen and design is much more complicated, but lot of research

work is going on to get efficient design and particularly whenever, you want to use adiabatic circuits, you have to identify applications, where adiabatic techniques outperform conventional ones. So, in such cases, we can use adiabatic circuits. So, with these concluding remarks, we have come to the end of today's lecture on adiabatic logic circuits. Thank you.