Low Power VLSI Circuits and Systems

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Lecture No. #26

Tutorial-II

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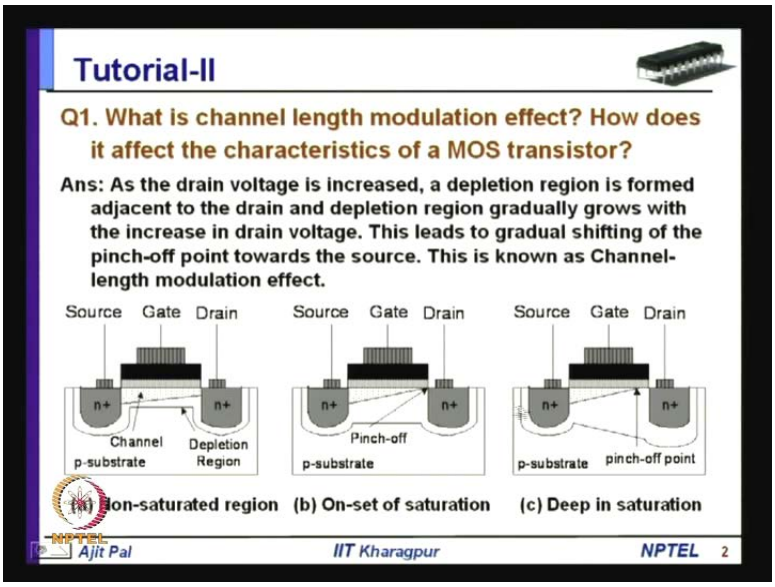

Hello today, we shall have tutorial on the mid semester questions and. So, this is the tutorial 2 we shall discuss the questions of mid sem exam and of course, in addition to that if you have got any other questions we shall discuss. So, first question was what is channel length modulation effect how it affects the characteristics of a mos transistor.

Uh as you know as the drain voltage is increased a depletion region is formed adjacent to the drain and depletion region gradually grows with the increase in drain voltage. So, three different situation are shown the first one is non non-saturated region where you can see width of the channel region is changing starting from source to drain, but it is not yet zero at the drain point on the other hand this is on set of saturation. Where you see the pinch of point has reached pinch of point; that means, the width of the channel region is almost zero near the drain.

But whenever the channel length is small I mean then as you further increase the drain voltage that pinch of point shifts towards the source and whenever the device size is large; that means, two fifty nanometer or three fifty nanometer in such a case of course. This is not this difference of change is not visible; however, in case of short channel devices this small change in channel length becomes visible and it has impact on the on the drain current.

As you know?

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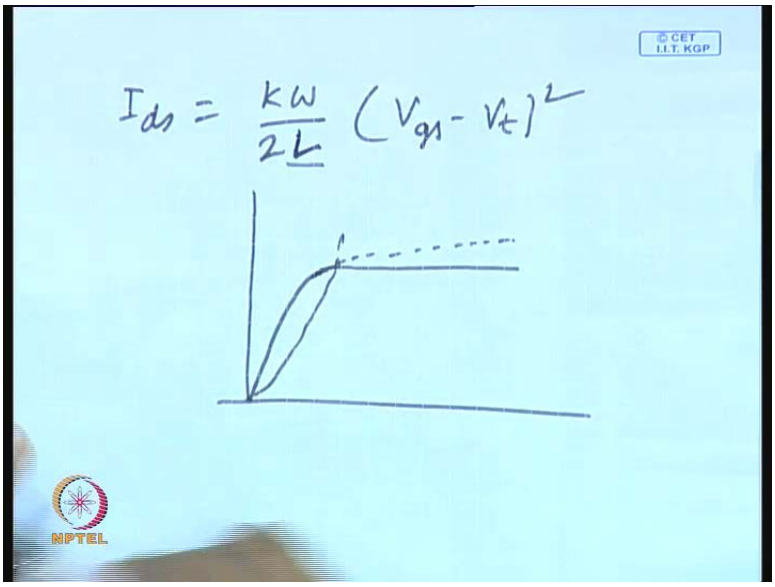

In the saturation region the equation for drain current is I d s is equal to k w by twelve into V g s minus V t whole square. So, in this case you can see there is no equation for drain voltage; however, this length channel length changes and since this reduces the drain current does not remain constant and as a consequence what happens instead of you know ideally the drain current should have been constant after the saturation point is reached, but it does not remain. So, it increases. So, this is the effect of channel length modulation and; that means, the drain current does not remain constant in the saturation region as it is.

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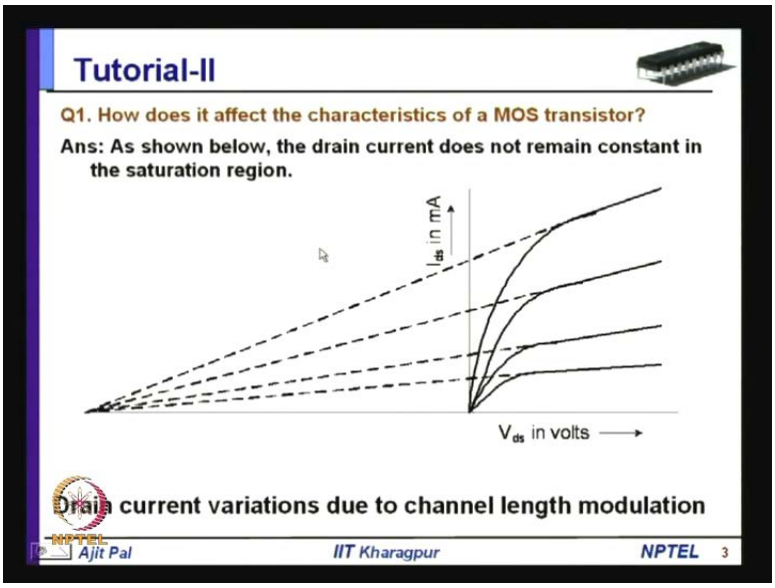

Shown in this diagram the variation of drain of drain current due to channel length modulation now.

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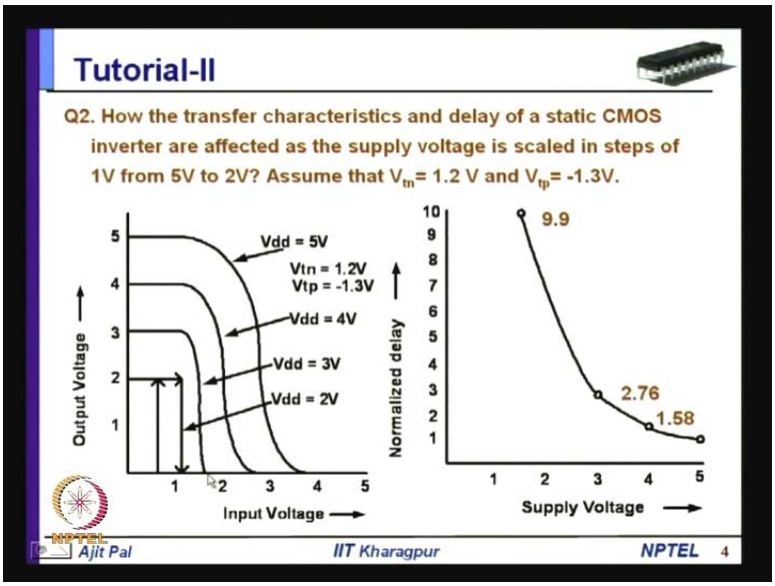

Coming to the second question how they transfer characteristics and delay of a statics c mos inverter are affected as you supply volt is scaled in steps of one volt from 5 volt to 2 volt assuming that V t n is equal to 1.2 volt and V t p is equal to minus 1.3 volt

So, as we know the c mos c mos inverters or c mos gates can work over a over a over a large voltage range; however, it has impact on the transfer characteristics and delay and

which is shown in this in this particular in this particular example. So, here as you can see when the supply voltage is 5 volt, so initially when we get input voltage gate voltage is less than 1.2 volt it remains constant and whenever it is more than 1.2 volt the both the transistor turn on; that means, initially the p mos transistor is on during this period and both of them turns on as the as the and as a consequence the there is flow of drain current the voltage goes down and a point is reached. When the supply voltage is equal to 5 minus 1.3 volt at that point the p mos transistor turns off and as a result the output voltage becomes zero.

So, for this reason starting from 1.2 volt to in this case three point seven volt the there is a variation of the drain current and of course, this current will be depending on the relative resistance of the p mos and n mos transistors.

So, this is how it varies for v d d is equal to 5 volt and for v d d is equal to 4 volt similar situation, but when the input voltage is 0 then of course, output will be 4 volt and it will remain constant up to input voltage of 1.2 volt then again it will start decreasing and when then it will become 0 when the input voltage is 4 volt minus 1.3; that means, 2 point seven. So, at 2 point seven it becomes 0 and in this part it changes from 5 volt to 4 volt to 0 volt

So, this is how the characteristic changes transfer characteristic changes and similarly for three volt as you can see more or less it falls very quickly the reason for that is you know you both the transistor is remaining on up to 1.2 volt and then 2 minus 1.3 is close to one point seven. So, one point seven volt it becomes 0. So, you can see 1.2 to one point seven in this range it changes from three volt to 0 volt on; however, there is special situation when that.

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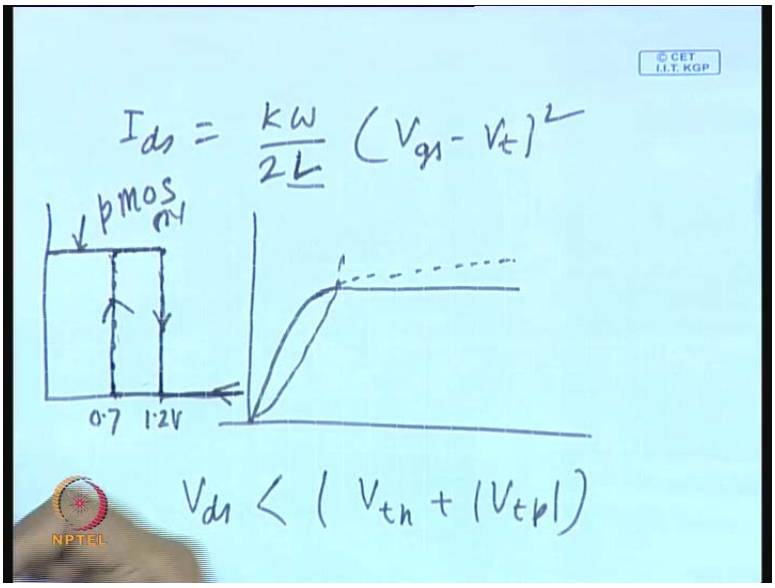

We know that when the when the v d s is less than v t n plus v t p then we get a kind of hysteresis.

So, that is the situation occurs when the drain voltage is 2 volt and 2 volt is definitely less than 1.2 plus 1.3. So, this is 2 point 5. So, what happens in this case as the input voltage increases from 0 volt the p mos the n mos transistors remains on up to 1.2 volt then it it switches to it turns off and during this no sorry I have taught wrongly. So, in this part we know the p mos transistor is on for this part which part 2 minus 1.3; that means, up to point seven volt. So, up to point seven volt p mos transistors is on and during this part none of the transistors are on. So, the characteristic is somewhat similar to this.

Let me draw here. So, up to point seven volt 0 point seven volt the p mos transistor is on p mos on then neither p mos nor n mos are on up to 1.2 volt. So, during this part none of the transistor is on. So, as a consequence delay will increase, because the output is remaining V d d because it has charged to V d d level during this period, but none of the transistors are on then of course,, the n mos transistor turns on when it reaches 1.2 volt and it goes down the output goes down to 0 volt and then it remains 0 for the remaining part of the circuit.

Now, as you reduce the voltage from V d d to toward 0 volt then what happens as you go as you go towards this side the initially the n mos transistor is on, but n mos transistor

turns off as it reaches the 1.2 volt. So, again during this part; that means, input voltage of one point seven to 1.2 none of the transistors are on and p mos transistor turns on here. So, we get a hysteresis like this; that means, as the input changes from 0 to v d it goes this way and if the input changes to 0 it goes this way. So, if you on oscilloscope if you see this that is known as x y plot we will kind this we will see this type of hysteresis.

Now, coming to the variation of delay as you know the delay is dependent on the supply voltage and threshold voltage.

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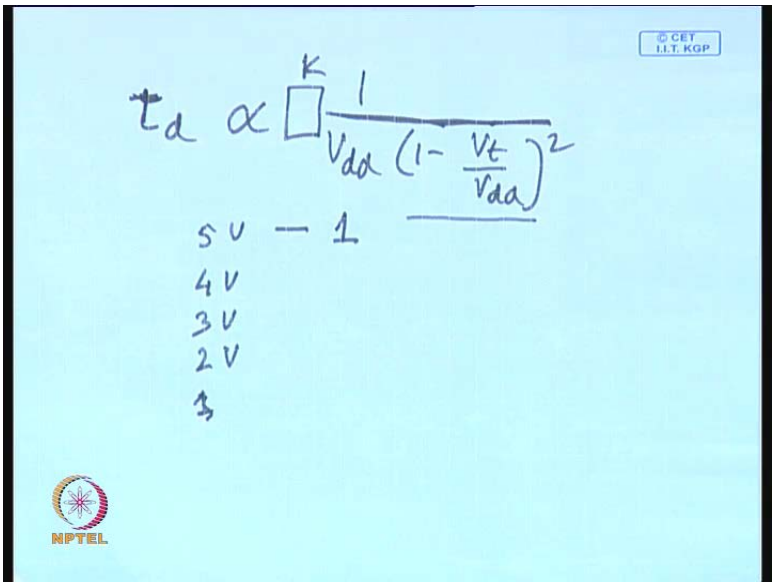

So, the t d you can say t d is proportionate to one by V d d into one minus V t by V d d here i have assumed that both the transistors have the same threshold voltage; however, we have to taken to the consideration 2 different threshold voltages for 2 transistors and equation will be little different if you-if you have accurate value, but this simple equation. You can use to have relative change in the delay for different supply voltage say 5 volt 4 volt three volt 2 volt and one volt 2 volt, so 5 to 2 volt 5 three 4 2.

So, if we consider the delay corresponding to this is one, we can find out what will be the delay based on these because other part is constant. So, here you have got a constant part that part we can consider you know same for all the voltages. So, considering the delay is equal to one for 5 volt we can see here delay is one for 5 volt is equal to one then how the delay is increasing as you go to 4 volt it is one point 5 eight; obviously, it is normalized with respect to the delay of when the V d d is equal to one volt and then you

can see for three volt it is 2 point six 2 point seven six times and when it is 2 volt it is 9.9 times.

As you know when the supply voltage becomes closer to the threshold voltage then delay increases dramatically, because this part will become very small and that is what is happening in this part of the circuit as you can see here the supply voltage is 2 volt and threshold voltage is 1.2 still it is point eight volt different and if the supply voltage is further reduced it will increase very sharply. So, delay will increase very sharply. So, this is how the delay changes for different supply voltages. So, that was question number 2 coming to question number three.

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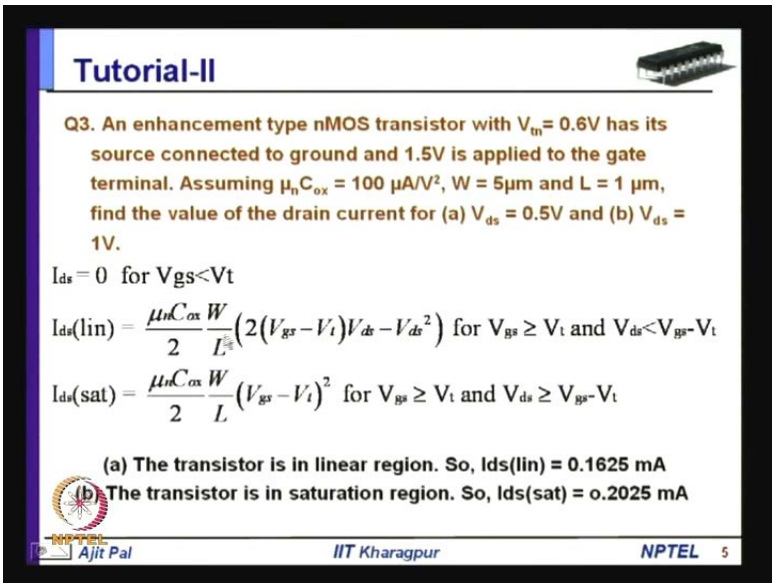

An enhancement type n mos transistor with v t n is equal to point six volt has its source connected to ground and one point 5 volt is applied to the gate assuming that mu n c o x is equal to hundred micro ampere per volt square w is equal to 5 micron and n is equal to one micron find the value of drain current for v d s is equal to point 5 volt and v d s is equal to one volt.

So, when the v d s is equal to point 5 volt; obviously, the transistor is in saturation on the other hand when v d s is equal to one volt it is just in sorry when v d s is equal to point 5 volt the transistor is linear region and when v d s is equal to one volt then the transistor will be in saturation as it is evident from this relationship. So, I mean v d s is equal to less than v g s minus v t one point 5 minus 1.2 one one one point 5 minus point six.

So, as a consequence we find that in these 2 cases the operation of transistors will be different; that means, the current will characteristics will be different as you know the current in the linear region-region is mu n c o x by 2 w by l into 2 v g s minus v t into v d s minus v d s square

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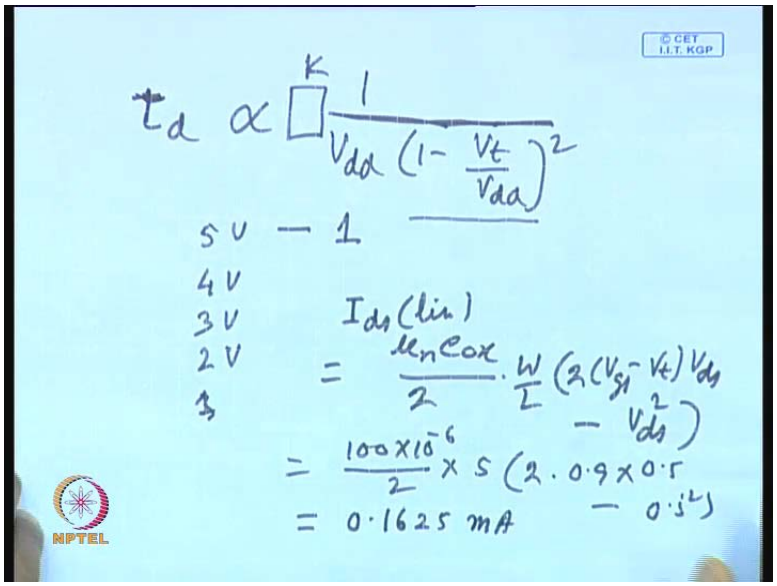

So, if we substitute it here; that means, first equation that is your I d s linear that is equal to mu n c o x by 2 into w by l into 2 into v g s minus v t into v d s minus v d s square. So, we can substitute different values mu n c o x value is given that is equal to one hundred into ten to the power minus six by 2 into w by l is equal to 5 and it is 2 v g s minus v t v g s is equal to one point 5 and v t is equal to v t is equal to as you can see v g s is equal to one point 5 and threshold voltage is given point six. So, one point 5 minus point six it is point nine 2 into 0 point nine into 0 point 5 minus 0 point 5 square.

So, if you solve this equation we will get 0 point one six 2 5 mille ampere. So, in a similar way you can find out the current in the saturation region.

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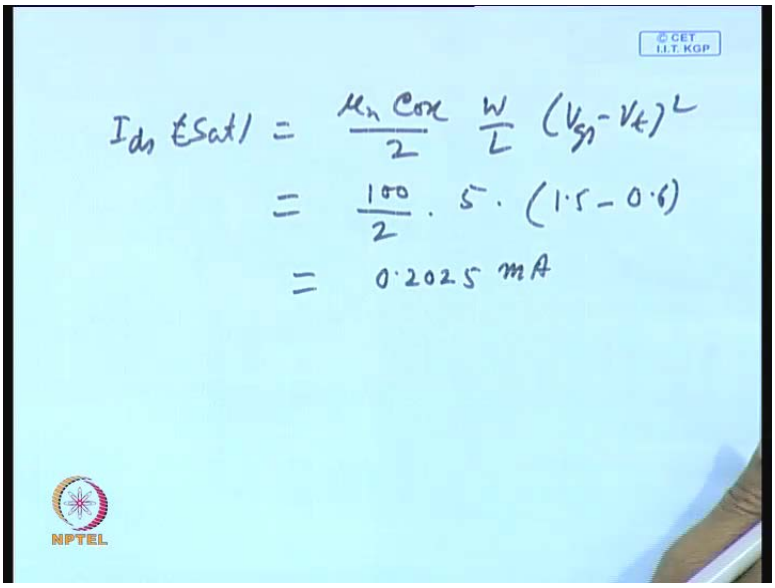

So, in that case i d s is equal to I d s sat saturation is equal to mu n c o x by 2 w by l and then v g s minus V t whole square. So, in this case it is hundred by 2 into 5 into v g s minus v t v g s is equal to v g s is equal to one point 5 minus 0 point six. So, that will give you 0 point 2 0 2 5 mille ampere.

So, this is these are the 2 drain currents in 2 different regions linear region and saturation region; that means, in the first case for a the transistor is in linear region. So, I d s is equal to 0 point one six 2 5 and in the second case the transistor is in saturation region. So, i d s that is equal to 0 point 2 0 2 5. So, this can be easily obtained as a sum.

Now, coming to the third question a static c mos.

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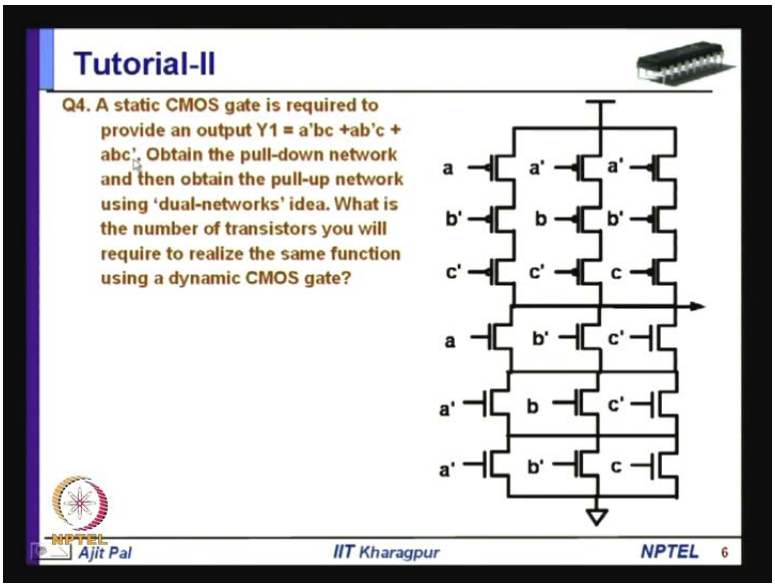

4th question static c mos gate is required to provide an output y one is equal to a bar b c plus a b bar c plus a b c bar. So, as we know.

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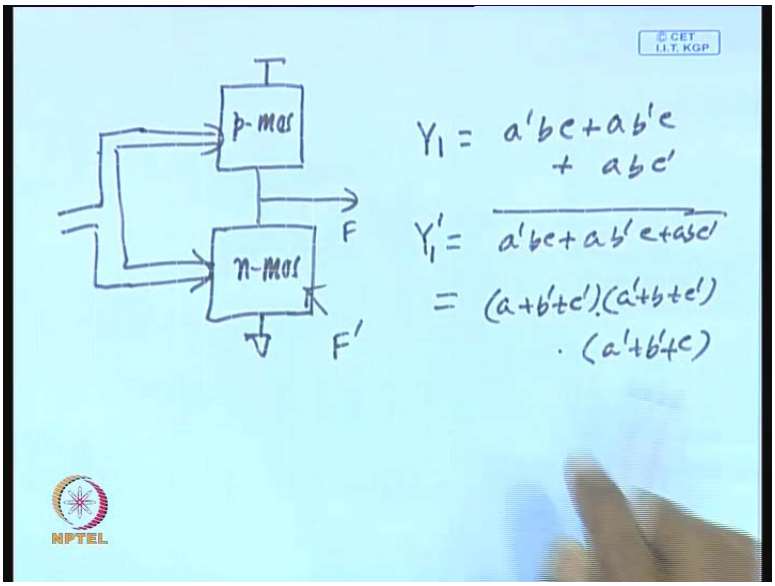

Whenever you are realizing a c mos circuit c mos gate you have got p mos network as pull-up device and you have got n mos n mos network as pull-down device and inputs are applied to both same inputs are applied same inputs are applied and you take the output from here and the n mos network is connected to ground cause it acts as a pull-down network this how realize the function.

As you know this n mos network corresponds to a bar. So, in this particular case y one y one function you have to realize and that y one is given as a bar b c plus a b bar c plus a b c bar now to find out the n mos network you have to complement it. So, you have to get y one bar and that is equal to a bar b c plus a b bar c plus a b c bar. So, this is equal to a plus b bar plus c bar into a bar plus b plus c bar into a bar plus b bar into c as you know this we get following the simple rule of Boolean algebra or de-Morgan's equation.

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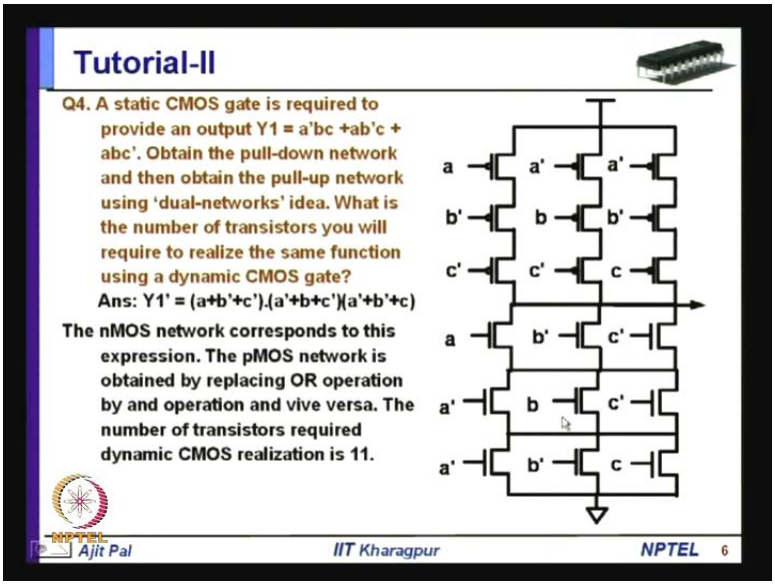

Now, this network will correspond to this n mos network. So, which is shown here you can see the n mos network corresponds to a b bar c bar which are in parallel a or b bar or c bar and a bar or b or c bar and a a bar b bar and c. So, this is the n mos network and dual of that this can be easily obtained as you know the p mos network is the dual of the dual of this n mos network. So, wherever it is parallel it will be in series. So, a b a b bar c c bar which are in parallel it will be in series a b bar c bar and it will be p mos network.

Similarly, a bar b c bar we get a bar b c bar which is also which will be also in series and in parallel with this here it was in series with this here it will be parallel with this similarly a bar b bar c that will be in series that will be parallel with the other 2. So, this is how you get the n mosp mos network from the n mos network the dual of this function

Now, whenever you go for realizing dynamic c mos then the network will be somewhat similar to this. So, you will have a p mos transistor

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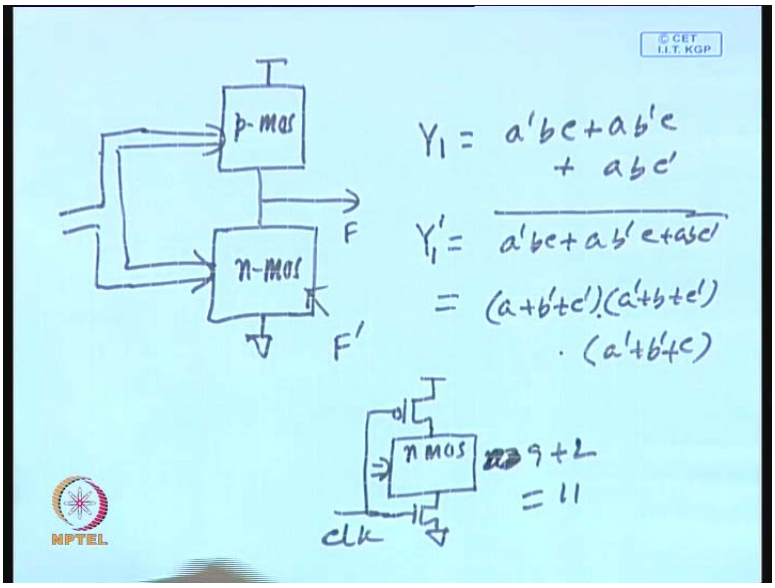

Then n mos network and there will be another n mos network will be, which will be connected to ground and here will be your primary inputs and you will apply clock here. So, the n mos network if the number of transistors in the n mos network is nine in this particular case n is equal to nine sorry number is nine. So, the total number of transistors will be nine plus 2 that is eleven. So, eleven is the number of transistor that you require to realize dynamic c mos and if you use p mos network even then you will have eleven numbers of transistors. So, this is the question number 4.

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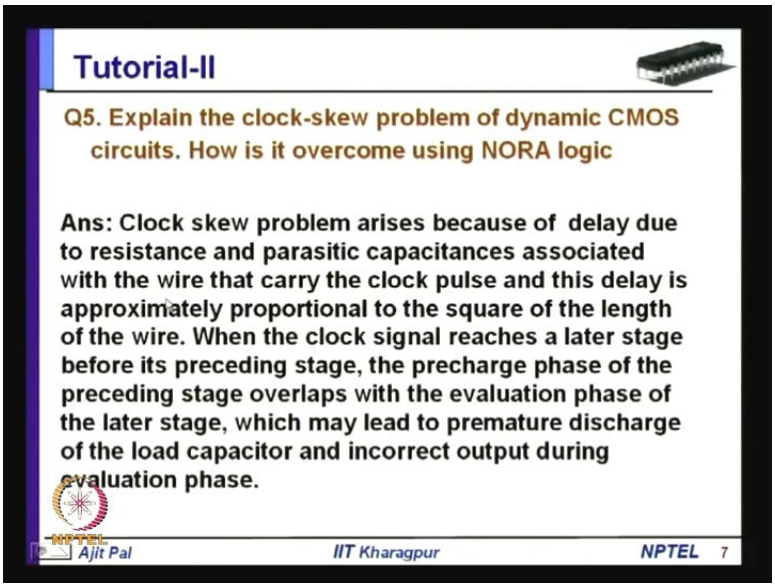

Coming to question number 5 explain the clock-skew problem of dynamic c mos circuit how is it overcome using nora logic as you know clock skew problem arises, because of delay due to the resistance in parasitic capacitance associated with the wire that carry the clock pulse and this delay is approximately proportional to the square of the length of the wire.

When the clock signal reaches a later stage before, it before its preceding stage the pre-charge phase of the preceding stage overlaps will be evaluation phase of the later stage which may lead to premature discharge of the load capacitor and incorrect output evaluation phase.

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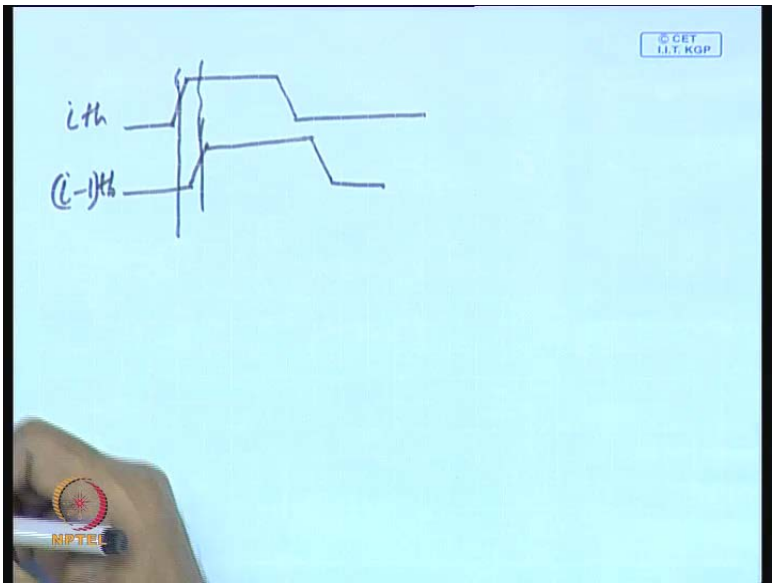

We have already seen discussed about it; that means, suppose this is the clock of one particular stage and this is the clock which has reached a I mean this is the clock of the preceding and succeeding stage and this is the clock of the succeeding stage; that means, this clock has reached the I x stage earlier than i minus one x stage.

So, as a consequence when the circuit is in the pre-charge phase here it will be in the evaluation phase. So, that will lead to I mean when it is in the pre-charge phase during this period it is it is in the evaluation phase of the I x stage and that may lead to as you know premature discharge of the output and as a consequence what will happen it may lead to incorrect output.

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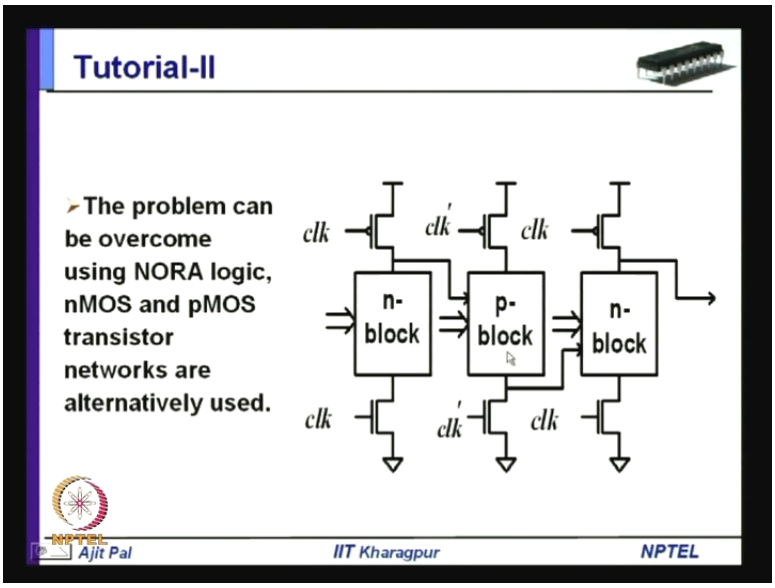

So, this problem as you know can be solved by using Nora logi,c where you are feeding the output of a of a dynamic circuit realized by n mos transistors, so n-block so output is going to a p-block.

As you can see this output will be one during pre-charge and this will not make any impact on the p-block because p mos transistors will turn on when output is zero since the output is one. It will not lead to any premature discharge and circuit will function without any problem and. So, alternately you will be using n-block p-block n-block and. So, on mos and p mos transistor network are alternatively used and this will lead to this will overcome clock skew problem.

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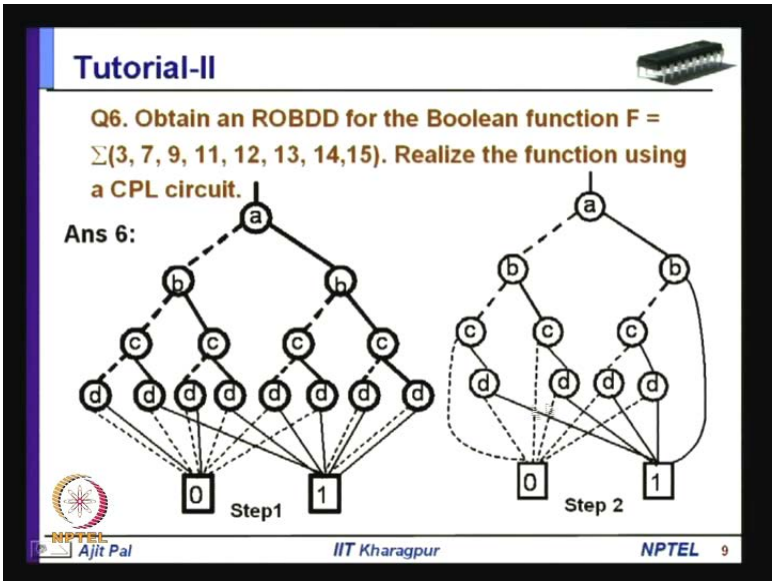

Now, coming the question of the this question coming to question six obtain an r o b d d for the Boolean function f is equal to three seven nine eleven twelve thirteen fourteen fifteen these are the mean terms of a Boolean function.

Now, you have to realize the function using a c p l circuit. So, from this function mean terms you can straight away get a V d d, but; obviously, it is not minimized you can see a V d d will have only single terminal 2 terminal notes one for 0 and one for one and. So, and from this side it is a bar b bar dotted lines corresponds to 0 and solid lines correspond to one. So, you can see this is a bar b bar c bar d bar. So, for a bar b bar c bar d bar means 0 0 is going to 0 similarly a bar b bar c bar d which is one also going to 0 because is 0 and one both of them are falls in this particular case.

So, in this way you can map the entire all the edges to either to 0 or to one; that means, 0 one 2 then three is true. So, it will map to one then 4 5 is also false. So, they will go to 0 then six seven eight these are all false. So, they are coming to 0 and then nine is will go to one this is nine a bar b sorry this is your six this is i believe this is seven. So, this is a bar b c d. So, a bar b c d that is seven that will go to one and then eight will be go to 0 will go will go to 0 and this is nine ten eleven again is going to one twelve thirteen twelve thirteen 4teen all will go to one.

So, in this way you can map all these line in this manner and then you can do minimization. So, wherever both 0 line and one line is going to 0 or it is going to one they can be they are redundant. So, these redundant nodes can be removed this node will

be removed this node sorry this node will be removed this node will be removed. So, we will be left with this node this node this node and this node and this node 4 nodes one 2 three and 4 remaining 4 nodes are redundant and directly c will come to 0.

Similarly, this c dot will also come to 0 and like that. So, that is that is what you get in the step 2 directly c dot is c dot i mean dash dash dash line dotted line from c will come to 0 then similarly this dotted line from c will come to 0 then this and and this similarly this too and this will also disappear. So, this dotted line a b c. So, one 2 three 4 actually this entire part has been removed because you can see this will merge and this c will also be redundant. So, this b solid line has come to one as it is shown here

So, in this way in the first step this much of minimization is possible now we find that for all the d's dotted line are going to 0 and solid line are going to one. So, all the d's can be merged together to form a single d as.

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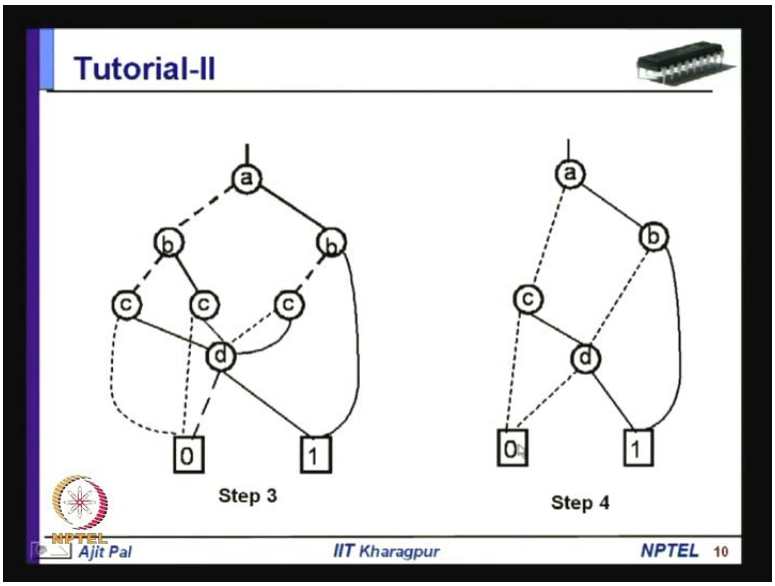

It is shown in this particular diagram. So, all the d's have been merged and as you do the merging of all the d's we find that this c becomes redundant because dotted lines and solid lines are all terminating at b. So, this dotted line from b will come to d and d's to c's can be merged together because dotted line going to 0 and solid is going to d. So, by removing by combining these 2 c's and removing this c we get this final r o b d d because there is we cannot really i mean minimize it any further neither in an edge nor in node can be removed from this. So, this is the final r o b d d we get after all this simplification

So, from this particular from this particular r o b d d.

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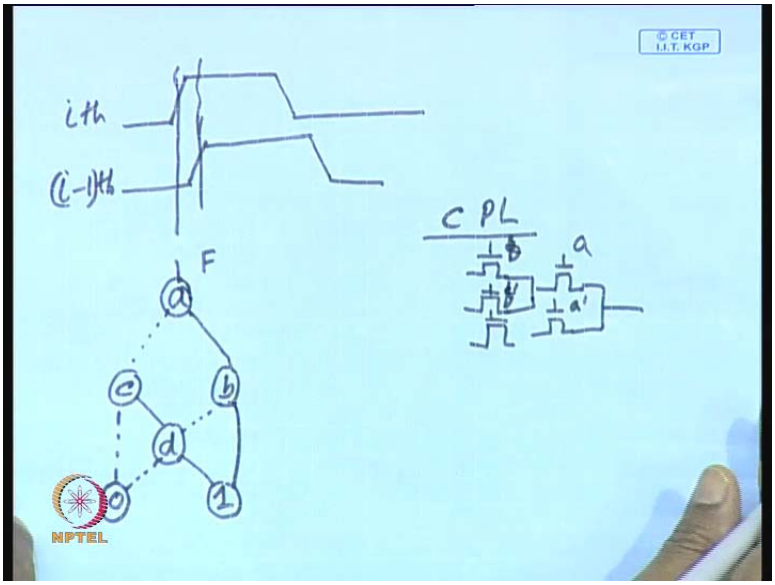

Which we have got let say a then dotted line is coming to c solid line is going to b and you have got a d and solid line from c is coming here dotted line from b is coming here and then you have got 0 dotted line from c will go to 0 dotted line from d is also going to 0 and then you have got one and the solid line from b will come to one and solid line from d will come to one this is the r o b d d that we get now from this you can very easily realize the past (()) network.

So, past (()) network can be realized and which can be used to have the c p l realization c p l realization you can easily do for let us consider the realization of this ape bar first. So, here it will you will be having a a bar and a a bar and if we if we are considering this side let us consider this side. So, it will go to c and this will this will go to c bar this is c bar and here we will be having a bar sorry this will be no solid is going to b. So, this will be b this will be b bar.

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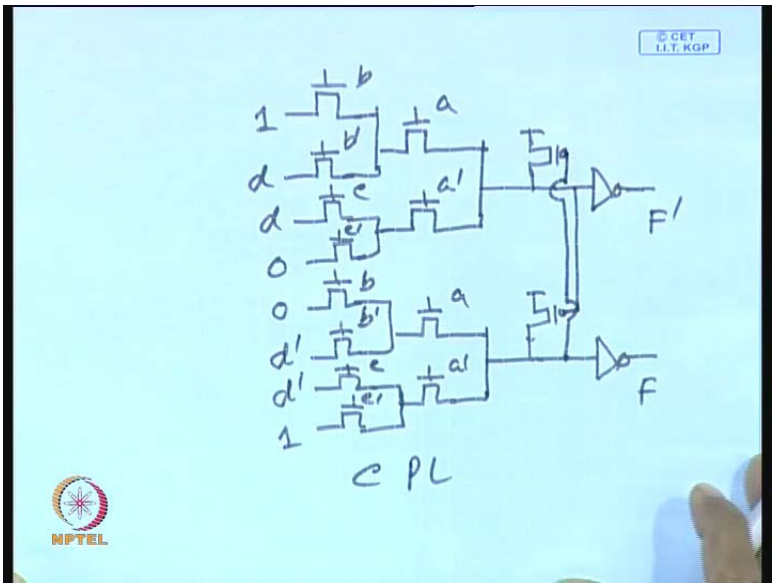

Let me redraw it separately. So, let us start with a a bar a and a bar and this side will go to b b bar and this side will go to c and this side will go to c bar.

So, in this case a b this will be this is going to one and as we have seen in this particular case a b will be a b going to one and then this will go to d this will go to b and this will go to 0 and then your c p l circuit will be having an inverter and a and a p mos transistor as pull-up device. So, this will be connected here this will be connected to v d d and this thing will go to the other side. So, I have to replicate this part and we shall be having same thing a a bar and b b bar and c c bar and again you will be having an inverter and another p mos another p mos transistor will be here and this gate will be connected to this and the gate of this will be connected to other side.

So, this is how a c p l realizes since here you are getting ape you will get ape bar here and here you will get ape. Now what will be the inputs here since it is the realizing complementary function only thing you have to do you have to apply complimentary inputs? So, here it will be 0 d bar d bar and one. So, this is how you can realize the c p l circuit starting with this r o b d d. So, this is this is this is the r o b d d this is the r o b d d and corresponding c p l circuit it is shown here. So, this is how you can realize the circuit. So, this is the c p l realization this is what i have already discussed uh.

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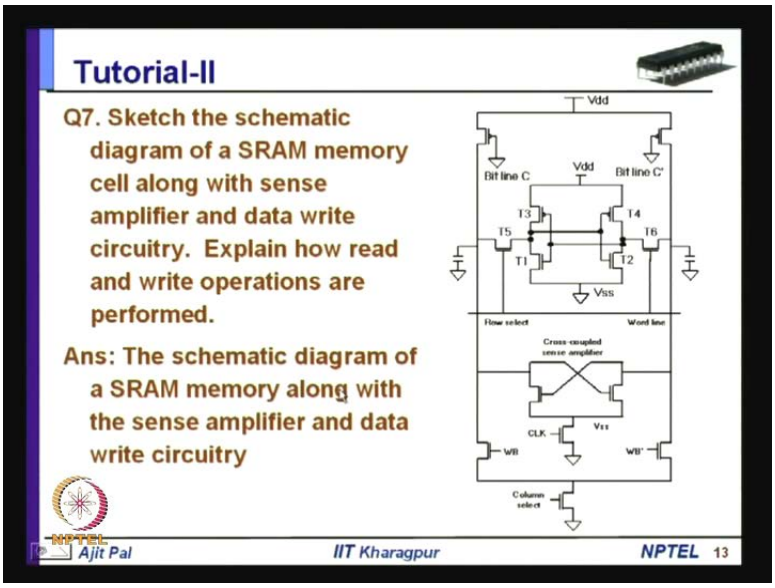

Now, coming to question number seven sketch the schematic diagram of the s ram memory cell along with sense amplifier and data write circuitry and explain how read and write operations are performed. So, this is the schematic diagram of a s ram memory cell. So, you have to explain the read and write circuits and you can see you have got a memory cell then you have got row select line and word select line row or word select line and column select line is here.

So, for write operation once the column select and row select lines are performed through the i o part of the circuit corresponding bit values will be available there and once the word line is activated by the row select signal the those zeros and ones I mean whatever is the coming from the I o lines will reach these points these points and whichever is the zero that will activate this p mos transistors.

Suppose, your this is the bit line c bar I mean if this is one; that means, then zero has to be written if zero has to be written then zero will pass on to pass to this line and that will make this transistor on and as this transistor turn on this will make this line one and this will make this transistor turn on and this will become one i mean this will become zero and this will become one because this is turning on and this is turning on; that means, t three t three is on and t two is on that will make this one and this one zero. So, this is how writing will take place and after you have withdrawn these row select and select

column select signal this is the value will be written within this s ram cell as long as power v d d is there.

Now, reading operation is little complicated because you have to use the sense amplifier. So, reading operation can be done in three steps.

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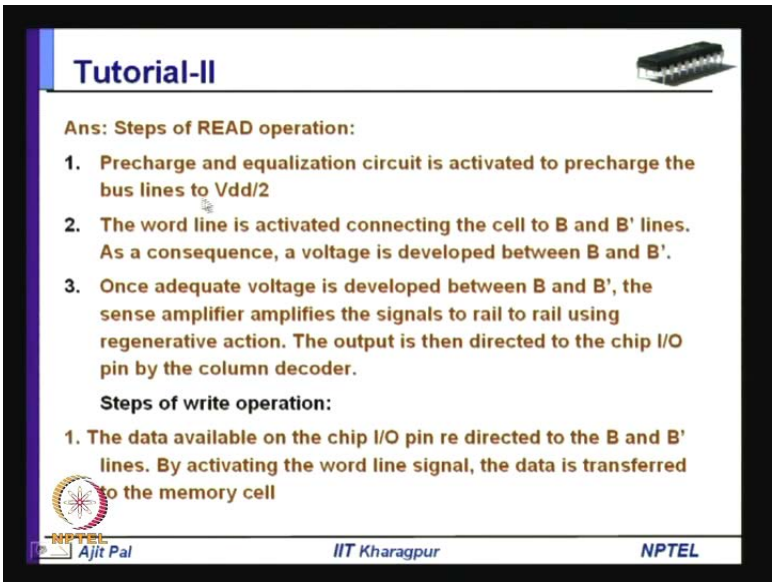

First you have to do pre-charge and equalization circuit is activated to pre-charge the bus lines to v d d by 2. So, there is a pre-charge and evaluation circuits which will be activated to make the bus lines zero.

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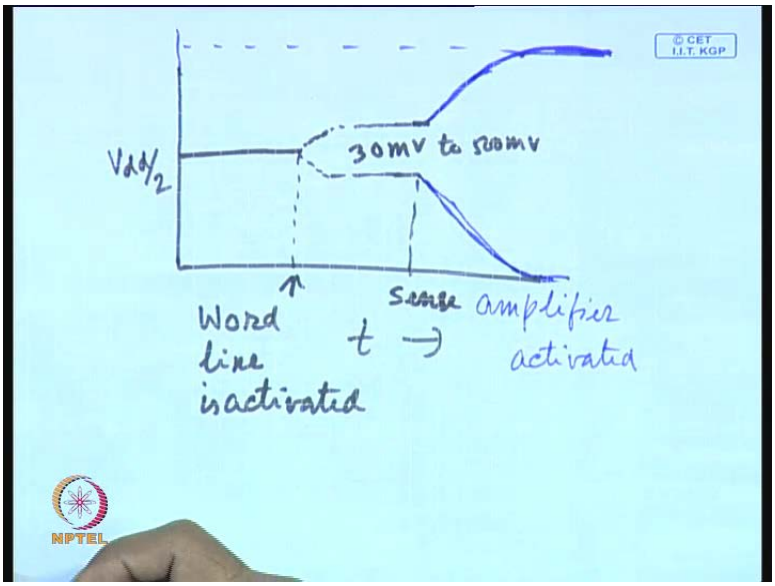

We can draw the circuit. So, initially there will be pre-charge both the lines will be pre-charged to v d d by 2 both the bit lines.

That means that bit line bit line and bit line bar now at this point the word line is activated connecting the cells b and b bar lines connecting the cells to b and b bar lines as a consequence a voltage is developed between b and b bar; that means, at this point you are activating the word line. So, this is time. So, at this point word line is activated.

So, as the word line is activated 2 2 outputs will be will have some difference that difference can range from say thirty mille volt to 5 hundred mille volt not much. So, that much difference will be created between these 2 buses; that means, if you go back to the original diagram. So, a voltage difference will be created between these 2 lines; that mean, bit lines c and c bar. So, depending on what you are writing one will become lower than V d d by 2 another will become higher than V d d by 2.

So, you will be having a difference of fifty mille volt to 5 hundred mille volt between these lines and that will that will be applied to this cross coupled sense amplifier. So, sense amplifier will be activated now there is a clock and as this sense amplifier is activated here this is this is where sense amplifier sense amplifier activated at this point.

So, here exponentially these 2 will go in 2 different directions and very soon it will become zero and this will become v d d and here there is a there is a positive feedback and that is why very quickly this happens the sense amplifier amplifies the signal and we get a real to real output on c n c u l lines. So, this is how in three steps this is happening the read operation is happening; that means, after this is done we will get here difference between these 2 lines will be v d d; that means, one of them will be zero and one of them will be one depending on what value was stored in this.

If zero was stored here; that means, this will be if zero was stored then you know this bit line c bar will become one and this will become zero and if one was stored this will this will become v d d and this line will become zero this is what what will happen after three steps and i have already explained the right operation how it occurs.

So, this is how the read and write operation occurs in a static c mos circuit.

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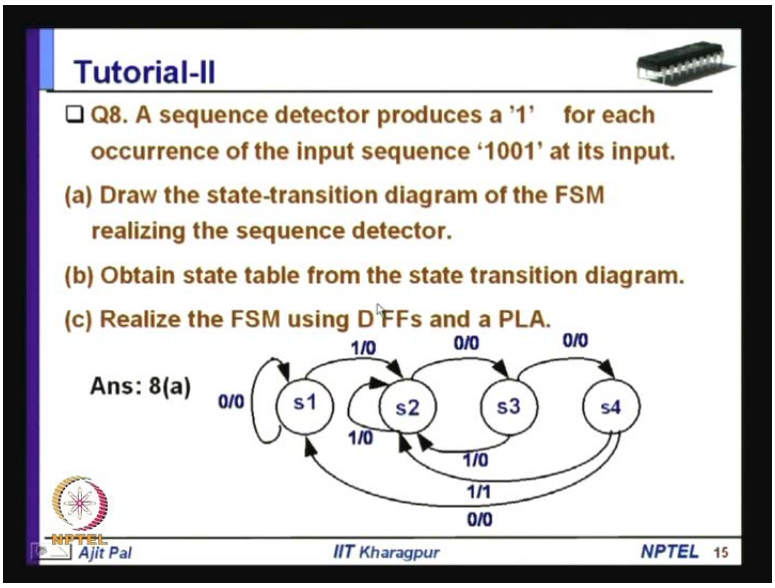

Coming to question number eight a sequence detector produces a one for each occurrence of the input sequence one zero zero one at its input draw the state transition diagram of the f s m realizing the sequence detector and obtain second part is obtained from the state transition diagram and third is realize the f s m using the d flip flop and p l a.

So, here your question is.

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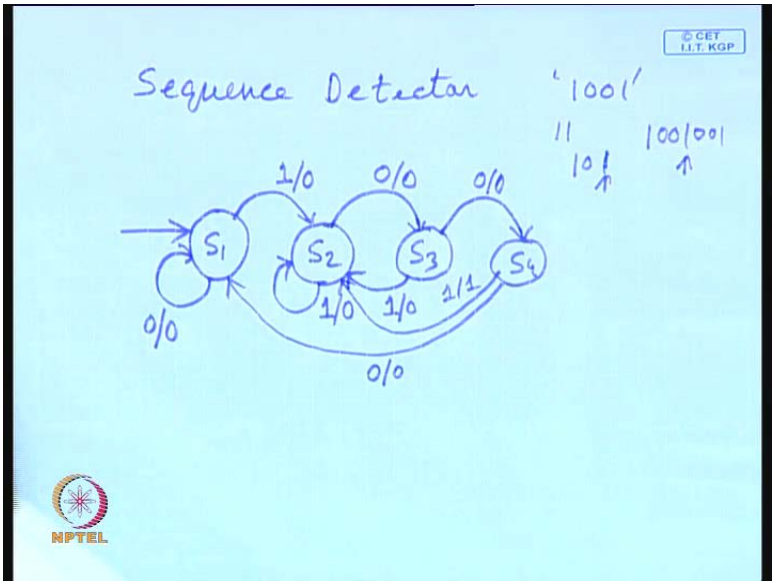

Sequence detector and that has to detect the sequence one zero zero one; that means, for each occurrence of one zero. One it will produce one now how do you dram the state transition diagram we have to consider an initial state let us assume this is the initial state s one initial state.

Now, either a zero can appear as at the input line or one can appear if zero keeps on zero appears then it has to remain in this because there should not be any change because no change is required for starting with zero. So, zero input will produce zero output now if a one appears as input then it has to switch to another state s two because it has to detect the sequence. So, a change is required and it will go to state two whenever a one occurs of course,, zero would be outputted at this point.

Now, again you have the two inputs that can come whenever the machine is in state s two. So, if a zero comes what will happen after this because it is it is it is in the proper directions. So, if a zero comes then it will go to another state that is your s three; that means, zero by zero now if whenever it is in this state and if another one comes then what will happen; that means, if the input is one one then it may be the beginning of another sequence. So, in such a case it has to remain in this state. So, here it will circulate as long as ones continues to come,, but it will keep on producing zero; that means, output will be zero, but as zero keeps on coming it will remain in the state s two.

Now, the machine is in when machine is in state s three two things can happen as zero can come or one can come. So, one zero and zero when a zero comes when a zero comes it will go to another state s four now if a one comes what will happen that one; that means, what will happen one zero one; that means, one zero one if it comes then; obviously, it is not going to produce one. So, it may; however, this can be this one can be considered as as the first one for another for a valid sequence. So, it will go to s three whenever a one comes producing zero.

Now, when the machine is in state four now this is now in one zero this is zero by zero one zero zero and zero has come and now what can happen; that means, one it is gone there and zero it has come here now there is a possibility that either a zero or one will come let us assume what happens when zero comes if a zero comes it has to go back to this point; that means, if a zero comes than it will go here; that means, zero by zero.

Now, what will happen if a one comes where it should go you see one zero zero one now you cannot rule out the possibility of this sequence; that means, this can be the end of one one zero zero one, but the beginning of another one zero zero one that is the reason why you have to go to this state. So, it will be one by one. So, this is the state transition diagram for the sequence detector one zeros zero one; that means it will have four states and the way this sequence will take place is shown here and as I have drawn in this diagram.

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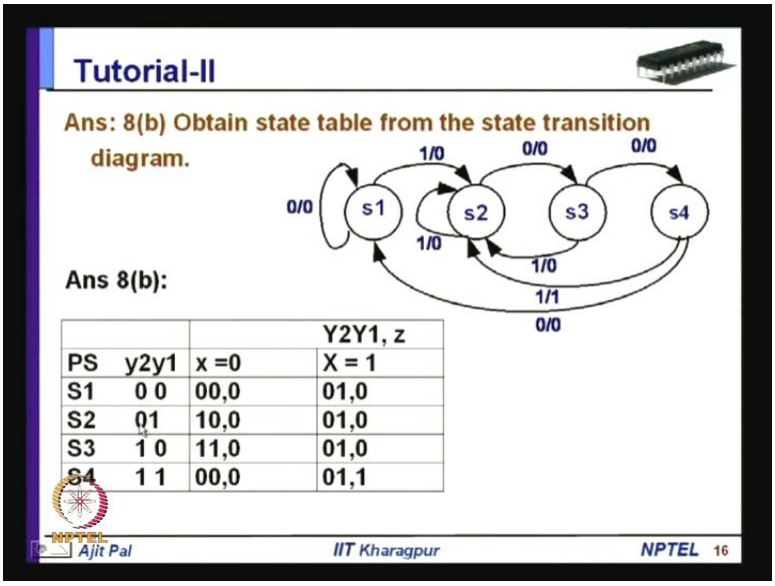

Now, you can very easily obtain the obtain the state table from the state transition diagram. So, you have got four states s one s two s three and s four. So, zero zero zero one one zero one one. That is the coding you have done the state assignment this step is known as state assignment it is not necessary that you have to use this code you could have used a zero zero zero one one one one zero you could have given that also.

So, here there is no hard and fast rule. In fact, this state assignment plays a important role in deciding the area delay and power dissipation of the combination on circuit. So, in this case we have done it in a arbitrary manner without considering whether the circuit will be complex or it will should have minimum delay no consideration has been done.

So, with this simple state assignment you can get the corresponding outputs; that means, y two y one next state values and output the output z which are for different inputs x is equal to zero and x is equal to one these are listed here; that means, when s is s one is

machine is in state s one it will remain in state s one when input is zero as it is shown here zero zero it is going to zero zero; however, if a one comes it has to go to state s two and. So, it is going to zero one.

So, in this way you can when the machine is in state s two if a one comes it is going to next state that is state s three and when zero when sorry a one comes it remains there zero one and when zero comes it has to go to state s three as it is shown here and when it is in s three it goes to s two if a one comes s two and when zero comes it goes to s four. So, one one is thus forms a state s four similarly when the machine is in state s four it can go to state s one when a zero comes and when a one comes it will give you it will go to state s two that is zero one is the code for that and; however, here it will produce one.

So, from these you can easily write down the equations for y two y one and z. So, y two z is true only here. So, z will be equal to y two y one x x is equal to one y two is equal to one and y one is equal to one and you can see y one is this is y two this is y one. So, y one will be equal to in this case it is x; that means, when x is equal to one i mean for all for all the state combinations. It will go to y one. So, y one is equal to x plus corresponding to this that is your y two y one bar x plus y two y one bar will be expression for y one and expression for y two will be corresponding to these two; that means, y two bar y one x bar plus y two y one bar x bar and which has been written here.

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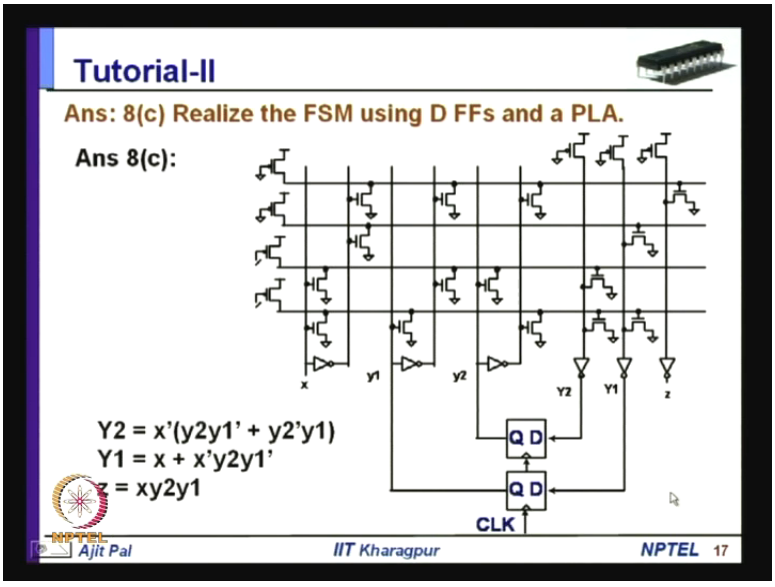

So, this is z x y two y one y one is equal to x plus x x bar y two y one bar and y two is equal to x bar y two y one bar plus y two bar y one as i have shown from this table.

So, from this table straight away you will get this and then you can realize the p l a corresponding to this particular expression as i have told it will have for how many product terms we will have one product term x bar y two y one bar another product term x one bar y two bar y one two product term third product term is x this product term is common here already x x bar y two y one bar it is already there. So, one two three and then 4 x two x y two and y one bar, so there will be 4 product terms and for these 4 product terms you will have a you will have 4 lines you know these lines corresponds to each product term.

So, you have got one two three and 4 for 4 product terms you have got 4 lines in the p l a these are the row lines and then it is non nor p l a here you have applied 4 inputs x y one y sorry three inputs x y two and y one x y two and y one which are complimented outputs are also there and this particular row corresponds to the product term x bar y y two y one and y y one bar and y two.

So, this this is row corresponds to that and this row corresponds to the other product term x bar y two y one bar this row corresponds to x this row corresponds to x y two y one. So, this is how you can realize y two y one and z and y two and y one these are the next state functions you have to feed it feed them to the d flip flops and then feed back to the to i mean that you generate y two and y one after a bit delay this is how you can realize the the complete sequential circuit using p l a. So, p l a is realizing the combinational part of the circuit and these two are the d flip flops that is required to store the states of the machine; that means, those zero zero zero one zero to zero one one zero one one will be stored here and that will be give the state.

So, with this we have discussed all the question that was said in the mid semester exam now if you have any other question you can pass on the papers write it on a piece of paper and pass pass on to me write write your questions on piece of paper pass it on pass it on to me. So, Five minutes left i can discuss one or two questions if you have any otherwise you can end this session thank you we are ending this tutorial two session thank you very much.