Low Power VLSI Circuits and Systems

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Lecture No. # 24

Supply Voltage Scaling – III

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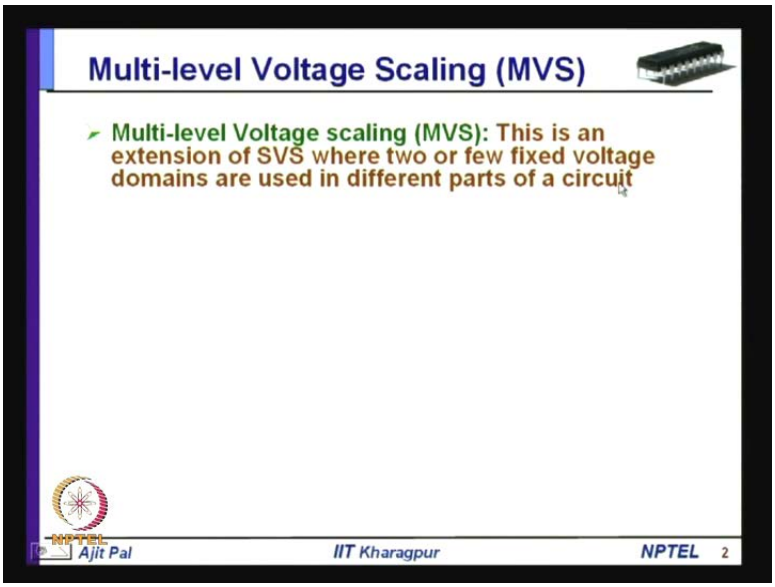

Welcome to today's lecture on supply voltage scaling. In the last two lectures, we have discussed how static voltage scaling is done, and a voltage level, a lower voltage level is assign to the entire circuit. And we have discussed various techniques, approaches used for this purpose. Today, we shall focus on multi-level voltage scaling, and here is the agenda of today's lecture. As I mentioned, multi-level voltage scaling is as is an extension of static voltage scaling, where two or few fixed voltage domains are used in different parts of a circuit.

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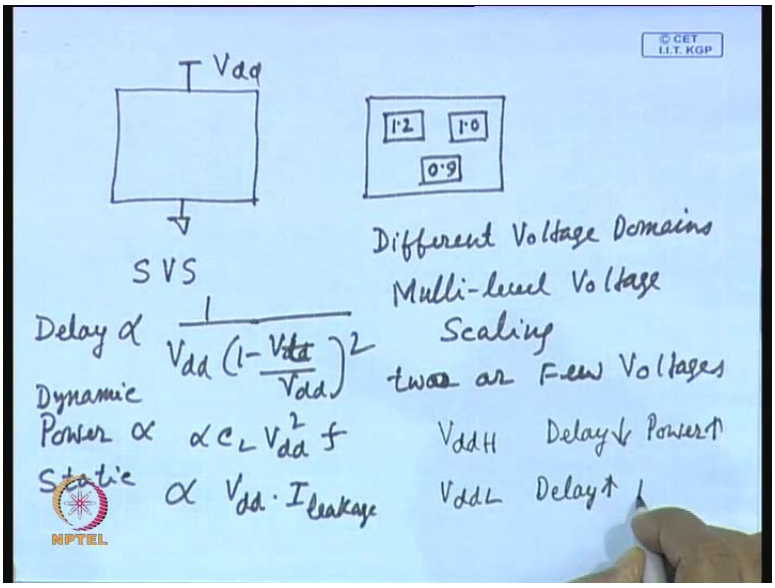

That means, earlier what we did if you have got a circuit entire circuit is having a particular voltage V dd, and that is being scaled that is your static voltage scaling using single voltage. Now, we are considering a situation where inside a single chip may be s o c or may be a single circuit, and different parts of the circuit can be assigned even voltages, we can create different voltage domains like this. And may be this circuit will operate at say 1.2 volt; this can operate at 1.0 volt; this can operate at 0.9 volt like that; that means with within a single circuit you have got different voltage domains.

And how these domains are created? We shall see; and this is called multi-level voltage scaling. And here, we are using two or few voltages few voltages not many, may be 2 or 3 or 4 different voltages are used. And now, what is the basic concept? As we know high V dd gates have less delay, but higher dynamic and static power, and low V dd gates have larger delay but lesser power dissipation, it is already known to us. Why? As you know, the delay is proportional to 1 by V dd and 1 minus V dd sorry v t by V dd square. So, as voltage increases delay decreases and at voltage is reduced, delay increases.

And then, as you know power particularly the dynamic power or switching power is proportional to alpha c l V dd square and f, so as the voltage increase the dynamic power dissipation increases. Not only dynamic power but static power as well as you know static power dissipation is proportional to V dd into I leakage. And both voltage I mean the leakage current can also be dependent on voltage, and as a consequence the power

dissipation increases as voltage increases, and delay of course, reduces in this case as voltage is increased. So we can say that if we use high V dd say V dd high, then delay is less V dd high delay is less and power is more. On the other hand, if we use say lower voltage say V dd Low so lower supply voltage, then delay is more, but power is less. So, we can use two or more voltage levels, and we can judiciously combine them such that there is overall reduction in the power dissipation. However, we shall try to maintain the same performance level, as it is the main goal or main challenge of supply voltage scaling techniques.

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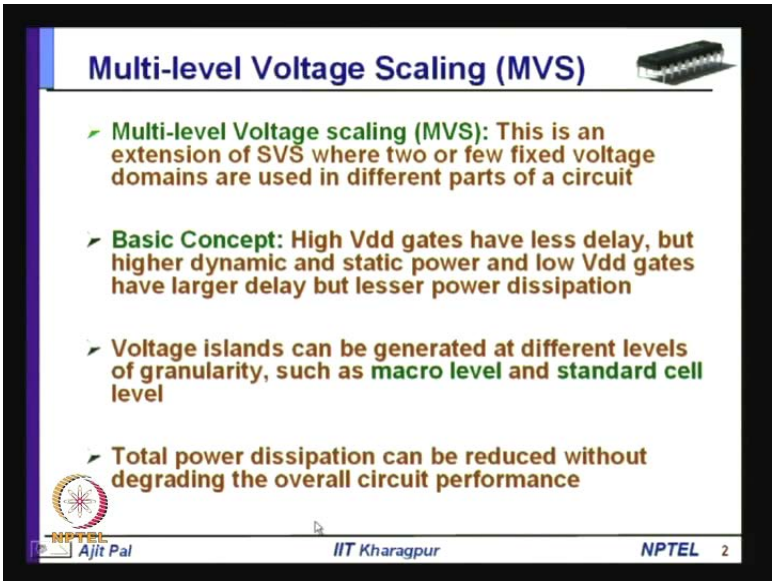

So, this is the basic concept, and we can create voltage islands at different levels of granularity such as macro level and standard cell level. So, we shall be having different voltage domains and that can be done at different levels; for example, the different levels of granularity, it can be macro level; that means, it can be a big circuit block like ALU (( )) convertor, transmitter, receiver like that or it can be at the standard cell level. So, we shall discuss both of these techniques. And then as I mentioned total power dissipation can be reduced without degrading the overall circuit performance that is the overall goal. So with this objective is mind objective in mind we shall proceed to discuss multi-level voltage scaling.

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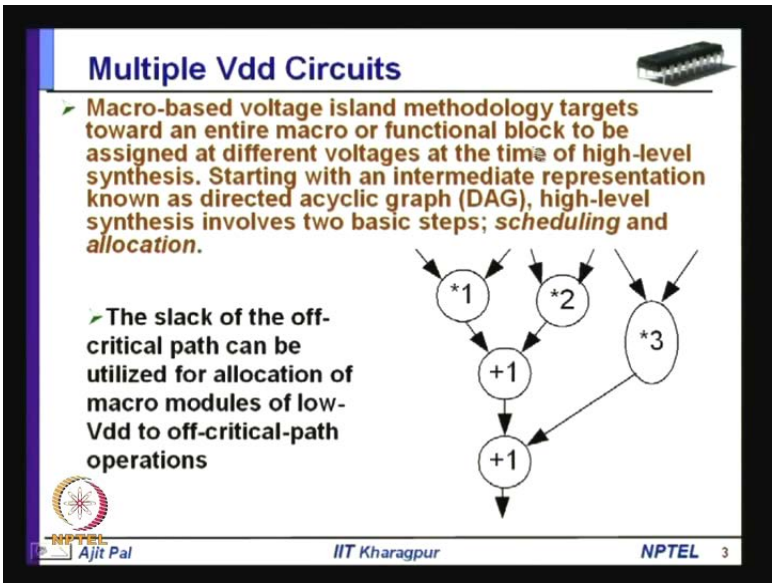

First, let us focus on macro-based voltage island methodology. Here it targets towards an entire macro or functional block to be assigned at different voltages at the time of high-level synthesis. And starting with an intermediate representation known as directed acyclic graph DAG high level synthesis involves two steps; scheduling and allocation. So, what you are doing here? We shall be performing multi-level voltage scaling at macro level, and as you know, we the it is done at high-level synthesis step stage, high-level synthesis. As we know synthesis of digital circuits involved in number of steps; one of them is the high-level synthesis; it is followed by logic synthesis, then it is followed by lay-out Synthesis.

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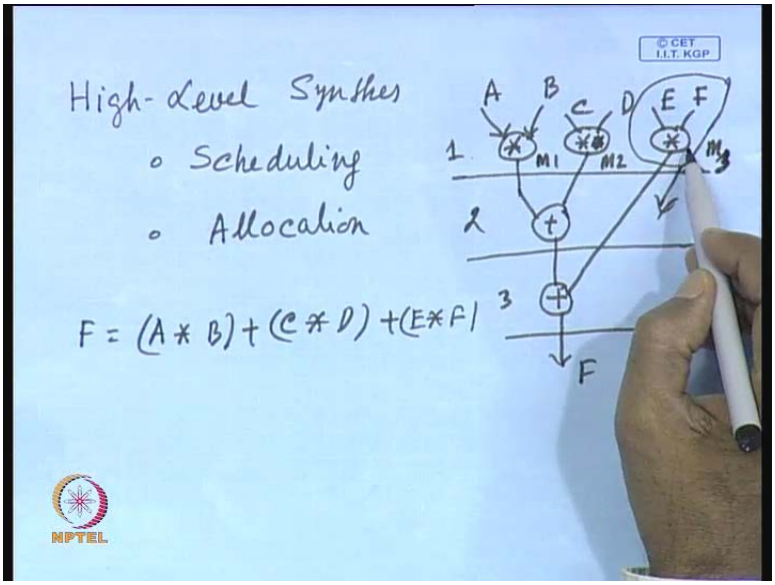

So in high-level synthesis, there are two basic steps; number one is scheduling and second step is allocation. So, what is done in scheduling? Different operations or schedules at different time steps; for example, suppose you have to perform this operation say, you have to realize this function operation say A into B plus C into D plus you are doing addition here, so E into F. So suppose, the you have to this you have to realize this function; that means, A into B plus C into D plus E into F.

So, what how the corresponding DAG will be say A B multiplication directed acyclic graph, and then you will be performing another multiplication here, sorry multiplication where you will do multiply C and D, and they will be added together with the help of an adder, and then you will require another multiplier so to perform multiplication of E and F, and then you will performing addition and here you will get your function F.

Now, what you can do? In time step, one you can schedule this multiplication, multiplication one where you are doing multiplication of A and B, and then you will also do the multiplication C and D and multiplication E and F. So, all the three are scheduled in step 1 in time step 1, and time step 2, we will do this addition, and this will be followed by another time step, where we will do this the third addition I mean, second addition. So, this is how you can do. So here, you can see in this case we have the option of scheduling this multiplication E and F either to the first time step or you can schedule it to second time step still it will perform the purpose; that means, this is the job of the scheduling. You may have the choice of scheduling some functions at different the different time steps. So, this is what is done in scheduling.

Then in allocation, you are essentially allocating different circuit elements circuit blocks to different functions. So, multiplier has to be allocated to the operation multiplication adder has to be allocated to addition. Suppose, this particular of this particular is scheduled multiplication is scheduled in this step. In this case, what you can do? Multiplier one can be allocated to this operation; multiplier two can be allocated to this operation. Then, since this these two multipliers are performing in step time step 1, this particular operation, if it is scheduled to second time step, then you can allocate multiplier 1 to perform this multiplication as well.

However, if it is scheduled in step 1 then you cannot do it, so you have to use another multiplier so a third multiply is required has to be allocated to this operation. So this has the… That means, the scheduling and allocation are interdependent, one affects the other. Scheduling may increase the requirement of hardware that is the reason why these two are inter-related and it has to be done.

Now in this particular case, what we are trying to do? We are starting with a DAG; this is the directed acyclic graph as I have told, and then the slack of the off-critical path can be utilized for allocation of macro modules of low V dd to off-critical path operations. So look at this particular directed acyclic graph. So, we find that this multiplication this multiplication, this addition; this addition that means 1, 2 and this addition 1 and 1 these two these all four are on the critical path. So but however here, what has been done this multiplier one is performing this multiplication operation, then multiplication two is being performed by another multiplier second multiplier, and addition here is being performed by a single adder in this time step and in this time step.

So, which are on these are all on the critical path, so you cannot really change their positions. However, you have a multiplier another multiplier 3, which can start competition in time step and has to finish before the end of second time step, so it has a slack. So, what you can do? You can it can overlap the multiplication operation over two time steps because of because of the slack availability of slack in this off-critical path. So, this multiplier can be assigned a lower supply voltage and obviously delay will increase it will take longer time, but as long as it does not exceed the… I mean two times time required in two time steps, then no there is no harm; that means, as long as the competition is complete before the second the third time step starts, it will you can

proceed with this particular allocation. So this is the basic idea of this multiple V dd circuit.

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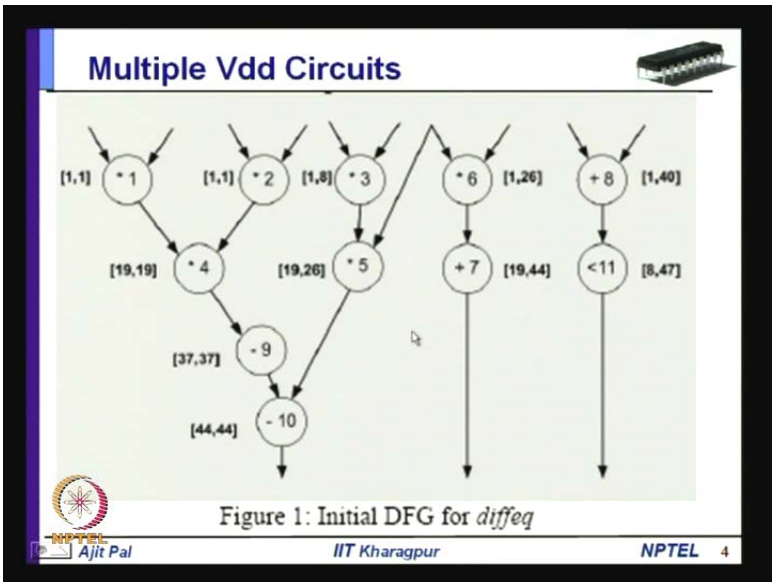

Figure 1: Initial DFG for *diffeq*

Let us take up another example; this is a this is releasing differential equation. So to solve differential equation this is a little complicated as you can see it involves a large number of multipliers and adders you can see 1, 2, 3 then 4, 5, 6, 6 there are six multiplications, then 6, 6 then there are 9 and 9 is also a multiplier. So you find a large number of multiplication and large number of additions of their and also a comparator is required this operation 11. So, 11 different operations are there. Now in this particular case, you can see this is a critical path 1, 4, 9 and 10, 2, 4, 9 and 10 are on the critical path. However, this 3 and 6 operation 3 and operation 5 are not on the critical path. So, we have the option of allocating some I mean low voltage and it lies the slack to achieve lower power dissipation.

Essentially, what you are doing here we are trading slack for lower power, and in this case as you can see these timings are given here; that means, shows that it is requiring the various timings which are shown here; that means, multiplication is requiring 18 time cycles, that is why 18 clock cycles; that is why it is starting at times tamp 19, and here it is starting at timestamp 37, and so again another 18 clock cycles are required to complete this multiplication. So, this operation can start at the 44th clock cycle.

So, this one has some slack this multiplication can start at timestamp I mean, clock cycle 1, and here there is a slack you can see even it if it starts at time clock cycle 19 8 still it will it can perform the operation. Similarly, it can start at 19 or 26, so there is a slack. So these two multiplications have slacks in the range 1 to 8 and nin19 to 26. This slack can be utilized to assign lower supply voltage to these multipliers.

Similarly, this multiplier and this addition has larger slack as you can see, because only requirement is that before 44th clock cycle you have to complete these two operations, same is to for these 2 I mean, addition and comparison. So, you can assign multipliers of lower supply voltage, what does it really mean? That means, in your library you must have macros which will operate at two different voltage levels; that means, they are optimized for different voltage levels to offer operation in two voltage levels. One can operate at V ddH high voltage level, and another can operate at lower voltage level V ddL. It is not necessary that they will have only two voltage levels; you can have more than two voltage levels as well.

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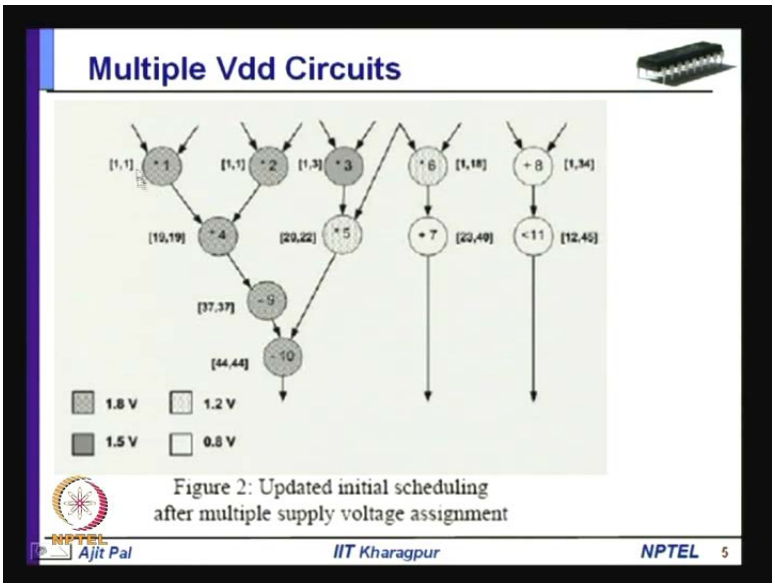

For example, in this particular case, we have the choice of 4 different voltage levels 1.8, 1.5, 1.2 and 0.84, 4 different voltage levels. As you can see the multipliers and adders which are on the critical path they have been given the voltage 1.8; that means, these modules will operate at 1.5 1.8. On the other hand, this multiplier is operating at 1.5 volt;

this multiplier is operating at lower voltage 1.2 volt still it is maintaining the time required by this.

Similarly, this multiplier is operating at voltage 1.2. This adder is this multiplier I think this is adder this adder is operating at 0.8 volt, even then it will satisfy the timing requirement. Similarly, this adder is operating at 0.8 volt and this comparator is will operate at 0.8 volt. So in this way, you can see in the allocation step we can allocate different types of multipliers, adders, comparators to different operations so and this is also known as technology binding. So technology binding means, by what by what type of circuits you are realizing a particular operation. And as you do this there will be significant reduction in power dissipation as it is shown in this particular table.

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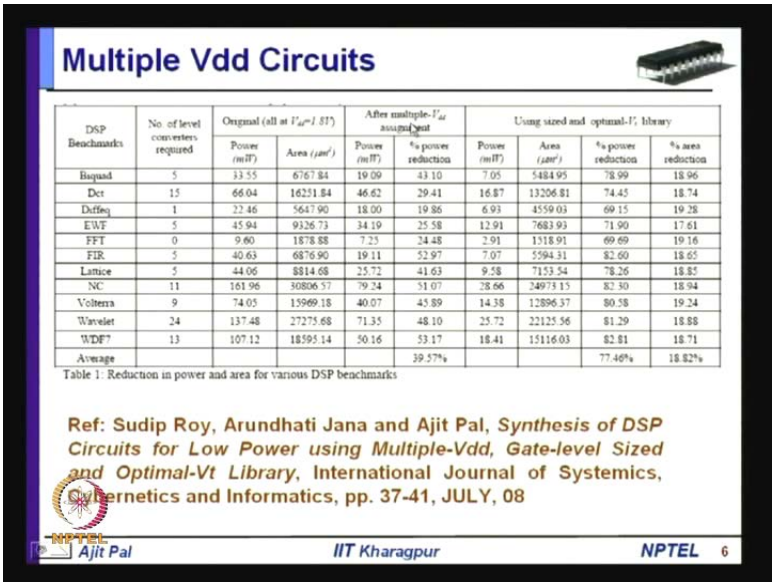

DSP Benchmarks	No. of level converters required	Original (all at V_{dd}=1.8V)		After multiple-V_{dd} assignment		Using sized and optimal-V_t library			
		Power (mW)	Area (μm^2)	Power (mW)	% power reduction	Power (mW)	Area (μm^2)	% power reduction	% area reduction
Biquad	5	33.55	6767.84	19.09	43.10	7.05	5484.95	78.99	18.96
Dct	15	66.04	16251.84	46.62	29.41	16.87	13206.81	74.45	18.74
Diffeq	1	22.46	5647.90	18.00	19.86	6.93	4559.03	69.15	19.28
EWF	5	45.94	9326.73	34.19	25.58	12.91	7683.93	71.90	17.61
FFT	0	9.60	1878.88	7.25	24.48	2.91	1518.91	69.69	19.16
FIR	5	40.63	6876.90	19.11	52.97	7.07	5594.31	82.60	18.65
Lattice	5	44.06	8814.68	25.72	41.63	9.58	7153.54	78.26	18.85
NC	11	161.96	30806.57	79.24	51.07	28.66	24973.15	82.30	18.94
Volterra	9	74.05	15969.18	40.07	45.89	14.38	12896.37	80.58	19.24
Wavelet	24	137.48	27275.68	71.35	48.10	25.72	22125.56	81.29	18.88
WDF7	13	107.12	18595.14	50.16	53.17	18.41	15116.03	82.81	18.71
Average					39.57%			77.46%	18.82%

On the other hand, if you use multiple voltages as I have told 1.5, 1.2 then this 1.5, 1.8 1.5, 1.2 and 0.8. You can have significant reduction in power dissipation. You can see there is a power reduction of about 40 percent 39.59 percent. So, there is a significant

reduction in power dissipation and of course, whenever you are using just the reducing the voltage you are not changing anything else there will be no increase in area so area will remain same. And the only reduction will be in the supply voltage and that will lead to reduction in power dissipation, and you can see you can reduce 39.57 percent.

Of course, this part we shall discuss later where we can use different threshold voltages that are used for reducing leakage current that we shall consider later. This is based on a paper published in the year 2008 in international journal of systemics Cybernetics and informatics. So, we can see this is the module level voltage scaling where you are assigning different voltages to different modules and achieving lower power.

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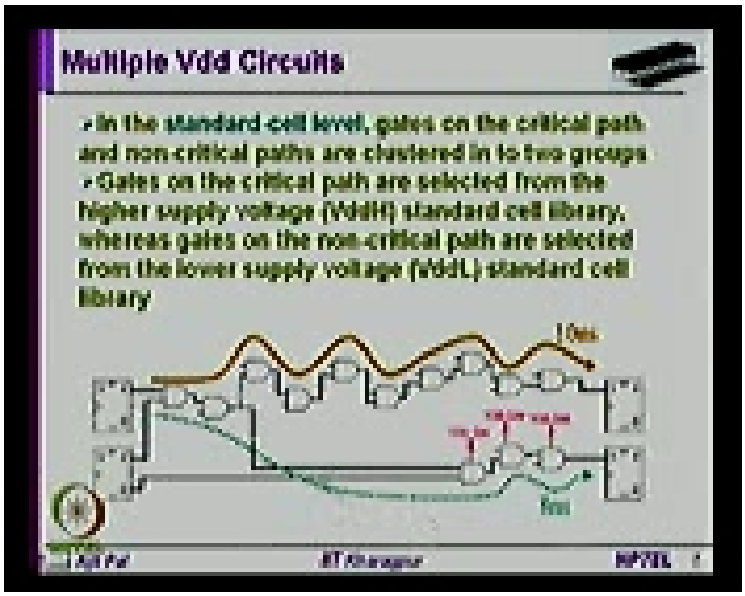

Now, coming to standard cell level as you know, you can have gates on the critical path and also there can be gates on the non-critical path. As you can see in this diagram here, this is a critical path shown by the red line, and the critical path delay is 10 nanosecond. On the other hand, this blue line the green line is showing the non-critical path these two gates are these gates are on non-critical path.

So, what you can do these gates can be assign lower voltages lower voltage V dd Low. On the other hand, gates on the critical path can be assign high V dd; V d d high, and this is and as long as the that this critical path delay 10 nanosecond is exceeded by assigning low voltage to these gate to these three gates it will serve the purpose; that means, the

performance will not be degraded. However you will be getting reduction in power dissipation, so this is the basic idea of standard cell level voltage scaling.

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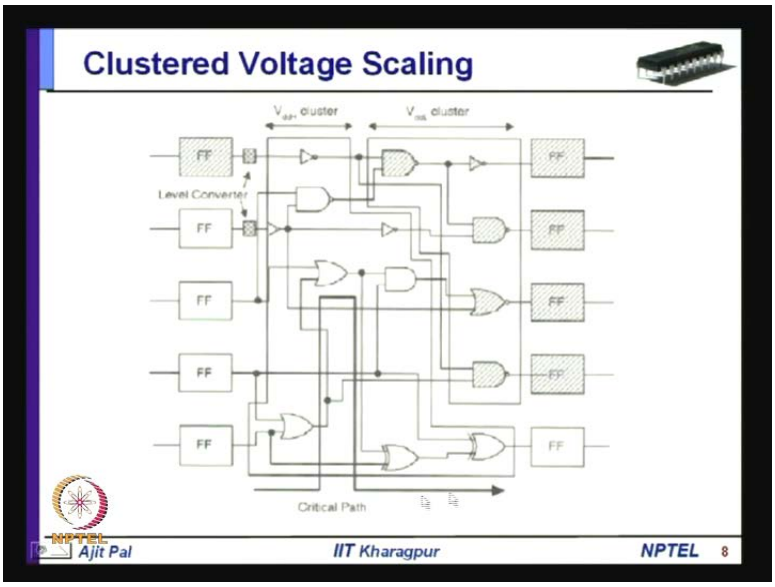

So for example, in this case the these flip-flops, these gates without any shade these are on the critical path. So, there they can be assigned higher voltages. On the other hand, this flip-flop; this n a n d gate; this flip-flop; this n a n d gate; this n o r gate; this n a n d gate they are on the non-critical path. So this is you can form a cluster of low-level voltage V ddL, and this is here you can form a cluster of V ddH. So in this way, you can have two different types of clusters and you can assign them low and high level voltages.

One point, you must have noticed here there is a mention about level converter. So later on we shall discuss about it the need for level converter, whenever you require it a when the signal passes from one voltage domain to another voltage domain there is a need for level converters. Later on, we shall discuss in detail about the need of these level converter. So for example, in this table the number of level converter requirements have been given here I did not discuss about it, but later on the need for level converter and fair level converter is needed we shall discuss later on. So, this is how the clustering can be done.

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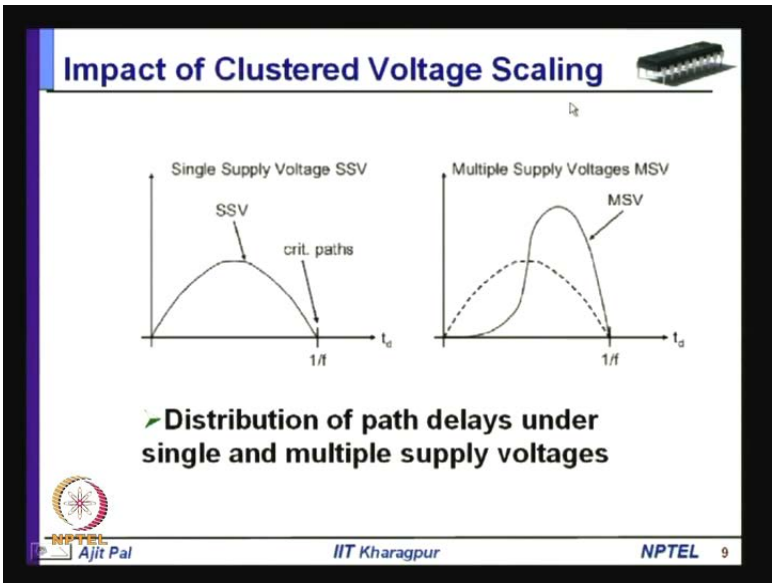

Now, what is the impact of this clustered voltage scaling? So normally, you know whenever you do static voltage scaling.

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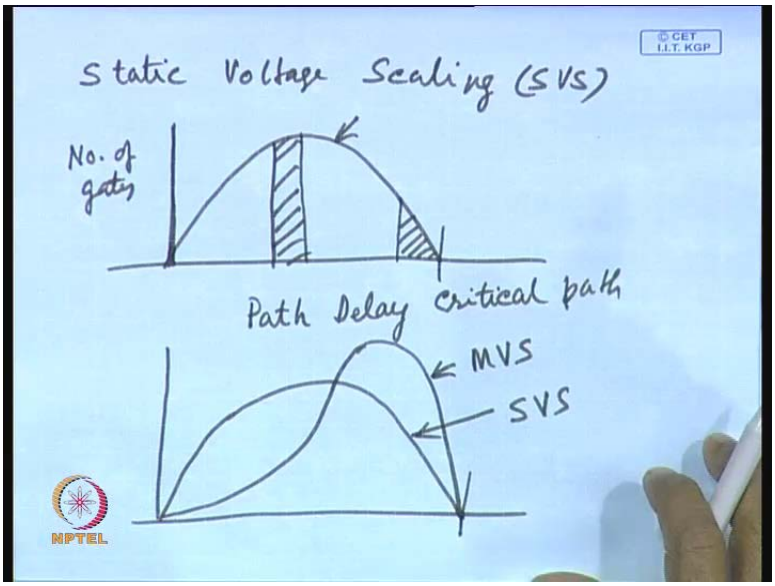

Say, we have already discussed about it static voltage scaling that is SVS. There if you consider different paths a circuit may have large number of paths, and if you plot the path delays this is the delay path delay, and on the y-axis it represents the number of gates on different paths. So you can see in this part you have got gates which are on very close to the critical path, because this is the critical path delay. On the other hand,

majority of the gates are on the very close to the typical delay of the circuit. And here is the critical path and then some gates have some gates may be having lesser delay may be having on the paths of lesser delay.

Now, whenever you do static voltage scaling, you get a curve like this, how? That means, the you have large number of paths and you have got different gates on different path delays and accordingly you can assign voltages. So, you can see the different gate gates on different delay levels. So, this is the these gates are in the medium range of delay path, so this one how it is modified whenever you go for multi-level voltage scaling.

How this particular curve is modified? It modifies in this way so this corresponds to say single voltage scaling, as you do multi-level voltage scaling it modifies in this way, number of gates remaining same and critical path delay remaining same. A large number of gates which were having smaller I mean smaller delay on this side now they are pushed to larger delay. However, they do not exceed the critical path delay, how they are pushed towards this larger delay by assigning lower supply voltage. So, as you assign lower supply voltage their delay will increase; that means, more number of parts will be having larger delay, so that this is how it is modified whenever you do multi-level voltage scaling and this corresponds to single voltage scaling. So, you can see the how the path delay modifies as you go from single voltage level scaling to multi-level voltage scaling.

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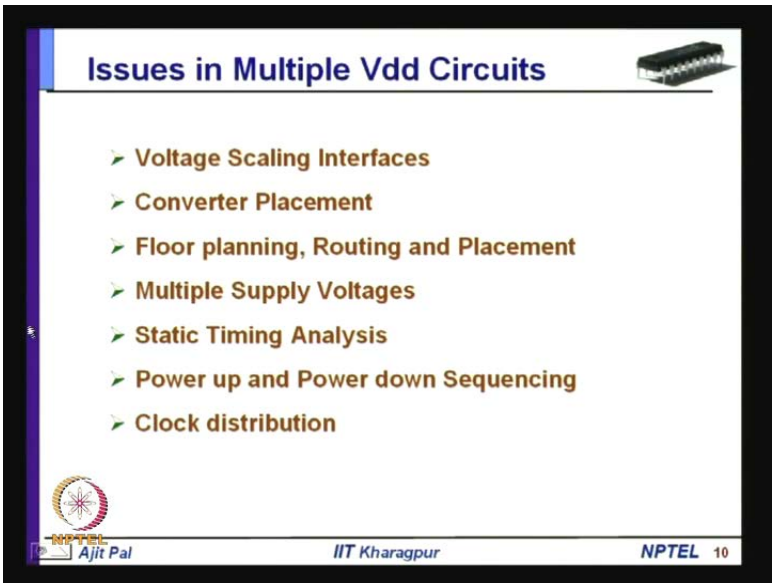

Now, we shall focus in various issues in multiple V dd circuits, we have seen how you can assign multiple voltages at macro level at standard cell level. It has got many challenges; that means, a circuit designer, if he wants to use multiple voltage domains or multi V dd circuits they have to face a number of challenges and they have to overcome them, what are the different challenges let us consider.

Number one is voltage scaling interfaces. As the signal passes from one voltage domain to another voltage domain in the in those interfaces you have to you will face some problem. What kind of problem we shall face? We shall discuss in detail, then you will see that you will require level converters in the voltage scaling interfaces, and then level converters are to be suitably placed and how and where they should be placed we shall be discussed that is also a challenge.

Then floor planning, routing and placement of not only different modules or different macros or standard cells how they will be placed, how the routing will be done, how the clustering will be done that will play a very important role. Then, multiple supply voltages, here the question will arise how many supply voltages you will use 2 or 3 or 4, that trade off has to be there is a tradeoff between delay and the reduction in power dissipation; that means, the gain performance in terms of reduction supply in power dissipation versus the you know as in the overhead that is that be increase. Overhead versus reduction in power dissipation that trade off has to be solved.

And then static timing analysis has to be solve, because you will see that static timing analysis will become complex. More complicated in whenever you go for multi-level voltage scaling, then power up and power down sequencing whenever you turning on the power and turning off the power that sequencing will become also difficult. And you have to solve you have to solve that problem, then clock distribution will be also a will be challenging in case of multi V dd circuits, so let us consider one after the other.

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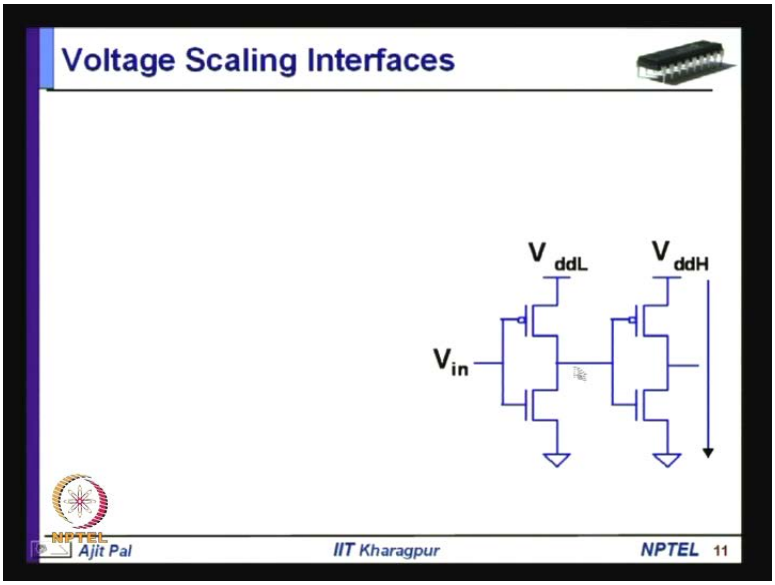

First, let us consider the voltage scaling interfaces. In this particular case, we have shown an inverter, which is in the lower voltage domain with supply voltage V ddL, and the signal is going from V ddL to V ddH. So, what kind of problem you will face in such a situation?

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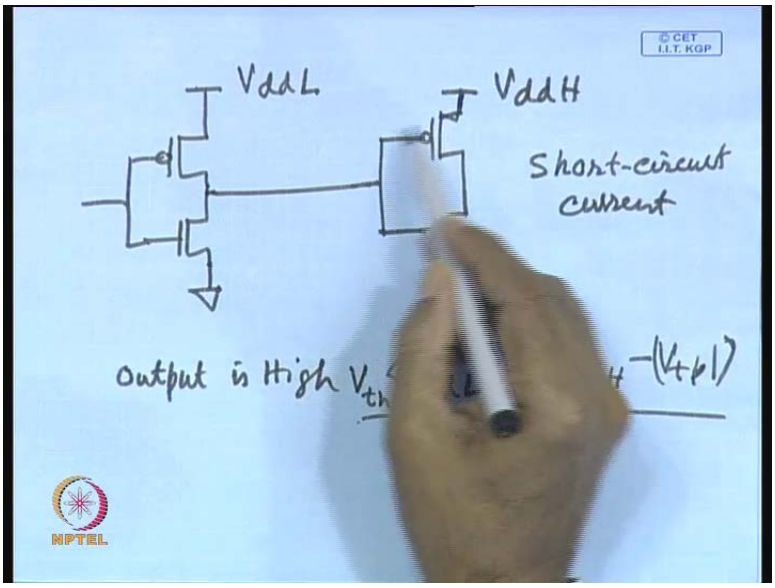

That means, you have got it did not be an inverter here for the sake of simplicity inverter is shown, it is operating at a lower voltage V ddL and signal from this inverter is going to a another inverter which is operating at higher voltage domain, V dd high. What kind of problem you can face in this particular case? The most serious problem that we will face is whenever this output is high output of this first stage is high it will produces a voltage V ddL, but what can happen this V ddL may fall in the range of say it can be greater than V tn but less than V ddH minus V tp of the this p m o s transistor; that means, if this happens what will happen; that means, this volt high level voltage is here which is higher than the threshold of this, and but you know this transistor also will remain on because voltage is less than the V ddH minus V tp. So, what will happen? This will lead to what is known as short-circuit current as you know. So the… there will be short-circuit current and this will lead to very high power dissipation, this is one problem we shall face.

Second problem that we shall face is whenever you are driving, even if this is not the situation; that means, if this condition is not satisfied, it may be higher that the V ddH minus V tp, even then the drive to the stage will decrease because at high level this voltage is lesser than V ddH. So, delay of the next stage will increase because of lesser drive that is coming from the previous stage; that means, whenever the signal is passing from low voltage domain to high voltage domain then there may be drive problem that will lead to larger delay of the next stage. And also this will lead to larger power

dissipation in the next stage, because of short-circuit power dissipation. So this problem has to be overcome.

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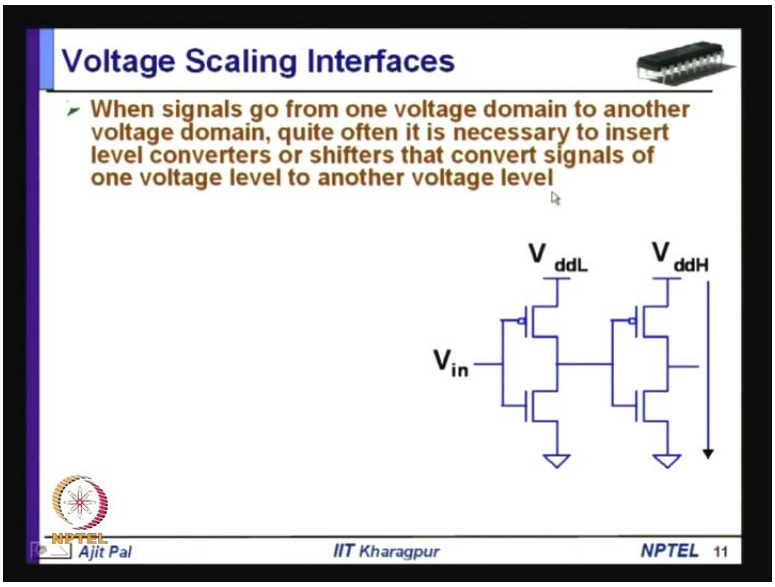

So, how this problem can be solved quite often it is necessary to insert level converters or shifters that convert signals of one voltage level to another voltage level. So you have to insert in between this low voltage domain and high voltage domain. Let us assume this is the low voltage domain; and this is the high voltage domain you have to put a level converter l c. So level converter will raise the voltage level of this side to high level it will receive input from lower voltage domain, and produce output at high voltage domain is the that is the function of level converter that is used in this case.

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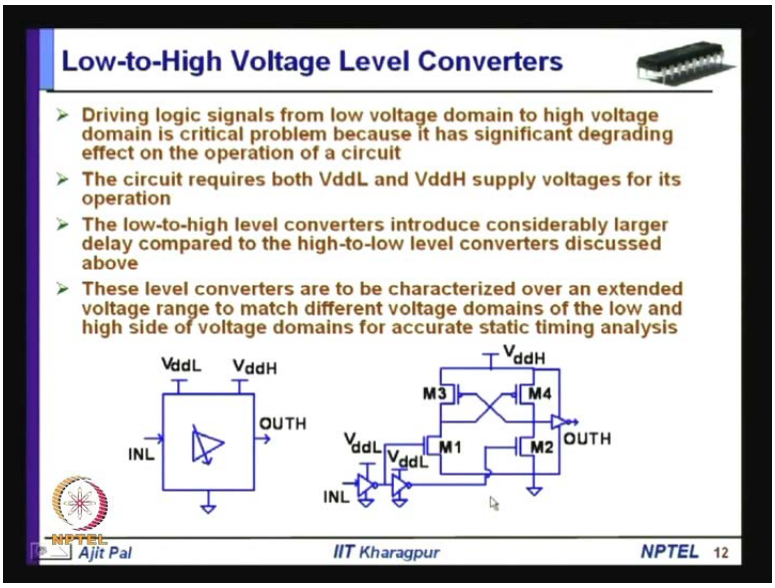

So, this I have already explained so you require a level converter to avoid this static power dissipation on this circuit, how can you realize a level converter? So, this is the type of level converter you can use.

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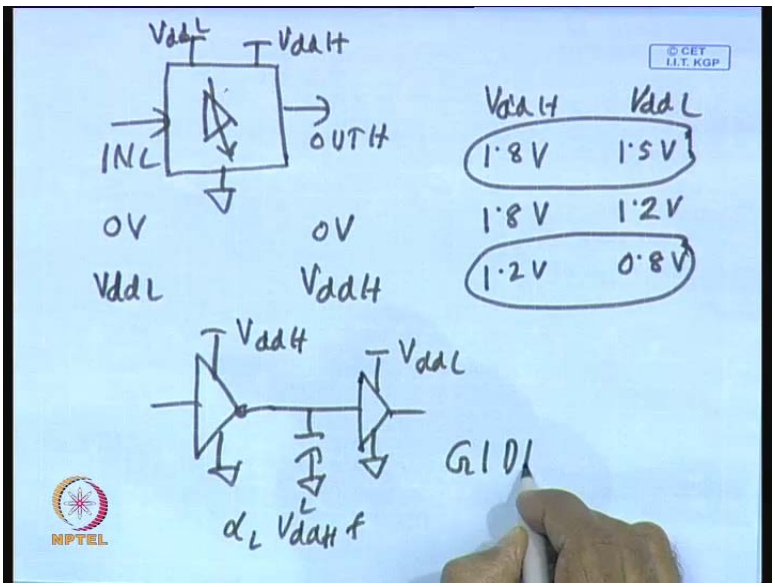

That means, you will require a level converter which is given the symbol there is a block it is receiving input at low level it is producing output at high level, and it is provided with V ddL to different voltage supply voltages V ddH and of course, there is a common ground. So, this is the symbol of a level converter in inside a symbol is given here which

is essentially; that means, it is changing the level that it signifies that, and it can be realized by using a circuit like this.

There are many ways it can be realized, but this is the most common form of level converter that is being used. So in this case, as you can see we have a two cross-coupled p m o s transistors acting like a kind of flip-flop. So, the base is the gate of this is connected to the collector of the other m o s transistor; I mean drain of the other transistor, and gate of this m o s transistor is connected to drain of the other transistor. So these are cross-coupled, then you have got two nMOS transistors here m 1 and m 2 which are receiving input from two inverters. So low-level input is given here and you have got two inverters which are operating at low voltage domains, and they are applying input only to the n m o s transistor not to the pMOS you note that this is very important. The inverter output is fed only to the n m o s transistor, and also the input to the next stage next inverter is also fed to the another inverter; that means, the these two voltages these two inputs are complimentary in nature, because they are coming from the output of inverters.

So, whenever this inverter turns on this will force this point to go down to 0 turning on this, and as it turns on this will this output will this output will be forced to one, and as it go at is become ones this transistor will be it will turn off there will be kind of regenerative action. As a result very quickly, output will change to at at this point it will change to high level and you will get the output; that means, when the input is low you were getting output low, but since this particular inverter is having a supply voltage V ddH here the output will be will correspond to high level.

Similarly, when this input is high this output is low, and this output is high this output is high means this transistor will turn on this will make this particular m o s transistor to turn on. And this will make this high and that will turn it off, and as it turn it off then this voltage will be low and you will get output low.

So that means, the input polarity at this point and at this point it is identical only difference is in the their levels. So, if this voltage is 0 level you will you get 0 level here. If this voltage is high level you get high level here. However that means, here 0 corresponds to 0 volt, in this case 0 corresponds to 0 volt, but here high-level corresponds to V ddL, and here high-level corresponds to V ddH. So that is the

difference in the input and output, so this kind of level converter can be used can be realized, as you can see this is little complicated, and obviously you have to characterized over an extended voltage range to match different voltage domains of low and high side of voltage domains for accurate static timing analysis.

So, as I mentioned earlier static timing analysis will be a problem; that means, this particular level converter has to be characterized for different voltage pairs; for example, you may be having voltage domains as I mention it the one van be 1.8 volt, another can be 1 .5 volt, this is one pair, then it can be 1.8 volt, and the 1.2 volt, or it can be 1.2 volt and 0.8 volt, so this kind this type of voltage pairs are there. So, this is your V ddH and this is your V ddL. So for all these pairs the level converters are to be characterized by characterization; I mean what will be their worst-cased delay, what will be their power dissipation and so on. So these are to be characterized for different voltage pairs, because you may likely to use level converters at the at the interface of different voltage domains circuits of different voltage domains, so you may have several such voltage pairs.

Now, coming to high-to-low level voltage level converters, what is the problem you can face whenever high to voltage level converters are used. So without a level converter the voltage swing of the signal reaching the low V dd domain is 0 to high V dd. So in this case, you know without level converter the voltage swing is more. This causes higher switching power dissipation and high leakage power dissipation due to g I d l effect.

That means, in this case what you are doing an inverter, which is operating at high voltage domain V ddH is driving another inverter, which is operating at low voltage domain. So in this case, what happens here there is a capacitor; this load capacitor has to be charge and this cause this charge corresponding to this voltage domains; that means, the power dissipation will increase because the voltage is high. As you know the voltage is power dissipation is proportional to alpha l V dd square. In this case, V ddH square then f; that means, the power dissipation will be unnecessarily be high, and also since you are driving with a higher gate voltage this will lead to higher power dissipation in this gate because of that GIDL effect, gate induced drain leakage effect, I have already discussed about it.

So, this to overcome this problem, the another the rise and fall time may be long leading to increase in short-circuit power dissipation this is another thing. Here you know since it

is changing over a larger voltage the rise and fall times may be little long, and that may be lead to short-circuit power dissipation of the stage, because of all these regions it is necessary to insert a level converter even when signal is passing from high voltage domain to low voltage domain. So the level converters which goes from high voltage domain to low voltage domain this is a symbol and you can realized in this manner.

Here, you can see it is essentially two inverter stages with a low-level supply voltage. Supply voltage corresponds to low-level voltage domain, and here you have got input coming from high voltage domain, and output is generated with that will corresponds to low voltage domain. And in this particular case, circuit is quite simple so static timing analysis is simpler compared to the previous case in a where the circuit is more complicated. However, it introduces buffer delay and its impact on static timing analysis is small compared to the previous case.

Now, let us come to the question of converter placement, we have discussed about different types of converters that you will require. Now you have to place them, where do you place them. As I mentioned in a circuit, you will be having different voltage domains, this will be one voltage domain, this can be another voltage domain. Where do you put the level it is not that it will be placed in the middle, so you have to either place them in a low voltage domain or in the high voltage domain; that means, if it is a low voltage domain and if it is a high voltage domain either it has to be placed or it has to be placed here. The level converter has to be placed, where the placement is beneficial.

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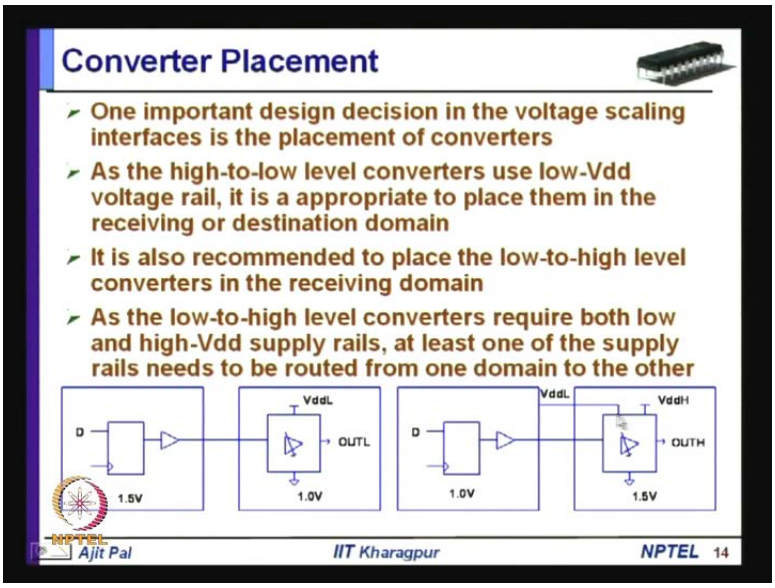

So, this is a very important design criteria design decision in the voltage scaling interface is the placement of inverter, where do you place. So, as the high-to-low level converters use low V dd voltage level, it is appropriate to place them in the receiving or destination domain. We have seen that this particular level converters requires only low voltage domain supply V ddL. So therefore, it is more logical say suppose this is V ddH domain, and this is V ddL domain. So it is more beneficial to place it in this domain because supply voltage rarely is reaching the low voltage domain in any case. So, there will be no need to connect a low voltage power to this for this level converter, if you place it here you will require that means this is this corresponds to high voltage domain. So you have to take the power the low voltage domain power line to this to this side if you place the level converter here. That is the reason here reason why it is advisable to place a level converter in a low voltage domain or destination domain.

And the rise and fall time may be long leading to increase in short-circuit power dissipation, sorry so as the high voltage level converter use low V dd so I have already discussed that. So it is also recommended to place the low-to-high level converters in the receiving domain, so the that was a previous case. In this case also, it has been found that it is beneficial to put them in the destination domain or receiving domain.

So, at the low-to-high voltage converters require both low and high v d supply rails, at least one of the supply rails needs to be routed from one domain to the another. So, we

have seen a low-to- high level converter voltage domain convertor requires both the supplies V ddL and V ddH. So wherever, you place it you have to take one of the power supply to the another domain, as it is shown in this case. So here, you can see this is a high voltage domain this is a low voltage domain, so level converter has been placed in a low voltage domain, so there is no need to route the do the routing for low voltage domain power supply to for this level converter, because it is already available here.

But you can see here the it is going from low voltage domain to high voltage domain. So your level converter is here which converts from low voltage domain to high voltage domain. So in the this particular level converter can be placed here or here, but it is beneficial to place in the low voltage domain, because this reduces some of the timing problems, but V ddL has to be taken from the low voltage domain to high voltage domain area. So, this will increase the routing area and obviously, the your cost of routing will increase so this is the challenge of placement of level converter.

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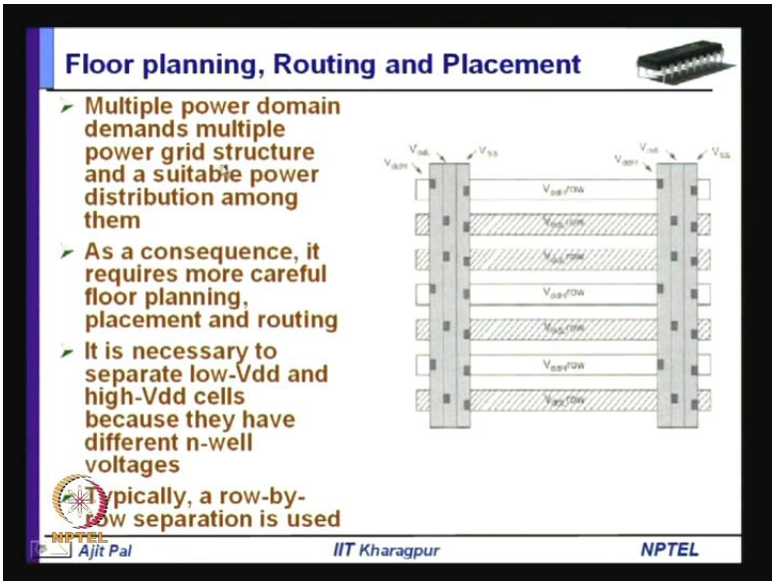

Coming to floor planning routing and placement, so multiple power domains demands multiple power grid structure and a suitable power distribution among them. What is being done you can see different rows, this is a row corresponds to high voltage domain without any shade, and this particular row corresponds to standard cell of low voltage domain. This is another row where you have got standard cells of low voltage domain. So you have done the kind some kind of clustering, you have place them in a particular

row, row by row placement has been done. For the convenience of connecting power rails see you can see on both sides you have got power rails V ddH V ddL and V ss that is the ground line, and then you will you are you are providing power from these power rails either from this side or from this side to high voltage domain and low voltage domain and so on.

So, this is how the routing and placement is done, and you have to plan floor planning is also done, and whenever you are using multi-level voltage scaling. So multiple power domains require multiple power grid structure and a suitable power distribution among them. As a consequence, it requires more careful floor planning placement and routing as I have discussed. It is necessary to separate low V dd and high V dd cells because they will have different n-well voltages, I hope this point is clear to you.

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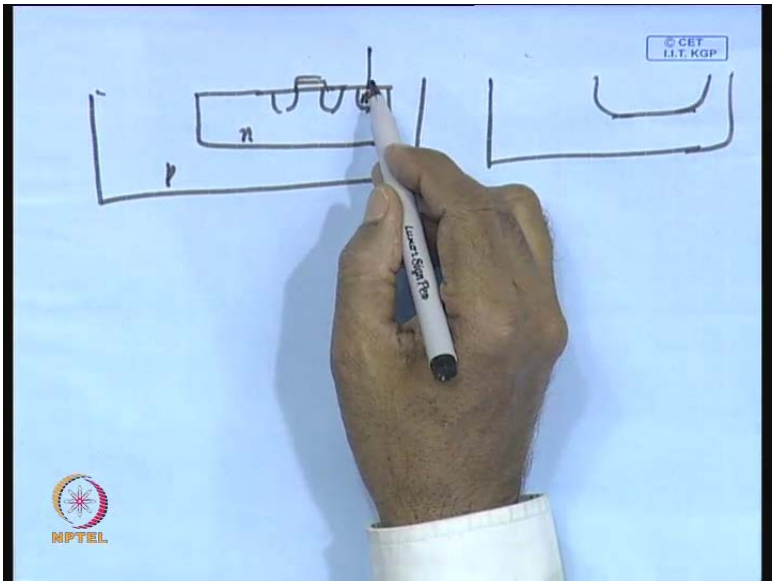

So, whenever you are realizing transistors of different voltages. As you know suppose, this is a n-well, this is a well this is a structure, and if there is a m o s transistor here, and this well is connected say suppose this is your n type and this is p type, and this is n plus this has to be connected to different voltages.

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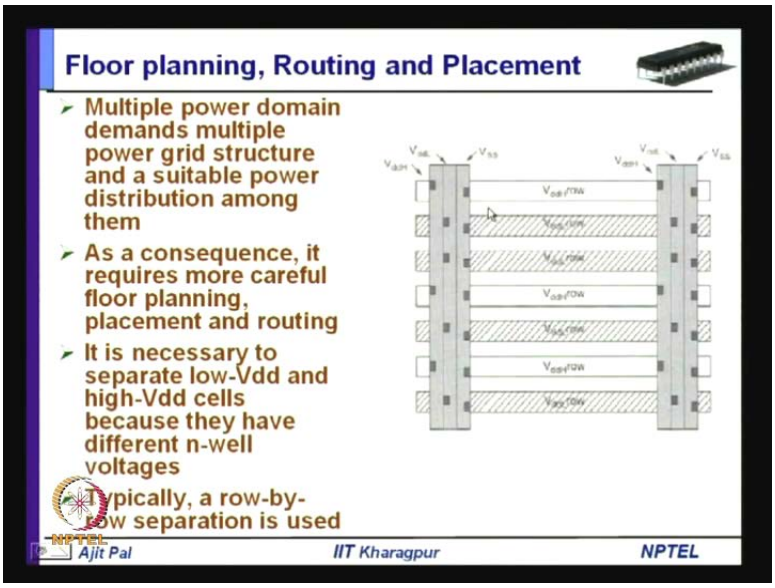

So, this well has to be connected this well has to be separated from voltage domain of another well, and a separation is necessary in whenever you are using multiple voltage domain, because this has to be connected to one voltage, this well has to be connected to another voltage and so on. So, this separation is necessary in multiple voltage domains, and typically a row by row separation is used as it is shown in this particular diagram. So you have to maintain some spacing between these rows so separations are equal. So this is about floor planning routing and placement.

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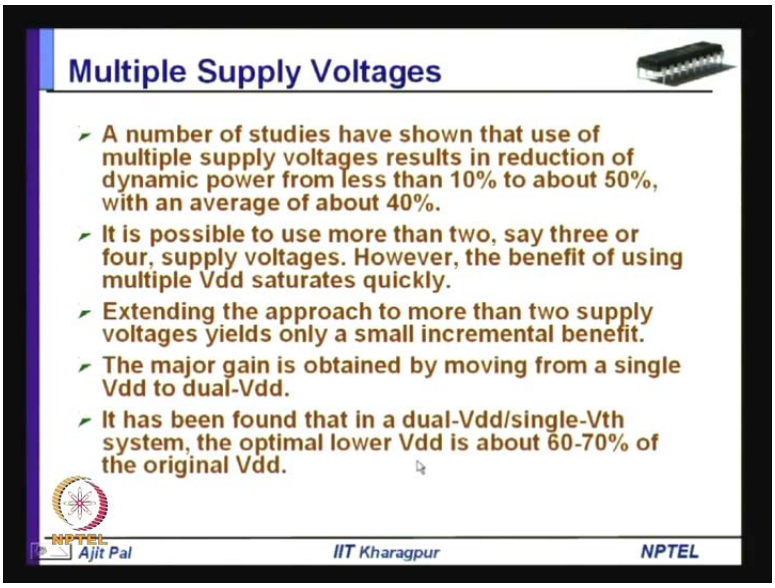

Coming to multiple supply voltages, a number of studies have shown that use of multiple supply voltages results in reduction in the dynamic power from less than 10 percent to 50 percent with an average of forty percents; that means, on the average you can have 40 per cent reduction in supply voltage; I mean power dissipation, question is will how many supply voltages you will use 2 or 3 or 4? So it is possible to use more than 2 say 3 or 4 supply voltages. However, the benefit of using multiple V dd saturates quickly; that means, it becomes say point of diminishing return as you go from 2 V dd to 3 V dd or from 3 V dd to 4 v dd.

So and major gain is obtained whenever you use dual V dd. So, whenever you go from single V dd to dual V dd, there is significant reduction in power dissipation, but whenever you go from dual V dd to triple V dd you do not get that much saving. So it has been found that dual V dd versus single V dd system the optimal lower that another point is what will be the supply voltage, and it has been found that the lower V dd has to be about 60 to 70 percent of the high V dd.

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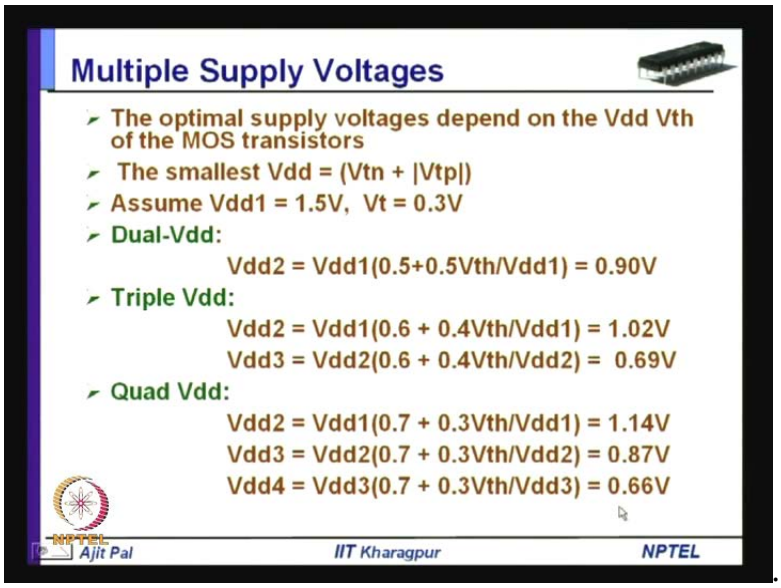

And in this particular slide different voltages are shown this is the high V dd 1.5 with threshold voltage 0.3, and whenever you go for dual V dd second supply voltage is 0.9 volt, and this is the thumb rule that is being used to choose the second V dd. Whenever you go for triple V dd the other two voltages that means the second voltage and third voltage is selected which is 1.02 and 0.69, and the first one voltage is 1.5 volt, and whenever you use quad V dd and this is the thumb rule used to choose different supply voltages V dd 1 is 1.5 volt, V dd 2 is 1.1 4 volt, V dd 3 is 0.8 7 and V dd 4 is 0.66 volt.

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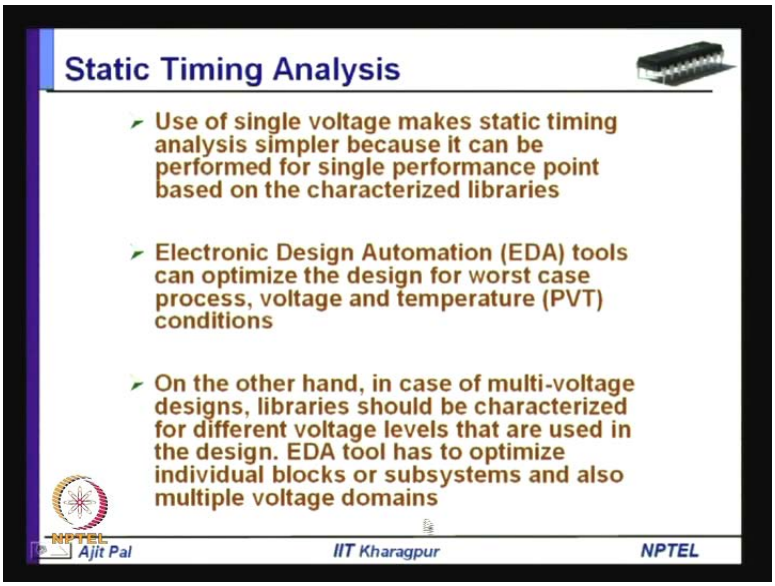

Coming to static timing analysis as I mention use of single supply voltage makes static timing analysis simpler, because it can be perform for single performance point based on characterized libraries. So, it will be operating at one voltage and for different; I mean it can consider the worst-case process voltage and temperature variations and characterize corresponding to a single voltage, and as I mention whenever you go for multiple voltages then electronic design automation tools can; I mean, it becomes say more problematic decision for e d a tools, because in multiple voltage domains library should be characterize for different voltage levels that are used in the design. EDA tool has to optimize individual blocks or subsystems and also multiple voltage domains; so static timing analysis become significantly difficult, whenever you go for multiple voltage circuits.

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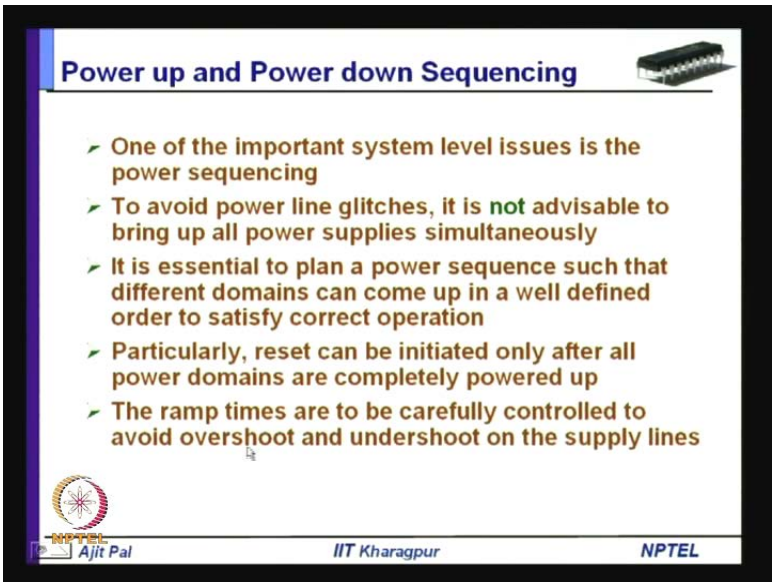

Coming to the another issue power up and power down sequencing, this is a very important system level issue, and to avoid power line glitches it is not advisable to bring up all power supplies simultaneously; that means suppose, you have got three voltage domains 1.5, 1 and 0. 8, you should not bring up all the supply voltages together that may lead to power line glitches. So to avoid those glitches, you have to you have to plan a power sequence such that different domains can come up in a well-defined order to satisfy correct operation, and you have to follow some sequence to achieve good performance.

Particularly reset can be initiated only after power domains are completely powered up, so you will the power supply require some time for stabilization. So unless the power supply is stabilized, you should not reset a circuit. For and resetting the circuit is important to bring it to a initial known state, and that is why resetting has to be done only when the circuit is completely powered up. The that is why the ramping up and ramping down is necessary to avoid overshoot and undershoot on the supply lines.

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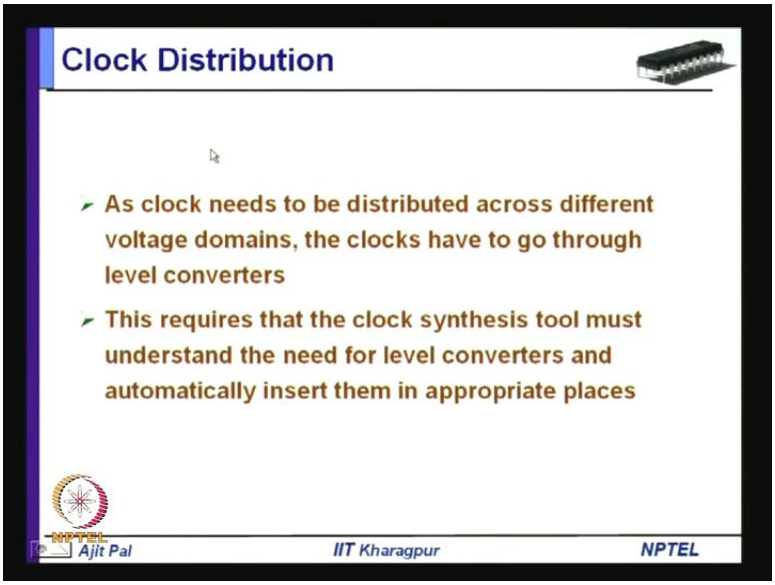

Similarly, the last problem is clock distribution, as clock needs to be distributed across different voltage domains the clocks have to go through level converters. So just like signals approaching from one signal level to another one voltage domain to another voltage domain, clock may be also passing from one voltage domain to another voltage domain. So, you have to place level converters for the clock distribution circuit, and this requires that clock synthesis tool must understand the need for level converters and automatically insert them in appropriate places.

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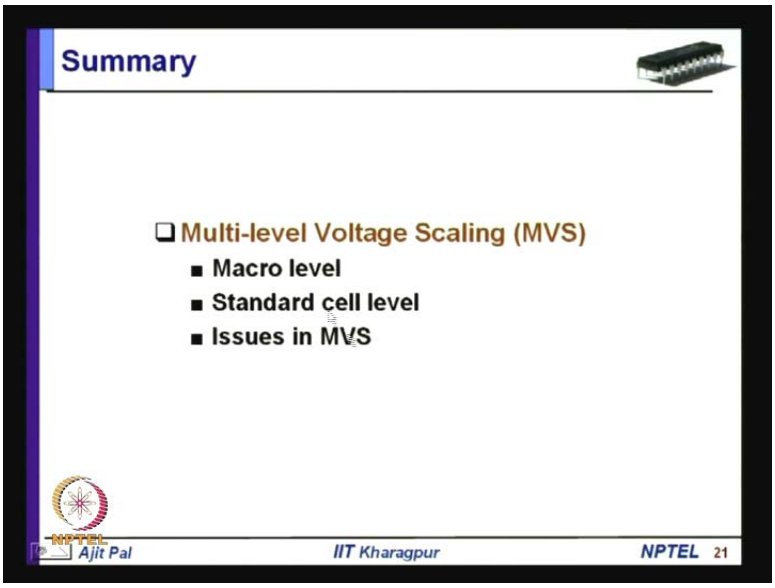

To summarized, we have discussed multi-level voltage scaling in this lecture, and we have discussed two types of multi-level voltage scaling using macro level cells and standard cells, and we have discussed various issues that you will encounter in multi-level voltage scaling. So with this, we have come to the end of today's lecture. In the next lecture, we shall discuss about dynamic voltage and frequency scaling, and also you know that continuous that automated voltage and frequency scaling techniques. Thank you.